DISTINCTIVE CHARACTERISTICS

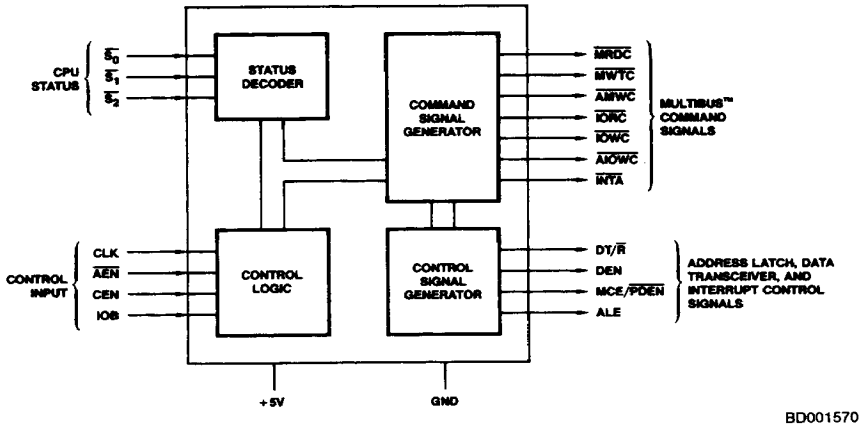
- Bipolar drive capability
- Three-state output drivers
- Multi-master or I/O bus interface
- Flexible system configurations

GENERAL DESCRIPTION

The 8288 optimizes 8086 or 8088 operations by providing command and control timing generation when the CPU is in maximum mode. It provides for highly flexible configurations for larger systems. It also adds powerful bipolar drive capability to the system.

The 8288 is implemented in bipolar technology in a 20-pin plastic or ceramic DIP.

BLOCK DIAGRAM

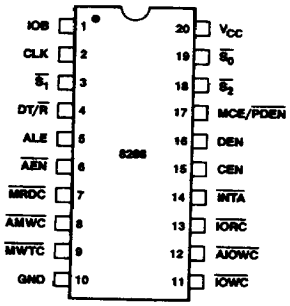


BD001570

Publication # 03358 | Rev. C | Amendment /0
Issue Date: April 1987

CONNECTION DIAGRAM
Top View

DIPs



CD001840

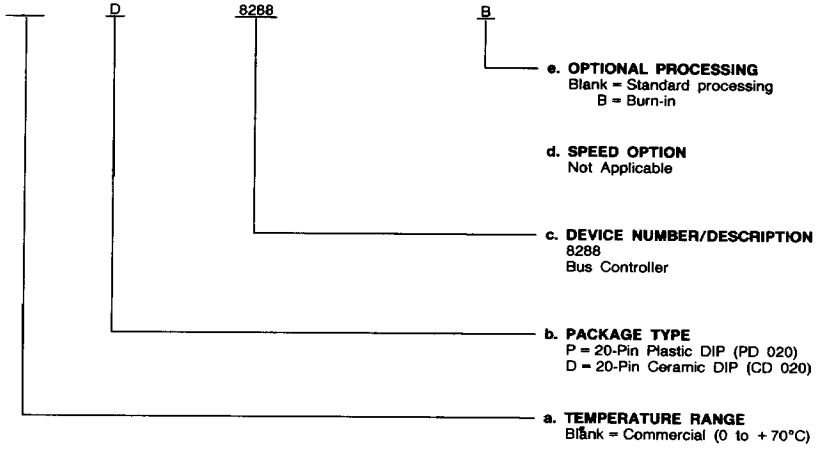
Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Temperature Range
b. Package Type
c. Device Number
d. Speed Option
e. Optional Processing



Valid Combinations	
P, D	8288
	8288B

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
19, 3, 18	$\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$	I	Status. These signals are the status input pins from the microprocessor. The 8288 decodes these inputs to generate command and control signals.
2	CLK	I	Clock. Clock signal from the clock generator.
5	ALE	O	Address Latch Enable. This signal strobes an address into the address latches. The latching occurs on the falling edge (HIGH to LOW) transition.
16	DEN	O	Data Enable. This signal enables the data transceivers onto the data bus (local or system).
4	DT/$\overline{R}$	O	Data Transmit/Receive. This signal determines the direction of data flow through the transceivers.
6	$\overline{AEN}$	I	Address Enable. This signal enables the 8288 command outputs at least 115ns after it becomes active LOW. When this pin goes inactive, it 3-states the command output drivers.
15	CEN	I	Command Enable. This signal, when LOW, enables all command outputs and the DEN and $\overline{PDEN}$ control outputs are forced to their inactive states.
1	IOB	I	Input/Output Bus Mode. When strapped HIGH, the 8288 functions in the I/O Bus mode. When LOW, the 8288 functions in the System Bus mode.
12	$\overline{AIOWC}$	O	Advanced I/O Write Command. The $\overline{AIOWC}$ gives I/O devices early indication of a write instruction by issuing an I/O Write Command earlier in the machine cycle.
11	$\overline{IOWC}$	O	I/O Write. This signal tells an I/O device to read the data on the data bus.
13	$\overline{IORC}$	O	I/O Read. This signal tells an I/O device to drive its data onto the data bus.
8	$\overline{AMWC}$	O	Advanced Memory Write. The AMWC gives memory devices an early indication of a write instruction by issuing a memory write command earlier in the machine cycle.
9	$\overline{MWTC}$	O	Memory Write. This signal instructs the memory to record the data present on the data bus.
7	$\overline{MRDC}$	O	Memory Read. This signal instructs the memory to drive its data onto the data bus.
14	$\overline{INTA}$	O	Interrupt Acknowledge. This signal informs the interrupting device that its interrupt has been acknowledged and drives the vectoring information onto the data bus.
17	MCE/ $\overline{PDEN}$	O	Master Cascade Enable/ Peripheral Data Enable. Dual Function pin: MCE (IOB LOW): This signal occurs during an interrupt sequence. Its function is to read a Cascade Address from a master Priority Interrupt Controller onto the data bus. $\overline{PDEN}$ (IOB HIGH): This signal enables the data bus transceiver for the I/O Bus during I/O instructions. It performs the same function for the I/O Bus that DEN performs for the system bus.

DETAILED DESCRIPTION

COMMAND AND CONTROL LOGIC

The command logic decodes the three CPU status lines ($\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$) to determine what command is to be issued.

This chart shows the meaning of each status "word."

$\overline{s}_2$	$\overline{s}_1$	$\overline{s}_0$	Processor State	8288 Command
0	0	1	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

I/O BUS MODE

The 8288 is put into the I/O Bus mode by strapping the IOB pin HIGH. This mode allows one 8288 Bus Controller to handle two external buses. This allows the CPU to access the I/O Bus with no waiting involved. In the I/O Bus Mode, all I/O command lines ($\overline{INTA}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$) are always enabled. When the processor initiates an I/O Command, the 8288 immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control the I/O bus transceiver. There is no arbitration present in this system, so the I/O command lines should not be used to control the system bus. Normal memory access requires a "Bus Ready" signal ($\overline{AEN}$ LOW) before it will proceed. The IOB mode is recommended if I/O or peripherals dedicated to one processor exist in a multiprocessor based system.

SYSTEM BUS MODE

The 8288 is put into the System Bus mode by strapping the IOB pin LOW. This mode is used when only one bus exists. No command is issued until 115ns after the $\overline{AEN}$ line is activated. Bus arbitration is assumed, and this logic will inform the bus controller via the $\overline{AEN}$ line when the bus is free for use. Both I/O commands and memory wait for bus arbitration.

COMMAND OUTPUTS

To prevent the processor from entering unnecessary wait states, the advanced write commands initiate write procedures early in the machine cycle.

The command outputs are:
$\overline{MRDC}$ – Memory Read Command
$\overline{MWTC}$ – Memory Write Command
$\overline{IORC}$ – I/O Read Command
$\overline{IOWC}$ – I/O Write Command
$\overline{AMWC}$ – Advanced Memory Write Command
$\overline{AIOWC}$ – Advanced I/O Write Command
$\overline{INTA}$ – Interrupt Acknowledge

$\overline{INTA}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. Its purpose is to inform an interrupting device that its interrupt is being acknowledged and that it should place vectoring information onto the data bus.

CONTROL OUTPUTS

The Data Enable (DEN), Data Transmit/$\overline{Receive}$ (DT/$\overline{R}$) and Master Cascade Enable/Peripheral Data Enable (MCE/$\overline{PDEN}$) are the control outputs of the 8288. The DEN signal determines when the external bus should be enabled onto the local bus while the DT/$\overline{R}$ determines the direction of the data transfer. These two signals usually go to the chip select and direction pins of a transceiver.

The MCE/$\overline{PDEN}$ function is determined by the IOB selection. When IOB is HIGH the $\overline{PDEN}$ serves as a dedicated data enable signal for the I/O or Peripheral System Bus.

INTERRUPT ACKNOWLEDGE AND MCE

The MCE signal is used during an interrupt acknowledge cycle if the 8288 is in the System Bus mode (IOB Low). An interrupt sequence consists of two interrupt acknowledge cycles occurring back to back. No data or address transfers take place during the first cycle. Logic should be provided to mask off MCE during this cycle. Just before the second cycle begins the MCE signal gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE (Address Latch Enable) strobes it into the address latches. On the leading edge of the second interrupt cycle the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

The MCE signal is not used if the system only contains one PIC. If this is the case the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

ADDRESS LATCH ENABLE AND HALT

Address Latch Enable (ALE) occurs during each machine cycle and serves to strobe the current address into the address latches. ALE also serves to strobe the status ($\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$) into a latch for halt state decoding.

COMMAND ENABLE

The Command Enable (CEN) input acts as a command qualifier for the 8288. If the CEN pin is HIGH the 8288 functions normally. If the CEN pin is pulled LOW, all command lines are held in their inactive state (not 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus devices and resident bus devices.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Temperature (Ambient) Under Bias ..... 0°C to +70°C
All Output and Supply Voltages ..... −0.5V to +7.0V
All Input Voltage ..... −1.0V to +5.5V
Power Dissipation 1.5W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits between which the functionality of the device is guaranteed.

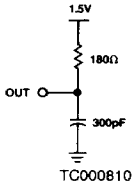
DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameters	Description	Test Conditions	Min	Max	Units
V_C	Input Clamp Voltage	$I_C = -5mA$		−1	V
I_{CC}	Power Supply Current			230	mA
I_F	Forward Input Current	$V_F = 0.45V$		−0.7	mA
I_R	Reverse Input Current	$V_R = V_{CC}$		50	μA
V_{OL}	Output Low Voltage Command Outputs	$I_{OL} = 32mA$		0.5	V
	Control Outputs	$I_{OL} = 16mA$		0.5	V
V_{OH}	Output High Voltage Command Outputs	$I_{OH} = -5mA$	2.4		V
	Control Outputs	$I_{OH} = -1mA$	2.4		V
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
I_{OFF}	Three-State Leakage	$V_{OFF} = 0.4$ to 5.25V		100	μA

3

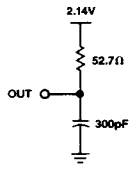
SWITCHING TEST CIRCUIT

3-State to High



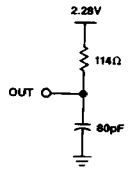
TC000810

Command Output Test Load



TC000800

Control Output Test Load



TC000790

SWITCHING TEST INPUT, OUTPUT WAVEFORM

Input/Output

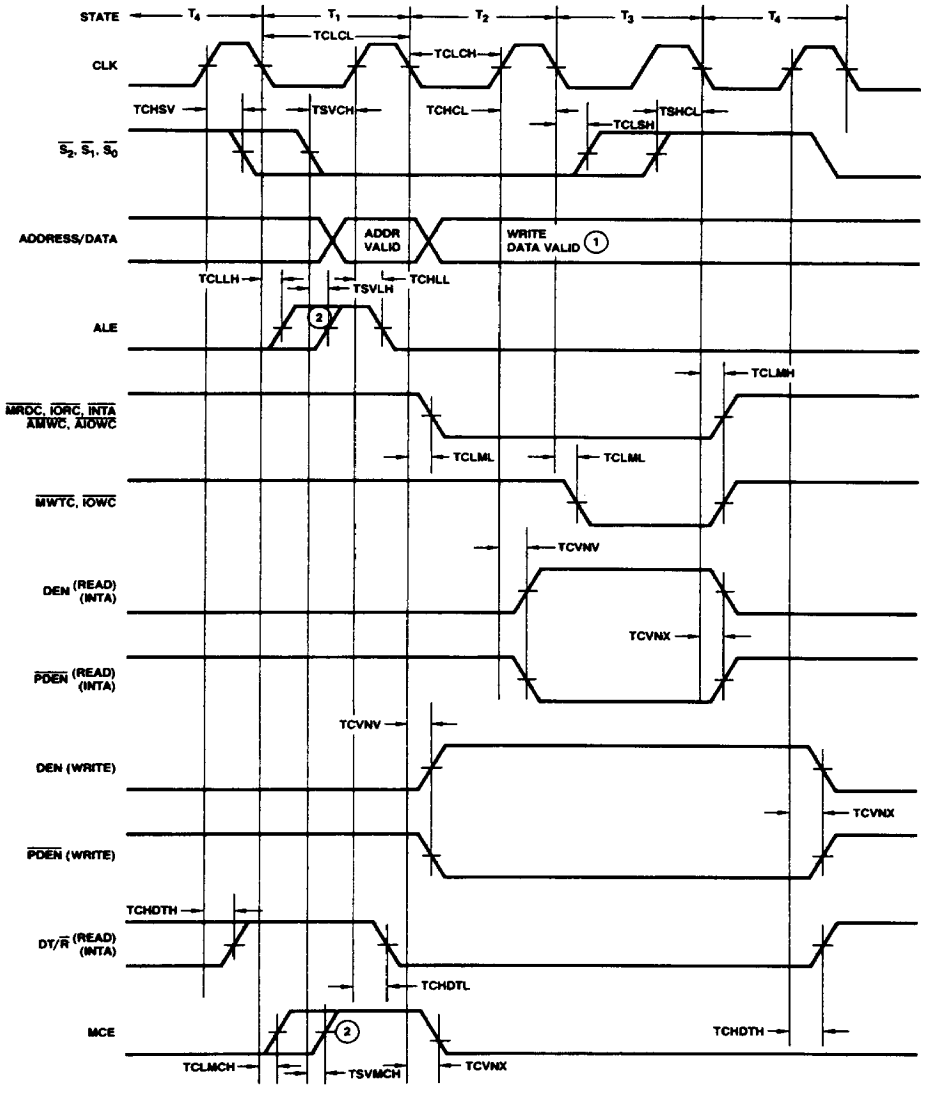
WF001870

AC Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0." The clock is driven at 4.3V and 0.25V. Timing measurements are made at 1.5V for both a logic "1" and "0."

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions			Min	Max	Units
Timing Requirements							
TCLCL	CLK Cycle Period				100		ns
TCLCH	CLK Low Time				50		ns
TCHCL	CLK High Time				30		ns
TSVCH	Status Active Setup Time				35		ns
TCHSV	Status Active Hold Time				10		ns
TSHCL	Status Inactive Setup Time				35		ns
TCLSH	Status Inactive Hold Time				10		ns
TILIH	Input Rise Time	From 0.8V to 2.0V				20	ns
TIHIL	Input Fall Time	From 2.0V to 0.8V				12	ns
Timing Responses							
TCVNV	Control Active Delay				5.0	45	ns
TCVNX	Control Inactive Delay				5	45	ns
TCLLH TCMCH	ALE MCE Active Delay (from CLK)					20	ns
TSVLH TSVMCH	ALE MCE Active Delay (from Status)					20	ns
TCHLL	ALE Inactive Delay	$\overline{MRDC}$			4.0	15	ns
TCLML	Command Active Delay	$\overline{IORC}$			7	35	ns
TCLMH	Command Inactive Delay	$\overline{MWTC}$			10	35	ns
TCHDTL	Direction Control Active Delay	$\overline{IOWC}$		I_{OL} = 32mA I_{OH} = −5mA C_L = 300pF		50	ns
TCHDTH	Direction Control Inactive Delay	$\overline{INTA}$				30	ns
TAELCH	Command Enable Time	$\overline{AMWC}$				40	ns
TAEHCZ	Command Disable Time	$\overline{AIOWC}$				40	ns
TAELCV	Enable Delay Time				95	200	ns
TAEVNV	AEN to DEN	Other		I_{OL} = 16mA I_{OH} = −1.0mA C_L = 80pF		20	ns
TCEVNV	CEN to DEN, PDEN					25	ns
TCELRH	CEN to Command					TCLML	ns
TOLOH	Output Rise Time	From 0.8V to 2.0V				20	ns
TOHOL	Output Fall Time	From 2.0V to 0.8V				12	ns

SWITCHING WAVEFORMS

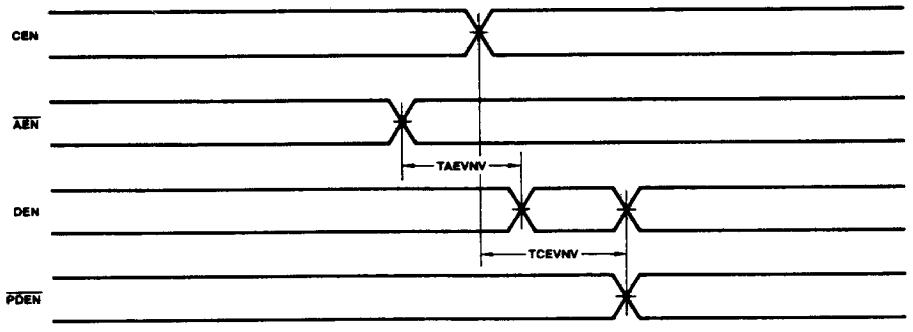


WF002110

Notes: 1. Address/data bus is shown only for reference purposes.
2. Leading edge of ALE and MCE is determined by the falling edge of CLK or status going active, whichever occurs last.
3. All timing measurements are made at 1.5V unless specified otherwise.

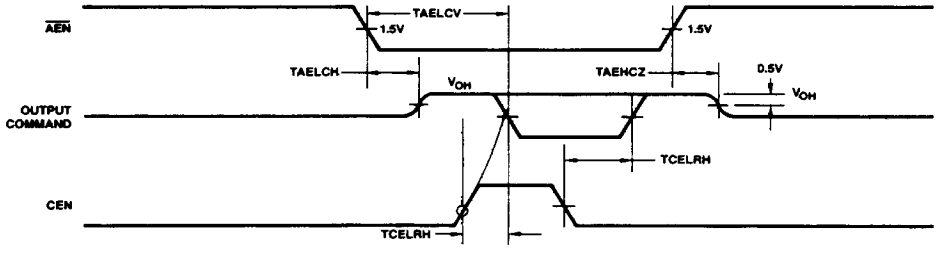
SWITCHING WAVEFORMS (Cont.)

DEN, PDEN QUALIFICATION TIMING



WF002040

ADDRESS ENABLE (AEN) TIMING (3-STATE ENABLE/DISABLE)



WF002050

Note: CEN must be low or valid prior to T_2 to prevent the command from being generated.