Radio Shack®

Service Manual

26-1130

TRS-80®
5-Meg
Hard Disk

Catalog Number 26-1130

CUSTOM MANUFACTURED IN U.S.A. BY RADIO SHACK, A DIVISION OF TANDY CORPORATION

TRS-80® 5-Meg Hard Disk

Service Manual

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****
Warnings
****

Do not move or tilt the Hard Disk Drive unit while the drive is running. Permanent damage to the drive may occur resulting in the loss of information or damage to the disk.

Do not drop the Hard Disk Drive unit from any height as permanent damage to the drive may occur.

1/ Overview

The TRS-80 5-Meg Hard Disk Unit consists of two non-removable 5.25-inch disks. There are four Read/Write heads (one on each side of each platter) which move towards or away from the center of the disk as needed.

The Disks and Read/Write heads are fully enclosed in a sealed chamber. A special air filteration system prevents dust and other particles, which destroy data, from reaching the disks. Another filtering system allows pressure equalization with the "outside" air pressure.

UNDER NO CIRCUMSTANCES MUST THE CHAMBER BE UNSEALED IN THE FIELD. A CLASS 100 CLEAN ROOM ENVIRONMENT IS NEEDED FOR UNDER-THE-BUBBLE REPAIR.

On all Hard Disk Units, flaws in the media are indentified at the factory before the disk drives are delivered to the customer. Attached to the bottom of each disk drive unit is a "Media Error Map". This map identifies the flawed tracks on that particular unit.

2/ Technical Specifications

Basically, the hard disk unit consists of two platters (or disks) lying parallel within the unit. There are also four Read/Write heads, one on each side of each platter. These heads move towards or away from the center of the disk as needed.

When a unit is purchased, there will be no more than 3 tracks per head with defects. This will not exceed 8 tracks per drive with defects. Also there will not be any flaws on Track 0.

Disks/Platters	2
Heads/Recording Surfaces	4
Tracks per Inch	254
Cylinders	153
Tracks	612

Hard Disk	Cylinders	Tracks	Sectors	Bytes
1	153	612	19,584	5,013,504
---	1	4	128	32,768
---	---	1	32	8,192
---	---	---	1	256

AC Power Requirements
50/60 Hz +/- 0.5 Hz
100/115 VAC installations (90 to 127 V)
200/230 VAC installations (100 to 253 V)
Fuse 2.5 at 250 Volts (Internal)

Power Supply (Primary Drive) Operating Characteristics

	Min	Typ	Max	Units
Vin Range				
Input Select 115V	90	115	135	Vrms
Input Select 230V	198	230	264	Vrms
Line Frequency	47	50/60	63	Hz

Output Voltages	V1 +5V	4.95	5.1	5.25	Volts
	V3 +12V	11.4	12	12.6	Volts
	V4 -12V	11	-12	-15	Volts
Output Current	V1 +5V	2.50		5.0	Amps
	V3 +12V	.75		2.0	Amps
	V4 -12V	.005		.10	Amps
Ripple Voltages	V1 +5V			50	mV
	V3 +12V			150	mV
	V4 -12V			150	mV
Efficiency		70			%
Hold Up Time					
Full Load, Low Line		10			mSec
Full Load, Nom Line		16			mSec
Over-Voltage Protection		5.80		6.80	Volts

Power Supply (Secondary Drive) Operating Characteristics

		Min	Typ	Max	Units
Vin Range					
Input Select 115V		95	115	135	Vrms
Input Select 230V		180	230	264	Vrms
Line Frequency		47	50/60	63	Hz
Output Voltages	+5V	4.75	5	5.25	Volts
	+12V	11.4	12	12.6	Volts
	-12V	-11	-12	-15	Volts
Output Current	+5V	.45		2.5	Amps
	+12V	.75		2.0	Amps
	-12V	.005		.10	Amps
Load Regulation (measured by varying load on considered output from typ to either min or max rated load)	+5V	5		5	%
	12V	-5		5	%
	-12V	-8.3		25	%

Ripple Voltages	+5	50	mV
	12V	150	mV
	-12V	150	mV
Efficiency	65		%
Over-Voltage Protection	5.80	6.80	Volts

Dimensions	
Height	5.50 in (13.97 cm)
Width	14.00 in (35.56 cm)
Length	15.00 in (38.10 cm)
Weight	
Primary	15.5 lbs (33.10 kg)
Secondary	12.5 lbs (27.5 kg)

Environment	
Ambient Temperature	50 to 95 degrees F. (10 to 35 degrees C.)
Relative Humidity	8% to 80%
Maximum Wet Bulb	78% non-condensing
Heat Dissipation	
Altitude	operating: 0 to 6000 feet (0 to 1829 meters) storage: -1000 to 12000 feet (-305 to 3656 meters)

Warm-Up Period	
Minimum On Power-Up	2 minutes
Minimum to Turn System On After Turning System Off	15 seconds

Hard Disk Drive	
Disk Organization	
Tracks per Unit	612
Tracks per Platter	306
Sectors per Track	34
Bytes per Sector	256
Cylinders per Disk	153
Average Latency	8.34 msec
Rotational Speed	3600 rpm +/- 1%
Recording Density	7690
Flux Density	7690
Track Density	254

Storage Capacity (Hard Disk)	
Unformatted	
Bytes per Track	10400

Bytes per Surface	1.59 MEG
Bytes per Drive	6.33 MEG
Formatted	
Bytes per Drive	5 M (Primary)
	5 M (Secondary)

3/ Connections

Connecting Your Primary Drive to a Model III

Be sure all power is OFF.

Note: Master unit does not come with Data Out connectors. These are supplied with each secondary unit and require installations.

Locate the hard disk expansion cable. Connect one end to the I/O bus card edge of your Model III. Be sure the cable exits the rear of the computer so that it won't bind.

Connect the opposite end of this cable to the COMPUTER IN connector, located on the rear panel of the primary drive.

Connect the power cord to the primary drive. Plug the other end into an appropriate AC power source.

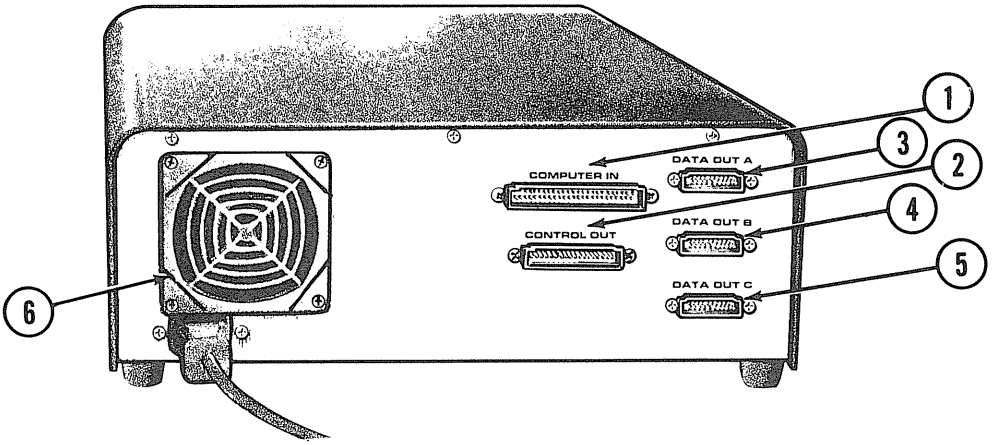


Figure 1. Back Panel of Hard Disk Drive

1. Computer In (50-pin) Connect the Hard Disk Expansion Cable from the I/O bus card edge of the Model III to this jack.

2. Control Out (34-pin) Connect one end of a Secondary Hard Disk Expansion Cable to this connector. The other end connects to the first secondary drive.

3. Data Out A (20-pin) Connect one end of the Data Cable from the first secondary drive to this connector.

4. Data Out B (20-pin) Connect one end of the Data Cable from the second secondary drive to this connector.

5. Data Out C (20-pin) Connect one end of the Data Cable from the third secondary drive to this connector.

6. Filter

Connecting Secondary Drives

The secondary drives are connected to the computer via the primary disk drive. The drives must be stacked with the primary drive on top of the secondary drives.

Locate the secondary hard disk expansion cable. Connect one end to the Control In jack of the secondary drive and the other end to the Control Out jack of the previous drive in the chain. If you have only two hard disk drives, this connector connects to the primary drive.

If you have another secondary drive, connect the second secondary hard disk expansion cable to the Control Out jack and the other end to the Control In jack of the next drive in the chain.

Locate the data cable. Connect one end to the appropriate data jack (A for the first secondary drive, B for the second, and C for the third). Connect the other end to the Data In jack on the secondary drive.

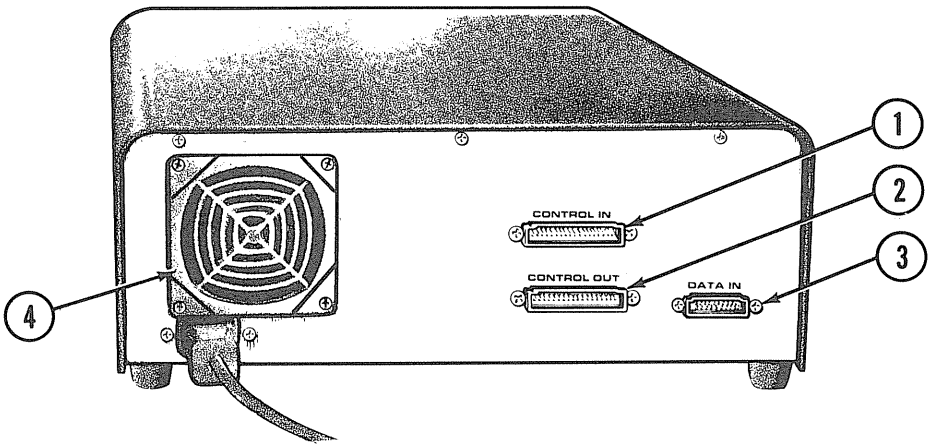


Figure 2. Back Panel of Secondary Hard Disk Drive

1. Control In (34-pin) Connect one end of a Secondary Hard Disk Expansion Cable to this jack. The other end connects to the previous Hard Disk Drive.

2. Control Out (34-pin) Connect one end of a Secondary Hard Disk Expansion Cable to this jack. The other end connects to the next secondary drive.

3. Data In (20-pin) Connect one end of the Data Cable from the the primary drive to this jack.

4. Filter

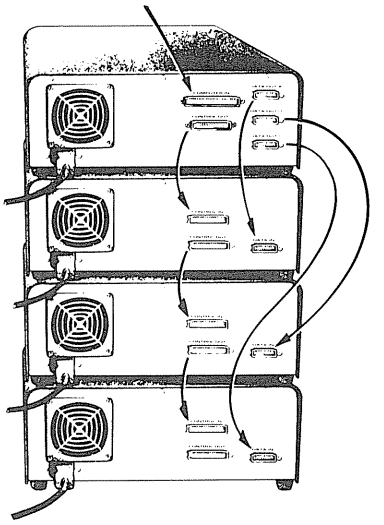


Figure 3. A Fully Configured Hard Disk System

Connecting the Primary Hard Drive to the Model I

To connect the hard disk drives to the Model I you need a Model I Kit (Catalog Number 26-1132). Included in this kit are:

- A Model I Adapter Cable
- Three Diskettes:
  - HARD DISK OPERATING SYSTEM
  - XTRA
  - INITIALIZATION

Important Note: The Expansion Interface must be buffered before the hard disk can be connected to your Model I. Instructions on how to determine whether the Expansion Interface is buffered are given next.

There are two types of Buffered Expansion Interfaces. The first type is recognized by its cables. The flat ribbon cable between the Expansion Interface and the Keyboard will have a black box on it. There will also be a 3-wire cable with a din plug type connector in the middle. See Figure 4.

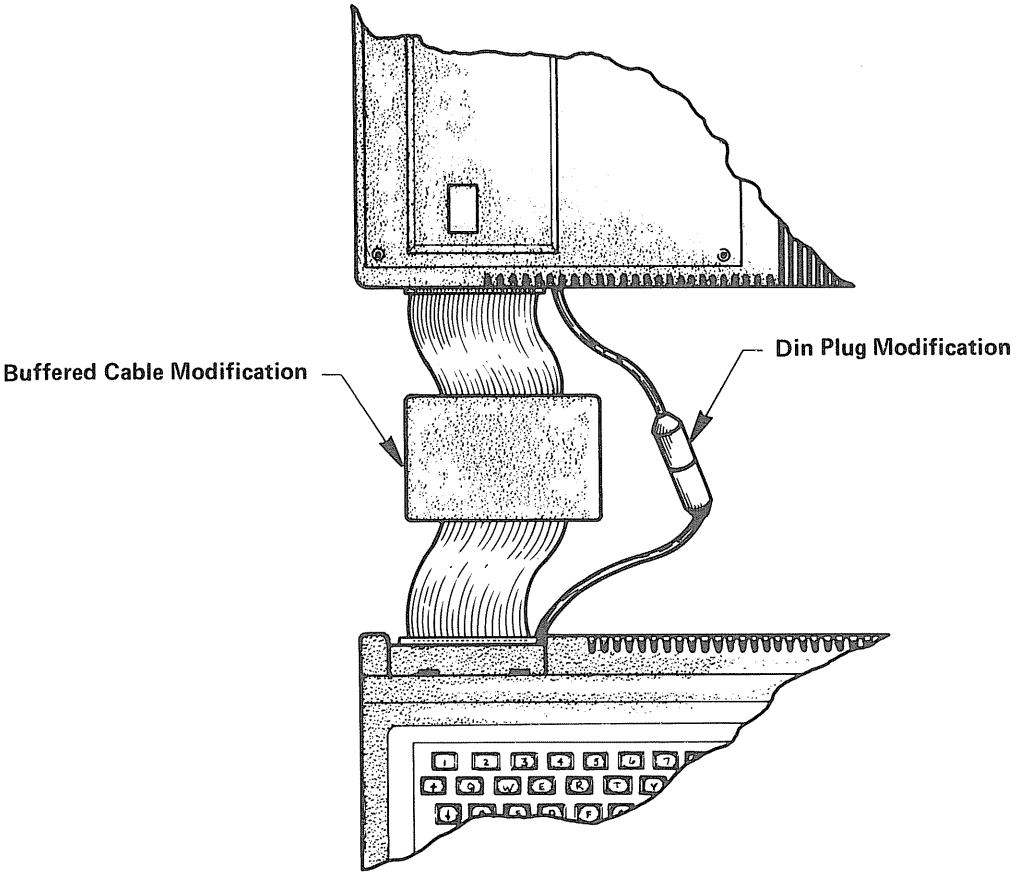


Figure 4. Expansion Interface/Keyboard with Buffered Modification

If the computer does not have these cables, then you must look inside the Expansion Interface through the bottom cover.

Look through the vents on the bottom cover for two rows of eight memory chip sockets. (The sockets may or may not contain memory chips.)

If the ROWS of sockets run long ways in the interface -- parallel to the keyboard -- then the computer is buffered and is ready to be connected to the hard disk. See Figure 5.

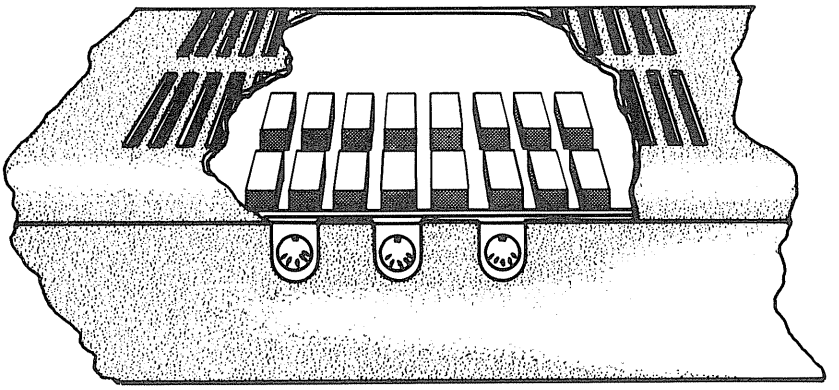


Figure 5. Buffered Expansion Interface as Viewed From the Bottom

If the ROWS of sockets run perpendicular to the keyboard, the computer is not buffered. See the illustration below:

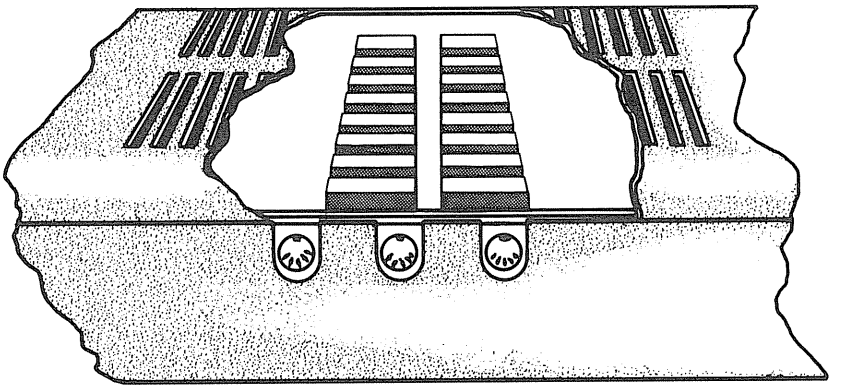


Figure 6. Non-buffered Expansion Interface Viewed From the Bottom

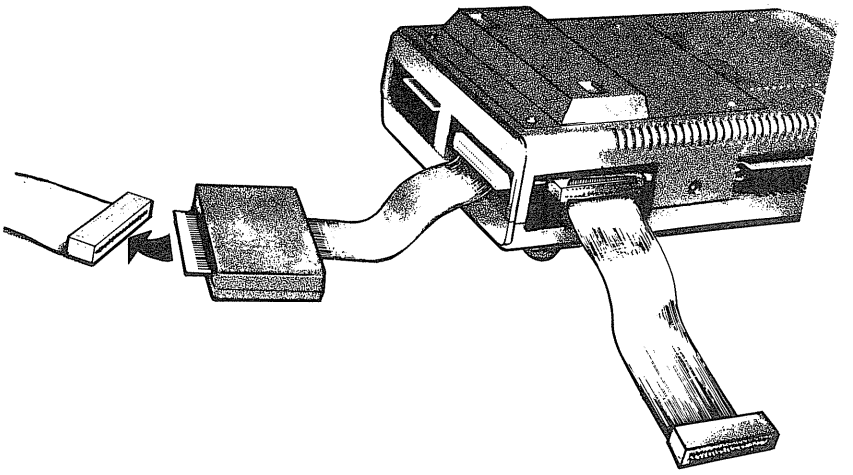


Figure 7. Connecting the Hard Disk to Your Model I

1. Locate the Model I Adapter Cable. One end has a connector (40-pin). The other end has a black box with a card edge exiting it.

2. Connect the 40-pin connector (the end with the cable) to the Bus Extension port (also called screen printer port) of your Expansion Interface. The cable should exit towards the bottom of the expansion interface.

3. Connect the card edge end to the card edge connector of the Hard Disk Expansion Cable (50-pin). The Hard Disk Expansion Cable should exit the bottom of the connector.

4. Connect the other end of the Hard Disk Expansion Cable to the COMPUTER IN connector of the primary hard drive. The cable should exit towards the bottom of the connector.

The primary hard disk drive is now connected.

4/Power-Up and Power-Down

Model III System Power-Up

1. Make sure all power is OFF and all floppy diskette drives are empty.

2. Turn on all peripheral equipment (such as a printer or additional floppy diskette drives)

3. Turn on the primary hard drive by turning the POWER KEY clockwise. This also turns on all secondary drives. All secondary drives' power lights should come on.

4. Turn the computer ON.

5. Insert either the INITIALIZATION diskette or the START-UP diskette in floppy Drive 0.

6. Press RESET. In a few seconds the screen shows a large LDOS logo.

   If the LDOS logo does not appear, repeat the above steps, making sure you inserted the diskette properly.

7. The screen then shows this prompt:

   LDOS Ready

   Since you've not yet initialized your Hard Disk System, the computer is now operating as a Floppy Disk System, the only way it can operate until you initialize it.

   If you've initialized the Hard Disk System, you can remove the START-UP diskette. You only need it to start up or reset.

To operate the system for floppy disk only, hold down the <CLEAR> key and press the RESET button. (You must keep the <CLEAR> key down until LDOS Ready appears.)

Model III System Power-Down

1. The LDOS Ready prompt should be the last line on your screen. If not, press <ENTER> or exit your program so that it appears.

2. Remove all floppy diskettes from their drives.

3. Turn off any peripheral equipment.

4. Turn off the hard disk drive by turning the power key on the primary drive counterclockwise. This turns off all the drives.

5. Turn off the computer.

Model I System Power-Up

These are the steps to power-up and power-down the Model I Hard Disk System. Please use these steps.

1. Make sure all floppy diskette drives are empty.

2. Turn on all peripheral equipment (such as printer and floppy diskette drives)

3. Turn on the primary hard drive by turning the POWER KEY clockwise. This also turns on all existing secondary drives. Wait for the power lights on all the secondary drives to come on.

4. Turn the Expansion Interface ON.

5. Turn the CPU/Keyboard ON. Wait until all floppy disk drive motors stop, then carefully insert the HARD DISK OPERATING SYSTEM INITIALIZATION diskette or the START-UP diskette in Drive 0.

   The START-UP diskette is a modified copy of your INITIALIZATION diskette created during initialization. Initialization procedures are described later in this supplement.

6. Press RESET. In a few seconds the screen shows a large LDOS logo.

   If the LDOS logo does not appear, repeat the above

steps, making sure you inserted the diskette properly.

7. At the bottom of the screen, LDOS asks you for the date. Type today's date in the mm/dd/yy form and press <ENTER>. For example, for June 17, 1982, type:

   06/17/82 <ENTER>

8. LDOS then displays the name and date of the diskette above the logo. It also displays the expanded date below the logo.

9. The screen then shows this prompt:

   LDOS Ready

   Since you've not yet initialized your Hard Disk System, your computer is now operating as a Floppy Disk System, the only way it can operate until you initialize it.

   If you have already initialized your Hard Disk System, you can remove the START-UP diskette (created during initialization). You only need it to start up or reset.

To operate the system for floppy disk only, hold down the <CLEAR> key and press the RESET button. (You must keep the <CLEAR> key down until LDOS Ready appears.)

Model I System Power-Down

1. The LDOS Ready prompt should be the last line on your screen. If not, press <ENTER> or exit your program so that it appears.

2. Remove all floppy diskettes from their drives.

3. Turn off any peripheral equipment.

4. Turn off the primary hard disk drive by turning the POWER KEY counterclockwise. This also turns off all existing secondary drives.

5. Turn off the Expansion Interface.

6. Turn off the CPU/Keyboard.

5/ Replacement Procedures

Replacement procedures contained in this manual are limited to case disassembly, removal and replacement of subassemblies, and case assembly.

Before beginning repair, disconnect all external cables from the rear connector panel.

Disassembly

1. Remove the top row of screws (3) from the rear panel and lift off the case.

2. To remove the hard disk controller board, remove all cables from the board (data cables, hard disk expansion cable, controller connecting cables, power harness, and lamp controller harness).

NOTE: At the time of disassembly, be sure that the nylon washer on center stand-off is saved for reassembly.

3. To remove the hard disk power supply, remove the 4 screws which secure the power supply mount-and-shield to the bottom of the unit and lift off the cover. Loosen all cables. Disconnect the power harness from the drive unit. Remove the six screws which hold the power supply board.

Reassembly

1. Fasten the power supply in the bottom of the unit by using 4 #6 screws and 2 #10 screws. Reconnect the power cables.

2. Replace the power supply shield-and-mount and fasten it using 4 #6 screws. Reconnect the power harness on drive. Position the clear insulating sheet on the power supply mount-and-shield.

3. Be sure and replace nylon washer between the hard disk controller board and center stand-off. Fasten the board

using five #6 screws.

4. Reconnect all cables, the lamp driver harness, and the power harness. (Make sure that the lamp driver harness is toward the rear of the unit.) Be sure that the data cables are connected so that the cable comes from the left-hand side of the plug when looking from the front of the unit.

5. Replace the case top and 3 #6 screws in the rear panel.

6/ Maintenance

The only regular maintenance the 5-Meg Disk Drive requires is a periodic cleaning of the filter on the back of the unit. Clean this filter whenever it becomes filled with dust and particles.

To clean the filter, carefully remove the outer grill -- DO NOT REMOVE THE SCREWS. Then remove the filter and rinse with tap water. When the filter is completely dry, put it back in the drive.

7/ Theory of Operation

Hard Disk Controller Board

General

The hard disk controller board is a discrete implementation of all functions required to control the 5.25 inch disk drive via a standard data and control bus. The controller is fabricated using a mix of high-speed bipolar and MNOS devices contained on a single two-sided PC board. The design of the circuitry makes use of a high-speed microcontroller, the 8X300, newly developed NMOS support devices, Schottky and low power Schottky devices. All I/O connections are made using standard ribbon cable connectors. Standard pin-out configurations for disk interface connectors permit direct pin-for-pin connections to the drives. All host to disk data transfers are buffered by onboard RAM to achieve totally asynchronous transfers to and from the disk by the host.

The disk controller is built around five basic sections:

Processor Functions

All functions of the controller are ultimately disciplined by the onboard processor. Due to the high data rates associated with hard disk drives, a processor capable of extremely fast execution speed is required for processing of data and controlling machine functions within the circuitry. The processor used is the 8X300, a bipolar micro-controller particularly well-suited for handling data efficiently at high rates.

The 8X300 operates at a basic clock rate of 8MHz and performs all operations within two clock cycles giving it a speed of 4 MIPSS (Million Instructions Per Second) or one instruction executed every 250 nanoseconds. The architecture of the processor is different from most popular microprocessors in that no common data or address bus is provided to be shared by RAM, ROM, or peripheral devices.

Instructions are fetched from ROM via a dedicated instruction address and data bus. The Instruction Address bus (IA0 - IA13) is capable of directly accessing 8K words of program storage, however, the controller uses only the first ten address lines, IA0 through IA9, limiting onboard program storage to 1K words.

Program data is input to the 8X300 (U30) on the Instruction Data bus (IA0 - IA130) which is capable of directly accessing 8K words of program storage; however, the controller uses only the first ten address lines, IA0 through IA9, limiting onboard program storage to 1K words.

Fast IO Select

An extension byte has been added onto the instruction data memory to provide port access decoding on an instruction-by-instruction basis. This "Fast IO Select" byte is not processed by the 8X300, but it is decoded by auxiliary hardware (U39, U44, U45) to provide eight read strobes and eight write strobes which route data to the various devices distributed along the interface vector bus.

The Fast IO byte is latched into a 6-bit latch (U39) trailing edge of MCLK to ensure that the data remains stable during the entire instruction. This data selects a read strobe and eight write strobes which route data to the various devices distributed along the interface vector bus.

The Fast IO byte is latched into a 6-bit latch (U39) trailing edge of MCLK to ensure that the data remains stable during the entire instructions. This data selects a read strobe and a write strobe through two 1-of-8 decoders (U44 and U45) which are alternately enabled by the WC* control strobe produced by the 8X300. THe read strobe decoder (U45) is always disqualified at the end of instructions by MCLK' (MCLK prime), a delayed copy of MCLK, to provide edges on read strobes during sequential read operations from various ports. This delay compensates for timing races through the Fast IO latch (U39) and the control signals.

Because each decoder has a unique input, it is possible to select any read port with any write port during each instruction. Data is transferred between the processor and its ports on a separate 8-bit bus called the IO bus. This bus is active low. It must be noted that this bus is in no way related to the instruction data bus and should be thought of as simply an 8-bit bidirectional IO bus of the 8X300. In fact, it has been renamed as IO0 - IO7 to reflect this distinction.

Internal Bus Control

Several bus control signals are produced by the 8X300 to identify and strobe the data on the IO bus. Write Control

(WC) is a signal which determines the direction of the data to and from peripherals. When WC is false (during the first half cycle), data is being input to the 8X300 from the IO bus. When WC is true (during the second half cycle, data is being output to the IO bus from the 8X300. Select Control (SC) becomes active during the second half cycle instead of WC if the IO bus contains an 8-bit IO address. the WC and SC signals are combined by a NOR gate (U33) to initiate all accesses from the 8X300 to any output port within one instruction instead of the normal 5-bit immediate moves provided for by the instruction set.

All instruction fetches occur late in the second cycle of the preceding instruction. This time is marked by the generation of a 65 ns (nominal) active high pulse called MCLK which occurs every instruction. MCLK is used to latch data prior to being input on the IO bus to ensure stability during reads. MCLK is also used to disqualify read strobes which would otherwise remain true into the second clock cycle of any instruction which does not write to a port.

There are two more bus control signals produced by the 8X300, Left Bank select (LB*) and Right Bank select (RB*). However, due to the implementation of the Fast IO Select logic, only RB*, which is used as the chief enable signal for U17 and U18, is needed.

Reset Circuit

The 8X300 is held reset for approximately 40 milliseconds after initial power-on. This is accomplished by an RC network (R42 and C52). After this power-up sequence, there are two ways to reset the processor, both of which are controlled by the host computer.

One method of resetting the processor is by resetting of the host (i.e., reset switch) which drives the signal HDMR* low. The other method of resetting the processor is by software control. This is accomplished by setting bit D4 of port C1 HEX. This latches the signal (SFTRESET) which in turn triggers a one-shot U76 to drive RESET* low. The one-shot duration is set for approximately 100 u sec pulse width. RESET* is used to clear the drive control latches U62 and U52 and the host interface WAIT* (U43).

Processor Power Supply

Power is supplied to the 8X300 from the +5 volt (Vcc) power bus. Due to the internal operation of the 8X300, an on-chip

voltage reference is provided to produce bias to an external pass transistor (Q2) which drops Vcc to the 8X300 to approximately +3 volts. All signals into and out of the 8X300 are internally level shifted to be TTL compatible.

Read and Write Ports

Throughout the circuit, output ports are formed by "D" type latches using write strobes (WR0 -WR7) to latch data into the ports. Reading of ports is universally accomplished by using read strobes (RD0, RD2, RD4 - RD6) that enable selected tri-state output devices on the I/O bus. Additionally, two read strobes are used to clock the host DRQ* and INTRQ* latches (U5) and one read strobe is left unused as a "dummy" port for glitch-free operation of the Fast IO port decoders.

Read/Write Memory

Since the 8X300 does not permit data to be saved or retrieved from dedicated program storage, RAM must be installed on the IO bus. RAM must be accessed just like other port accesses via the IO bus by IO instructions. To provide for addressing the RAM, three latch/counters (U26, U27, U28) are connected to the IO bus to receive and store addresses required to access the RAM (U17,U18).

RAM Addressing

The RAM address bus (RA0 - RA9) uniquely addresses one of 1024 memory locations. As each counter chip reaches a count of 0, it will set a borrow condition to the next higher counter which will be decremented at the end of the next access to RAM. When all bits of the address have been reset, the ROVF* bit on the last counter (U26) will be reset, providing overflow status which can be read by the processor on (U26). By setting various beginning address values, ROVF* can be used to mark the end of any RAM access loop from 1 to 1024 bytes in length. The controller board uses this function to set sector buffer lengths of 128, 256, or 512 bytes.

Sector Buffering

All data read from or written to the disk is passed through the RAM to provide buffering required for asynchronous data transfer between the host and disk. The counters are post-decremented, which means that the effective addresses are stable to the RAM by at least the instruction prior to

the actual access. This pre-selection feature effectively reduces RAM access time to the output enable and propagation time of the RAM for read operations. This feature also reduces the width of the minimum WR* strobe pulse for write operations.

RAM Accessing

RAM access is initiated by RCS* which is the logical or (by U59) of RDO* and WRO* which are generated by the Fast IO decoders (U44 and U45). Data to be read from RAM will be placed on the IO bus whenever RCS* is low and WC* is high. Data is written into a selected RAM cell on the trailing edge of WC* if RCS* is low. During writes, both WC* and RCS* will be low for at least 120 nanoseconds so that data setup time requirements are met.

Scratchpad Operations

Because the RAM address counters can be pre-set, direct reads and writes to a specific address are possible. This function is used for scratchpad storage during program execution. This mode of RAM access requires two or three instruction cycles for each random access to the RAM as opposed to one for sequential access using the post-decrement feature.

MAC Control Port

Basic control of the various functional sections of the controller is accomplished by a dedicated 6-bit control port called MAC CNTRL (U29). MAC CNTRL enables CRC generation (CRCIZ*), functions of the WAIT control circuitry (WAEN*), gating of read or write functions (WRITE*), control of CRC check word output (lBLA*), and AM detection (SRCH). MAC CNTRL output states are latched into the port by a write strobe (WR7). Additionally, any time MAC CNTRL is loaded with a new byte, the lower two data bits (IOO and IOI) are strobed into the upper two address counter/latch bits (RA8 and RA9). All remaining ports are distributed among the basic functional sections of the controller and will be described in detail within the discussion of those functions.

Serial Data Separation

The controller board contains circuitry which processes incoming MFM data from the drive by a method called data

separation. Here, some background information may be helpful:

> In order to provide maximum data recording density and therefore maximum storage efficiency, data is recorded on the disk using a Modified Frequency Modulation (MFM) technique. This technique requires clock bits to be recorded only when two successive data bits are missing in the serial data stream. This reduces the total number of bits required to record a given amount of information on the disk. This results in an effective doubling of the amount of the data capacity, hence the term "double density."

Because clock bits are not recorded with every data bit cell, circuitry that can remain in sync with data during the absence of clock bits is required. Synchronous decoding of MFM data streams requires the decoder circuitry to synthesize clock bits when they are present. This is accomplished by using a phase-locked oscillator employing an error amplifier/filter to sync onto and hold a specific phase relationship at the data and clock bits in the data stream. The synthesized clock called RCLK can then be used to separate data bits from clock bits and to shift the resultant serial data into registers for parallelization into bytes.

Incoming Data Selection

Serial data is input from up to four radially connected drives via a quad RS-422 differential receiver (U54). The receiver converts differential input data to TTL levels for use by the controller. The data from the selected drive is then routed to gate (U53). At this point, data and clocks are still combined and appear as 50 nanoseconds (nominal) active high pulses spaced at intervals of one, one and a half, or two times the RCLK period. This data is presented to the input of another AND/OR/INVERT gate (U4) which will gate either MFM data or a reference clock into the first stage of the VCO error amplifier circuitry.

Reference Clock

The reference clock is derived from the write clock crystal oscillator (Q1, U10, and associated circuitry). This oscillator uses a fundamental cut crystal to oscillate at four times the RCLK frequency. The 4X output is then divided by U10 to produce both a 2X clock (2XDR*), which is used as a reference, and a 1X clock (WCLK) which is used to produce

MFM write data for the disk. The crystal (Y1) frequency is 20.000 MHz for compatible drives.

Clock Gating

The gating of the reference and MFM data into the data separator is dependent upon the condition of the Read Gate signal (RGATE) and the spacing of the data on the serial stream after RGATE is brought true. Due to the techniques which are employed to separate data from clocks, it is necessary to run the VCO at a rate twice the data clock (RCLK) rate. The VCO is therefore set to an open-loop frequency of 2 times RCLK. Any variations in this rate due to variations in disk rotational speed must be compensated for by the VCO, but instantaneous shifts in data due to the effects of adjacent bit cells on the disk and minor noise must be ignored. Also, the response of the VCO must be adjusted to effectively ride over missing clock bits which occur as a result of MFM recoding technique. The resultant compromise between response and reject requirements of the VCO cause the VCO to have a tendency to become locked onto harmonics of the data rate rather easily. This is likely to occur if the VCO is connected to a data stream over a field of data which has data bits spaced at one and a half or two times the actual RCLK time intervals.

To provide protection against this undesirable condition, the VCO is always held locked onto a stable clock running at two times the RCLK frequency whenever the controller is not actually reading data. Furthermore, great care is taken to switch in read data to the VCO error detector only when it is known that the data stream frequency is equal to the RCLK frequency. This can occur only when the data is a solid stream of all ones or all zeros.

High Frequency Detector

The switching function is initiated immediately after RGATE goes true and will only switch read data into the VCO after 16 consecutive ones or zeros (high frequency) are detected by a one-shot (U1) and counter (U2) connected directly to the raw MFM data. The one-shot is adjusted for a pulse width of one and one-fourth times the RCLK period. This is 250 nanoseconds, +/- 10 ns. These adjustments of the DRUN one-shot (U1) provide tolerances of up to one-fourth the RCLK period in jitter on the MFM data bits while still being able to distinguish MFM zeros or ones from other data patterns.

Each clock or data bit on the serial stream triggers the one-shot. If the time between successive triggers is less than the one-shot time constant, the one-shot remains retriggered. As the one-shot is triggered by data stream bits, so is the up/down counter (U2) whose count mode is controlled by the state of the one-shot outputs. While the one-shot is being retriggered, the counter counts up. When any data bit fails to reach the one-shot before its time constant is over, the one-shot resets and in turn clears the counter. Only when 16 successive retriggers occur, can the counter reach its terminal count. At this time, the counter overflow goes true and sets the DRUN* latch output (U3, pin 6) low which switches read data in and reference clock out. An AND-OR-INVERT gate (U4) performs the switching. DRUN* is read through (U74) by the 8X300 to determine the condition of the MFM data stream.

VCO

The Hard Disk controller uses a single chip VCO (U32) which simplifies circuitry and adjustments. The operating point of the VCO is initially set by adjusting the variable capacitor (C33) for a 10 MHZ output at TP9 and the frequency control voltage input (TP8) to 2.5 V +/- .5 V. It should be noted here that both of these adjustments are done using the same trim cap (C33).

The output of the error amplifier and filter is fed to the VCO and represents how far the VCO frequency is from that of the incoming signal. The error signal, which is proportional to the difference, allows the VCO to shift from center frequency and become the same as the frequency of the frequency of the input signal. When the loop is in lock, the difference frequency component will be DC and is passed by the low pass filter.

Frequency control is actually a matter of frequency range. The difference component may fall outside of the band edge of the low-pass filter and be removed along with the sum frequency component. If this is the case, then no information is transmitted around the loop and the VCO remains at its initial free running frequency. As the input frequency approaches that of the VCO, the frequency of the difference component decreases and approaches the band edge of the filter. Now part of this difference component is passed which tends to drive the VCO to the frequency of the difference component more and allows more of it to be passed through the filter. This is a positive feedback, which causes the VCO to snap into "lock" with the input signal.

The term "capture range" can be described as the frequency range centered about the VCO free running frequency over which the loop can acquire lock with the incoming data signal.

The free running frequency of the VCO is always twice that of the RCLK rate. In fact, RCLK is produced by the VCO through a divide-by-two counter (U14).

Power for the VCO's internal oscillator as well as for the error amplification filter is supplied from a 78M05 +5 volt regulator. This insures good noise separation for these stages from the power supply.

Error Amplifier

Control of the VCO is accomplished by the error amplifier, filter, and Data Separator chip. The error amplifier is a balanced current mirror whose output sources or sinks current to the filter stage. Whenever the VCO is running too slow, the error amplifier receives pulses from data bits before pulses from the VCO clock. This causes the error amplifier to produce pump-up pulses to the filter. The filter integrates these UP pulses and raises the overall voltage of the voltage control input (TP8) to the VCO. When the VCO is running too fast, the error amplifier produces pump-down pulses to the filter. There will always be some error present because without pulses of UP and DN the filter would float causing the VCO to drift off center frequency.

Phase Detector

The circuitry which feeds the error amplifier is called the phase detector. This consists of several "D" latches (U20, U21) and a delay line (U31). The function of this circuit is to provide time windows during which the leading edges of the incoming MFM data can be compared to the leading edges of the VCO clock. These windows are approximately 50 nanoseconds in length and are initiated by the leading edge of any data bit as it enters the detector. The windows are terminated by the same data bit, edge delayed by a net of 50 nanoseconds (60 nanoseconds in the delay line minus approximately 10 nanoseconds in propagation delays.) When both the delayed data bit and the nearest VCO clock edge arrive at the detector, the detector is reset until the next data bit arrives on the MFM data stream. The delayed data bit sets its half of the detector latches to produce the VP

pulses. The VCO clock edge sets its half of the detector to produce the DN pulse.

Window Extension

Once the VCO has been locked onto the phase of the incoming data, the actual separation of data and clocks can occur. This is accomplished by using a technique called window extension. This technique causes data bits to first have their leading edges shifted into the center of the RCLK half cycles then to have them latched or extended until the next rising edge of the RCLK. The shift is accomplished by tapping the data of the Sample on Phase Detector delay line at the 60 nanosecond tap, and inverting the VCO clock to the RCLK divider (U14). The delayed data clocks a pair of latches (U12 and U13). The "data" latch has its "D" input and CLEAR connected to RCLK* and the "clock" latch has its "D" input and CLEAR connected to RCLK*.

If an MFM data bit enters the latches while RCLK is high, it will be extended as a data bit. If RCLK* is high, it will be extended as a clock bit. Due to this extension technique, bits can jitter approximately one-fourth the RCLK period without being lost. The output of each latch is then further extended by being fed directly into the second half of the latches and clocked on alternate edges of RCLK. The final outputs of the data extension/separation stage are two separate signals; one signal consists solely of NRZ (non-return to zero) data and the other of NRZ (non-return to zero) clocks. The NRZ data and clocks are finally in a form suitable for processing by subsequent circuitry on the Controller board.

Clock Detection

Due to the nature of MFM data encoding, it is impossible to know exactly if MFM bits are data or clocks. This ambiguity results in having to create circuitry to assume that bits on RCLK* are actually data bits until the VCO is locked on and a unique data/clock pattern is detected. This is accomplished by holding the VCO to RCLK divider (U14) reset until it is fairly certain that bits on the data stream are actually clocks belonging to a field of zero data.

Once this assessment has been made, the processor releases the AM detector (U11) by raising the SRCH signal. This signal releases a latch (U11) which will remove DHOLD from the RCLK divider (U11) on the next rising edge of a MFM data

bit so that CLOCKS will be on the RCLK* phase and DATA will be on the RCLK phase. The processor makes its assessment of the state of the data stream solely on the occurrence of a significant run of zeros which is detected by the one-shot (U1) in the DRUN circuit. Once released, the phase of RCLK vs. data and clocks will remain stable throughout the read of an ID field or data field. Whenever SRCH is dropped, the VCO to RCLK divider is once again reset and no RCLKS are produced.

Data Conversion and Checking

MFM data which has been separated to form NRZ data and clocks is processed through specialized circuitry to prepare it for parallel processing by the 8X300. This processing consists of three functional circuits.

1. AM detection (U11)
2. Serial-to-Parallel conversion (U9)
3. CRC checking circuit (U6)

Each function will be discussed separately but bear in mind that many interdependencies exist.

AM Detection

As previously stated, it is impossible to know whether serial data bits are actually data or clock bits by just looking at the data stream. Furthermore, it is equally impossible to determine byte boundaries. The problem is solved by a uniquely recorded data/clock pattern called an Address Mark (AM). The AM consists of a data pattern of HEX 'A1' with a missing clock pattern of HEX '0A'. Normally a data byte of of HEX 'A1' requires a clocking pattern of HEX '0E'. In fact, due to the rules of MFM data encoding, an alternating clock pattern such as HEX 'A' or HEX '5' cannot exist legally.

The AM is used to uniquely identify the start of a field of information (data or ID field) within each sector. A long run of zero data always precedes each AM on the disk. Zeros have a clock bit for every RCLK. When attempting to read information from the disk, the Controller first acquires phase lock over a field of zeros. When this acquisition is achieved, the processor releases the AM detector (U11) by raising the Search control line (SRCH) on the MAC CNTRL port (U29).

Due to the circuitry associated with the VCO to RCLK divider, the RDAT* output of the data separator (U13 - 8) will be high and the CLKS* output (U12 - 8) will be low. RCLK* will be the shifting clock for RDAT* and RCLK will be the shifting clock for CLKS*. These four signals are routed into the AM detector. Inside the AM detector, RDAT* is shifted into an 8-bit synchronous serial shift register and clocked on the falling edge of RCLK*. CLKS* is shifted into a similar shift register on the falling edge of RCLK. The output stage of the RDAT* register is dumped into an 'A1' comparator and the output stage of the CLKS* register is dumped into a '0A' comparator. AM detection occurs when both detectors are true, thereby setting the AMDET* latch. At the instant AM occurs, the exact relationship between data and clocks is known. It is also known that data is being clocked by RCLK* so CLKS* can actually be discarded; their purpose was in detecting AM. The AMDET* signal is used as a synchronization signal to start subsequent conversion circuitry. The AMDET* signal remains true until the processor again de-asserts the Search control line.

Serial to Parallel Conversion

After an AM has been detected, the serial-to-parallel convertor (U9) takes over. NRZ data and RCLK are used to shift data bits into an 8-bit serial-to-parallel shift register. As each bit is shifted, a divide-by-8 counter circuit is incremented. After every eighth bit of data is shifted, the counter produces an overflow pulse marking byte boundaries in the serial data stream. The overflow bit from the counter resets the counter, clocks the data from the shift register into an 8-bit parallel latch, and sets a tri-state flag register called BDONE. The flag can be read by the processor to see if any converted data is ready to be read from the latches.

When the processor sees BDONE in the true state, it services the device by gating data onto the IO bus using read strobe 4 (RD4*) in conjunction with a tri-state buffer (U8). The act of reading the latches also clears off the pending BDONE flag. As successive bytes are processed, the BDONE is serviced by the processor as data becomes available.

Outputs from the serial-to-parallel device also include SHFTCLK* and DOUT. SHFTCLK* is actually RCLK* propagated through the device. DOUT is the Q output of the last stage of the shift register string. DOUT and SHFTCLK* are routed to the CRC generator checker device and also are tri-stated

along with BDONE. These signals are active only when WRITE* is high which indicates a read mode of operation.

CRC Checking Circuit

Data recorded on magnetic media is prone to several types of errors which could render data unusable if some form of error detection were not employed. Therefore, a cyclic redundancy check (CRC) is performed on all data transfers from the disk. The CRC is an error detection code consisting of 16 additional bits which are appended to every ID field and data field on the disk. These bits are produced by dividing the data stream serially with a large polynomial. This division produces a unique 16-bit value for any information passed through the CRC generator.

As data is being read from the disk, the CRC generator (U6) re-computes the original CRC bits. The value in the CRC generator must always be zero after the last two bytes (which contain the orginal recorded CRC) are read. When this happens, the data was correctly read and the controller will not flag an error. If, however, the CRC generator is not zeroed after it has checked all bytes of the recorded data, the controller will flag the data as erroneous and enter into a re-try condition. If the controller cannot get correct data after attempting to read it 16 times, the read will be aborted and the host informed that the data in the buffer is questionable.

The Controller board uses the same device to generate and check CRC's for data being written to or read from the disk. The polynomial used is:

$$X^{16} + X^{12} + X^{5} + 1$$ (commonly called the CRC-CCITT polynomial)

The processor polls the condition of the DRUN circuitry during read operations. When DRUN is true, it begins to search for an address mark. Once the AM is located, the processor will start to read parallel data which has been converted from NRZ data by the serial-to-parallel device. The processor will terminate this activity when it has received the information it is looking for or if an error is detected.

While the processor is reading the parallel data, the CRC generator is reconstructing the CRC check value. The CRC generator is initialized by the processor setting CRCIZ* low

for at least 250 nanoseconds during the search for the AM. CRCIZ* is originated on the MAC CNTRL port (U29). Upon receiving the CRCIZ* signal, the CRC generator/checker will preset all 16 of its internal polynomial division shift registers to logic ones and arm an internal latch which will enable the checking function on the leading edge of the first non-zero data to enter the device. It should be remembered that prior to an AM there is always a field of zeros (all data bits low) so the first non-zero data bit into the device will always be the most significant bit of the AM (HEX A1).

The CRC device, when enabled by the first non-zero data bit, will shift succeeding data bits into a feedback shift register string with Exclusive or gates tied to the feedback nodes on the first, fifth, twelfth, and sixteenth registers. As each RCLK occurs, the registers will divide the incoming data and a unique pattern of ones and zeros will appear across the registers.

When the last bit of an ID or data field is processed, the pattern in the registers should be equivalent to the 16 bits appended to the fields during original recording. The appended bits are also entered into the CRC device. If all of the bits in the appended field are identical to the bits in the registers, then the Exclusive-or-Gates in the register string will have flipped all of the ones to zeros and the CRC will have been satisfied.

The output of each register stage is tied to a 16-bit comparator which goes true when all of its inputs are zeros. The output of the comparator is retimed to remove any decoding slivers and is output as CRCOK. The processor can read CRCOK through U61 to see if a CRC error has occurred.

After the CRC bits are processed, the data stream will contain at least one more byte of zeros. It is the nature of the CRC polynomial that if no bits are set to ones in the registers and if a constant input of zeros is shifted into the registers, no bits will be flipped. This provides a convenient latching function for the CRCOK flag which will remain true for at least one byte after the last CRC check byte, giving the processor time to read the flag.

The data, clock, and BDONE are supplied to the CRC device on a 3-bit mini bus. During read operations, the serial-to-parallel device (U9) will be sourcing these lines since the WRITE control line from MAC CNTRL (U29) is low and this enables tri-state drivers on these lines. The

Parallel-to-Serial device (U7) will have its tri-state drivers disabled.

Serial Data Generation

The Controller records data on the disk in MFM format. In order to produce the proper data format, the Controller uses several specialized devices to process the parallel data supplied by the host into a serial MFM data stream. The data supplied by the host is temporarily stored in the buffer RAM until the correct sector is located for the data to be written.

The process of writing is essentially the opposite of reading except that the data separator circuitry is not required and the generation of the MFM data stream is produced by synchronous clocking techniques.

The functional sections of the serial data generation section are listed below:

1. Parallel-to-Serial conversion (U7)
2. CRC generation (U6)
3. MFM and precompensation (U5)

Parallel to Serial Conversion

Parallel data is converted into a serial NRZ data stream by the parallel-to-serial device (U7). The processor enables this conversion by lowering the WRITE* signal on MAC CNTRL (U29). WRITE* causes the tri-state buffers present on the parallel-to-serial device to become active, supplying the CRC device with data, clocks, and BDONE strobes.

The processor presents parallel data on the IO bus along with the WR4* write strobe which latches the data into the parallel port on the BDONE. Inside the parallel-to-serial device, the parallel latches are loaded into a serial shift register on every eighth WCLK transition. As the data is transferred to the shift registers, the BDONE status flag is set. The processor reads this flag through U61 to determine when to write the next parallel byte to the device. The timing of the parallel accesses is at a rate one-eighth that the bit rate of the NRZ data stream.

The output of the last register in the shift string is brought out of the device as a NRZ serial data stream. The shifting clock is also brought out as SHFTCLK to be used as the clock for the CRC device.

Whenever it is desired to write a repetitive string of identical data bytes, the processor can simply ignore the BDONE flag and permit the device to reload the data from its latches over and over again for as long as required to generate the field. This feature of the device is used in writing certain fields used in formatting.

CRC Generation

The CRC generator/checker (U6) is used to generate the CRC bits and to append them to the end of the data being written to the disk. This is the complementary function to that performed during reads. The operation of the polynomial generator is identical to read operations except that at the end of the data field, the processor sets a signal which causes the device to output the computed CRC after the data instead of reading the CRC and checking it.

The initial state of the shift registers within the device is forced to all ones by the processor pulsing CRCIZ* for approximately 250 nanoseconds while the parallel-to-serial device is outputting all zeros on the NRZ data line. At that time, a latch is set which holds the registers at ones until the first non-zero bit enters the device. The first non-zero bit will be the MSB of the AM (HEX A1) of the data field to be written. When the processor decides that enough zeros have been written to satisfy the sync field requirements, it will store a HEX A1 in the parallel-to-serial device. At the proper time (in sync with BDONE) the parallel-to-serial device will begin to send the MSB of the AM to the CRC device. This will start the CRC polynomial generator and the CRC will be computed.

As the processor writes the last byte of data to the parallel-to-serial device, it will drop the 1BLA* (1 Byte Look Ahead) signal on MAC CNTRL port (U29). This signal will cause the CRC generator (U6) to begin dumping the computed CRC onto the NRZ data stream at the conclusion of the last data byte (synchronized with the BDONE signal). In this fashion, the device is able to append the proper CRC information to the end of a field of data. 1BLA* is maintained at a low state for the duration of the unloading process which lasts for 16 bit times.

During the unloading process, the CRC registers back-fill with zeros. This feature is handy because by leaving 1BLA* low; for additional time, zeros will always be written after the CRC which is a requirement for the proper operation of

the CRC device during read operations. The NRZ data with CRC appended is then sent to the MFM generator device (U5).

MFM Generation

The conversion from NRZ write data to MFM write data takes place in the MFM/Precompensation device (U5). This device accepts NRZ data and a complimentary WCLK and produces MFM data and clocks by sending the data through circuitry which decides when and where to write clocks on the data stream under the MFM encoding rules. The proper encoding of the data into MFM requires the device to apply three rules to the data.

1. If the current data cell contains a data bit, no clock bit will be generated.

2. If the previous data cell contained a data bit, no clock bit will be generated.

3. If the previous data cell and the present data cell are vacant, a clock bit will be produced in the current clock cell.

The terms "data cell" and "clock cell" are defined by the state of WCLK. While WCLK is low, it is a data cell and while high, it is a clock cell. It can be seen then that both clock and data cells are one-half the period of WCLK or 100 nanoseconds. Also note that by the rules started above, a clock and data bit can never occur within the same WCLK period and legal spacings for bits can be one, one and a half, or two times the WCLK period only. The rules are implemented within the device by shift registers that hold the next two, last, and present data bits and combinational logic. The state of WCLK is considered and the appropriate bit cells are filled and combined on the MFMW output line of the device. This line is subject to decoding slivers, so it is run through a re-timing latch (U16) to clean it up.

Write Precompensation

The MFM data stream is now totally compatible with the recording rules and may be sent to suitable line drivers for transmission to the drive except for one modification. Due to the decreasing radius on the physical surface of the disk, the inside tracks have less circumference and therefore exhibit an increase in recording flux density over the outside tracks. This increase in flux density aggravates a problem in magnetic recording known as dynamic bit shift.

Dynamic bit shift occurs as the result of one bit on the disk (a flux reversal) influencing an adjacent bit. The effect is to shift the leading edge of both bits closer together or further apart than recorded. The net result is that enough jitter is added to the data recorded on the inside tracks to make them harder to recover without error. In any event, there is a method called write precompensation which can be applied to reduce the effect of this shift on the data.

Write Precompensation is a way of predicting which direction a particular bit will be shifted and intentionally writing that bit out of position in the opposite direction to the expected shift. This is done by examining the next two data bits, the last bits, and the present bits to be written and producing three signals depending on what these bits are. The three signals are EARLY, LATE, and NOM. They are used in conjunction with a delay line to cause the leading edge of a data/clock bit to be written early, late, or on time. As with MFMW, these signals are subject to decoding slivers and must be retimed by U16.

The processor can enable or disable the generation of these signals by controlling the RWC (Reduce Write Current) line from U52. When RWC is high, precompensation is in effect. When RWC is low, no precompensation is generated and the NOM output of the device is held true.

The delay line, U31, actually performs the precompensation with the help of an AND-OR-INVERT gate (U37). The MFMW pulses are applied to the input of the delay line and, depending on which of the three precompensation signals is present, the U37 selects a different tap on the delay line. Nominal data is actually tapped from the second tap, early data from the first, and late data from the third. From U37, the MFMW data is sent to the input of a quad driver (U35 or U36) where it is converted to a differential form and then sent to the disk drive. The AND-OR-INVERT gate (U37) has one other function. If the controller is not writing, the WGI (Write Gate Internal) signal will be low. This is inverted by U19 and applied to the fourth section of U37. This resulting high input effectively inhibits the gate from accepting MFMW data.

Host Interface

The interface bus to the controller is pin-for-pin compatible with the standard Model III I/O port. This

includes an 8-bit bidirectional data bus (U70) and 8 address lines (U71). For systems using interrupts and/or DMA, the controller also provides Interrupt Request (HDBINTRQ*) and Data Request (HDBDRQ*).

Accessing the controller is like other I/O devices. Address decoding is done on the controller board by U69. This decode can be jumpered to recognize four different address ranges. Standard setting is jumpered from 17 to 19, which utilizes port locations C0 to CF HEX. Further decoding to allow access of specific ports is done by U66, U67, and U68. Data bus direction is determined by U56, using standard bus as well as decoded signals.

Wait Enable

The generation of the WAIT* signal is controlled by a bit in the MAC latch (U29) called Wait Enable (WAEN*). If the controller is ready to accept random access to its task file, WAEN* will be asserted. After WAEN* is clocked through a latch (U43) to insure WAIT* is not asserted during a bus access in progress, DCRCS* (BIC or BOC in some applications) causes WAIT* to be asserted to the bus.

The WAIT* line is released on the trailing edge of any Read or Write Strobe to the communications latch, U60. This release is caused by the logical OR of RDG* and WRG* on U38 which presets the wait latch, U43, to a non-wait request condition.

Interrupts and DRQ's

The controller produces INTRQ* to signal the end of all disk operations and DRQ's to signal data ready to DMA controllers. INTRQ* and DRQ* originate on the MFM generator (U5) as an auxiliary function of that chip. The INTRQ* signal is set using INTCLK and the the DRQ signal is set using DRQCLK, both of which are produced by U44. Interrupts are cleared by CSAC'* (a 200 nanosecond version of the CSAC signal) and A0, A1 whenever the host reads the status register, issues a command or accesses the sector number register. Data requests (DRQ's) are cleared when the host accesses the data or cylinder low registers DRQ's will be reissued for each byte to be transferred. During power on or Master Resets (MR*), INTRQ* is set and DRQ is reset.

8/ Troubleshooting the Power Supply (Secondary Drive Only)

Section 1

Equipment for Test Set-Up

1. Isolation Transformer (minimum of 500 VA rating)-

CAUTION

Dangerously high voltages are present in this power supply. For the safety of the individual doing the testing, please use an isolation transformer. The 500 VA rating is needed to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC waveform.

2. 0-140 Variable Transformer (Variac)-
   Used to vary input voltage. Recommend 10 Amp, 1.4 KVA rating minimum.

3. Voltmeter-
   Needed to measure DC voltages to 50 VDC and AC voltages to 200 VAC. Recommend two digital multimeters.

4. Oscilloscope-
   Need X10 and X100 probes.

5. Load Board with Connectors-
   See Table 1 for values of loads required. The entry on the table for Safe Load Power is the minimum power ratings for the load resistors used.

6. Ohmmeter

Set-Up Procedure

Set-up as shown in Figure 8. You will want to monitor the input voltage and the output voltage of the regulated bus, which is the +5 output, with DVM's. Also monitor the +5 output with the oscilloscope using 50mv/div sensitivity. The DVM monitoring the +5 output can also be used to check the other outputs. See text of Section III for test points within power supply.

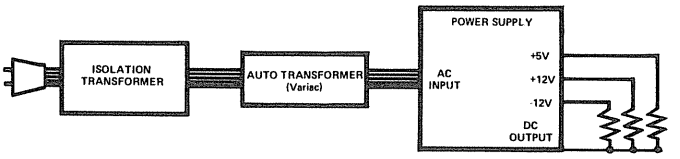


Figure 8. Test Set-Up

Section II

Visual Inspection

Check power supply for any broken, burned, or obviously damaged components. Visually check fuse resistor, if any question check with ohmmeter.

LOAD BOARD VALUES

OUTPUT	MIN LOAD	LOAD R	SAFE LOAD POWER	MAX LOAD	LOAD R	SAFE LOAD POWER
+5	0.45A	11.11 ohm	5W	2.5A	2 ohm	25W
+12	1.3A	0.40 ohm	8W	2.02A	24.24 ohm	50W
-12	0	0	0	0	120 ohm	2W

Table 1. Load Board Values

Start-Up

Load power supply with minimum load as specified om Table 1. Bring power up slowly with Variable Transformer while monitoring +5 output with scope and DVM. Supply should start with approximately 40-60 VAC applied and should regulate when 95 VAC is reached. If output has reached +5 volts, do a

performance test as shown in Section IV. If there is no output, refer to Section III.

Section III

NO OUTPUT

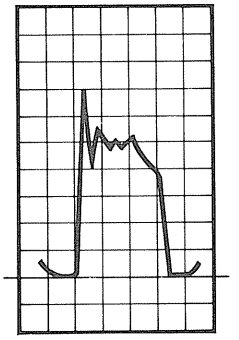
A. Check Fusable Resistor
If fusable resistor is blown, replace it, but do not apply power until cause of failure is found.

B. Preliminary Check on Major Primary Components
Check diode bridge (BR1), power transistor (T2), and catch diode (D3) for shorted junctions. If any component is founded shorted, replace it.

C. Primary Check on Major Secondary Components.
Using ohmmeter from output commmon to each output, with output loads disconnected, check for shorted rectifiers or capacitors. If +5 output is shorted, also check crowbar SCR (SCR1) and zener (Z1).

D. Check for B+
Set power supply and attach X100 scope probe ground to end of R10 nearest DB1. Slowly turn up power and check for B+ on end of R9 nearest mounting hole. With input at 95 VAC, this point should be between 120-140 VDC. If this is not correct, check BR1 and if necessary, check R21, D2, and finally input capacitors C5 and C6.

E. Check Q2 Waveforms
Using X100 probe on heatsink of Q2, check collector waveform. The collector of Q2 is the pin closest to the large capacitors C5 and C6. Transistor should be switching, correct waveform is shown in Figure 12. If this is not present, check for shorted junction on Q2. If OK check the base waveform. Base of Q2 is pin of transistor nearest the edge of PCB. The correct waveform is shown in Figure 12. If this waveform is not present, check L2, Q1, and D1, and secondary components Q3, D8, D9, D10, and L3. If any of the semiconductors are found shorted, or inductors open, replace them.



50 V/DIV
5 μsec/DIV

Input – 120VAC
Loads – +5 @ 2A
+12 @ 1A
-12 @ 0.1A

Figure 9. Q2 Collector Waveform

1.0 V/DIV
5 μsec/DIV

Input and Loads
same as above.

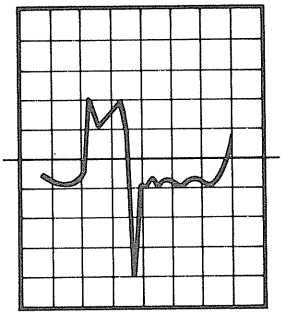


Figure 10. Q2 Base Waveform

Section IV

Performance Test

Each of these test conditions should be set-up and noted to be within the limits.

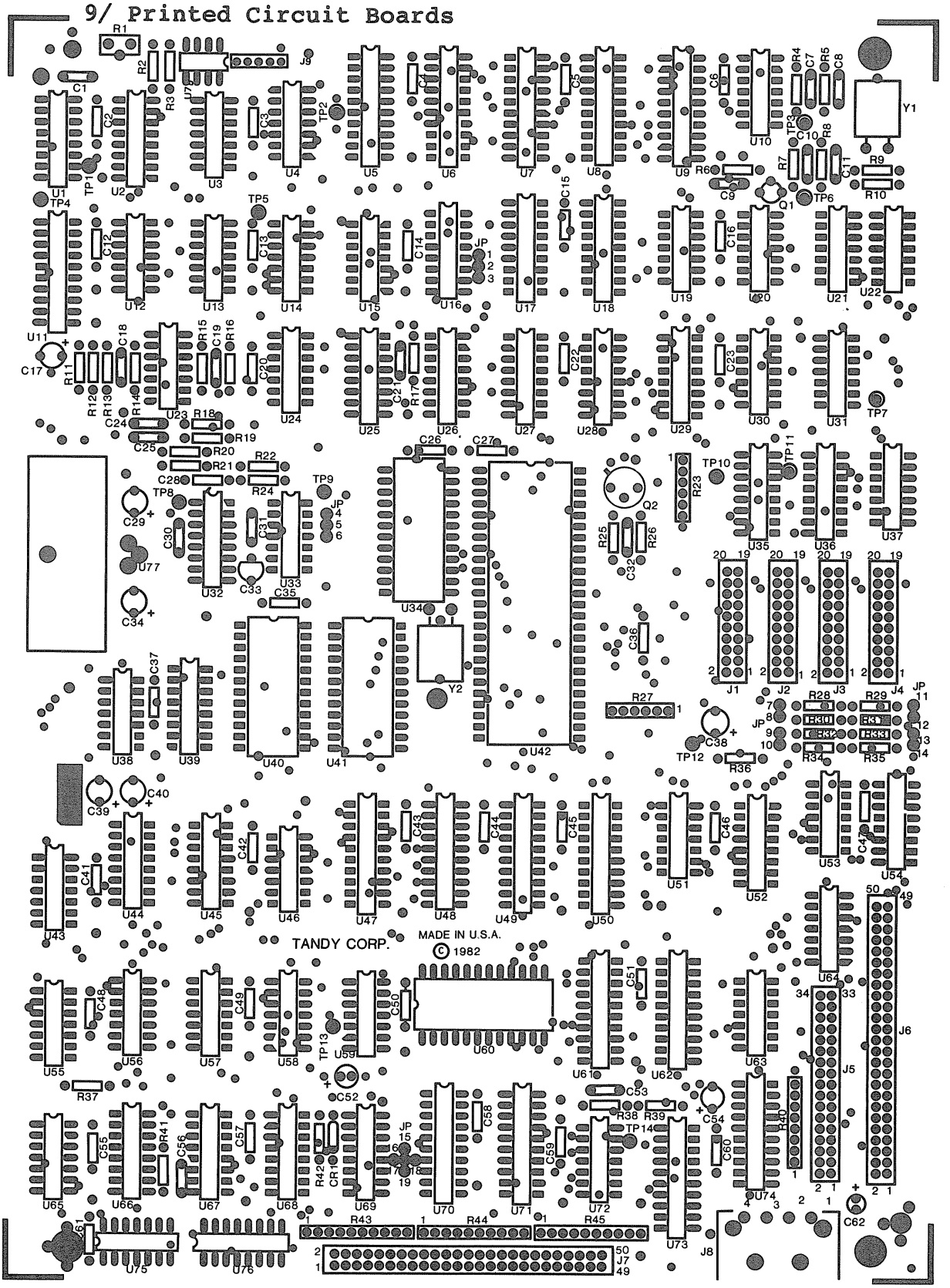
Test	Input	+5 Load	+12 Load	-12 Load
1	95VAC	Max	Max	Max
2	128VAC	Max	Max	Max
3	120VAC	Max	Min	Min
4	128VAC	Min	Min	Min
5	95VAC	Min	Min	Min

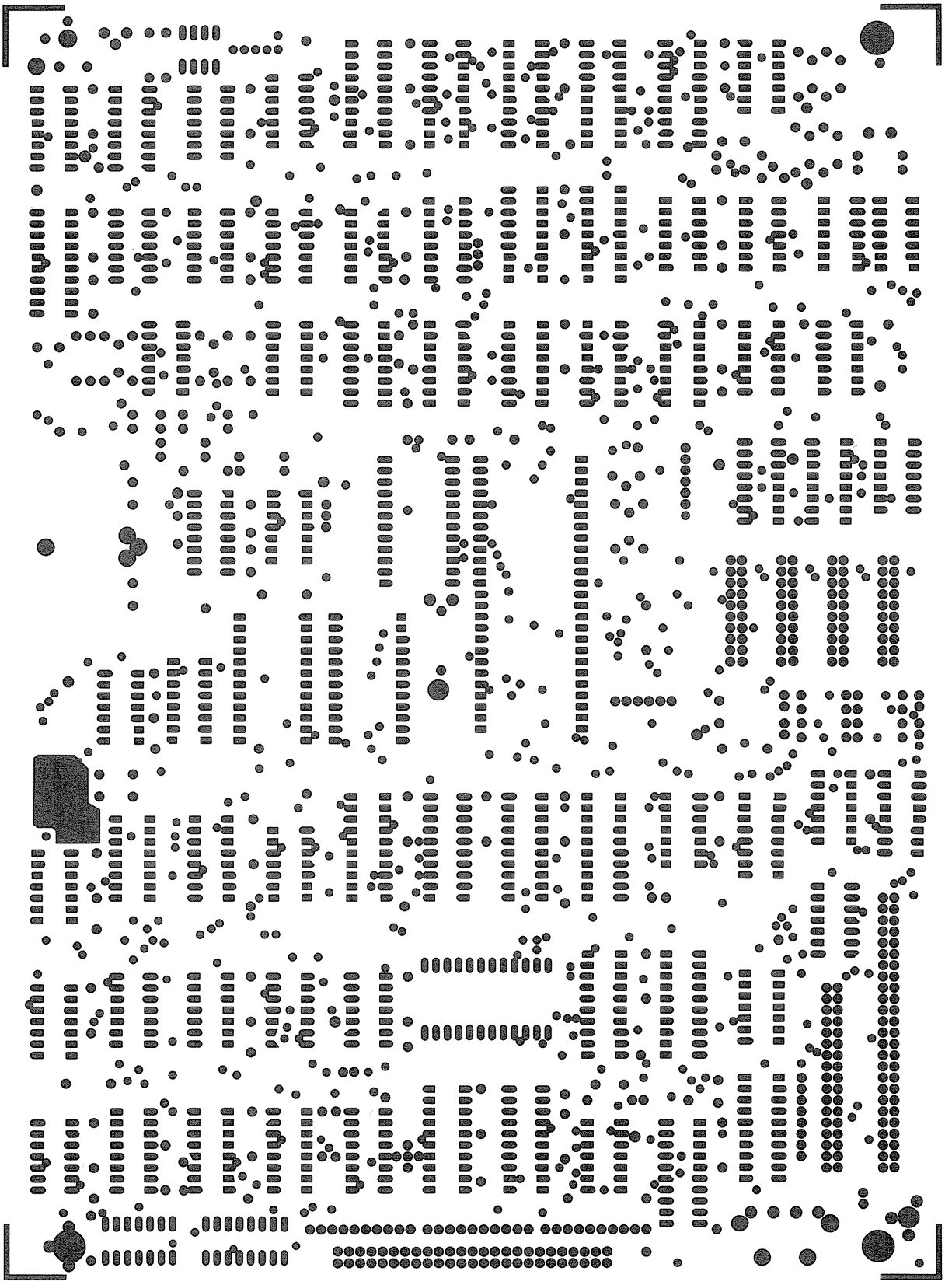
VOLTAGE AND RIPPLE SPECIFICATION

OUTPUT	MIN	MAX	NO LOAD	RIPPLE
+5	4.75V	5.25V		50mV P-P
+12	11.40V	12.60V		150mV P-P
-12	11.00V	15.00V		150mV P-P

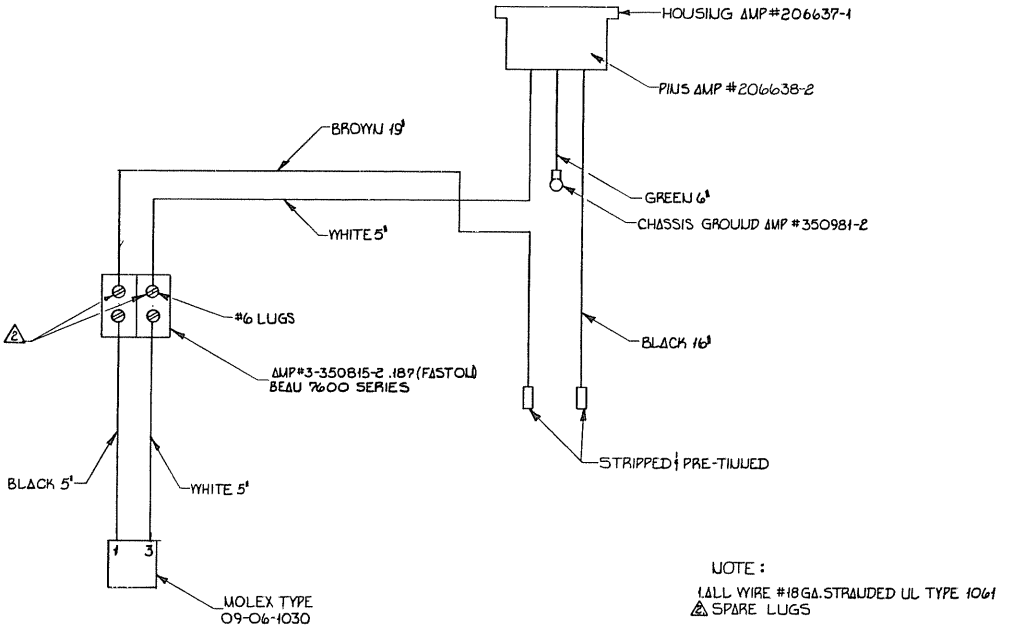
* Applies to resistive load only. Not under system operating conditions.

9/ Printed Circuit Boards

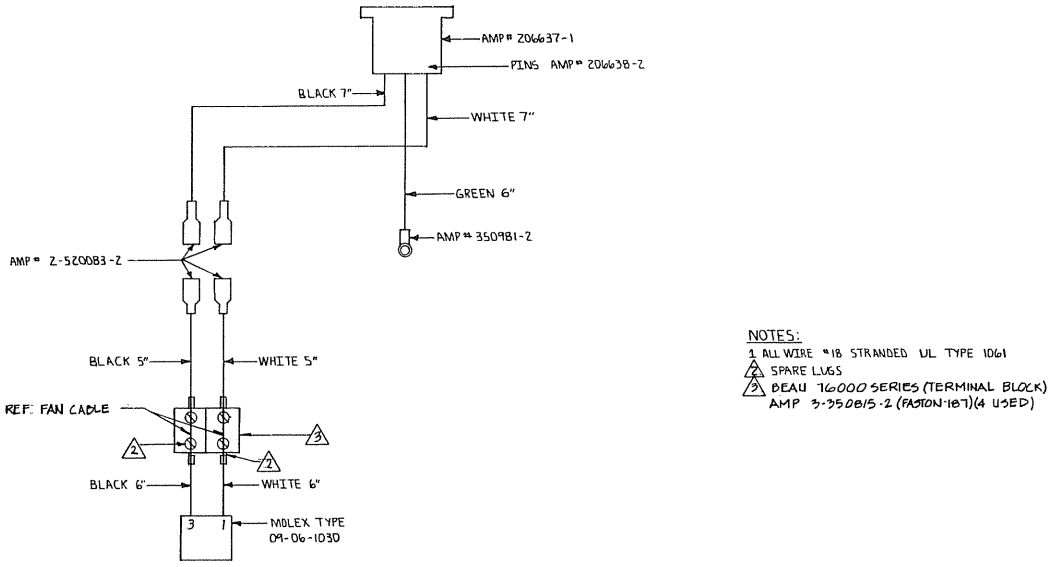




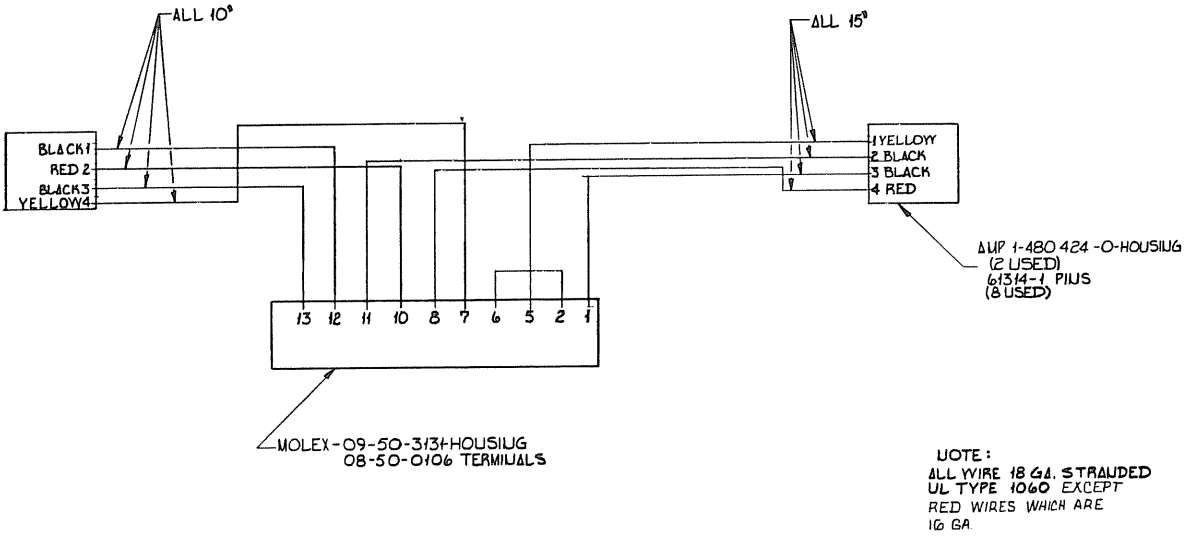
10/ Wiring Diagrams



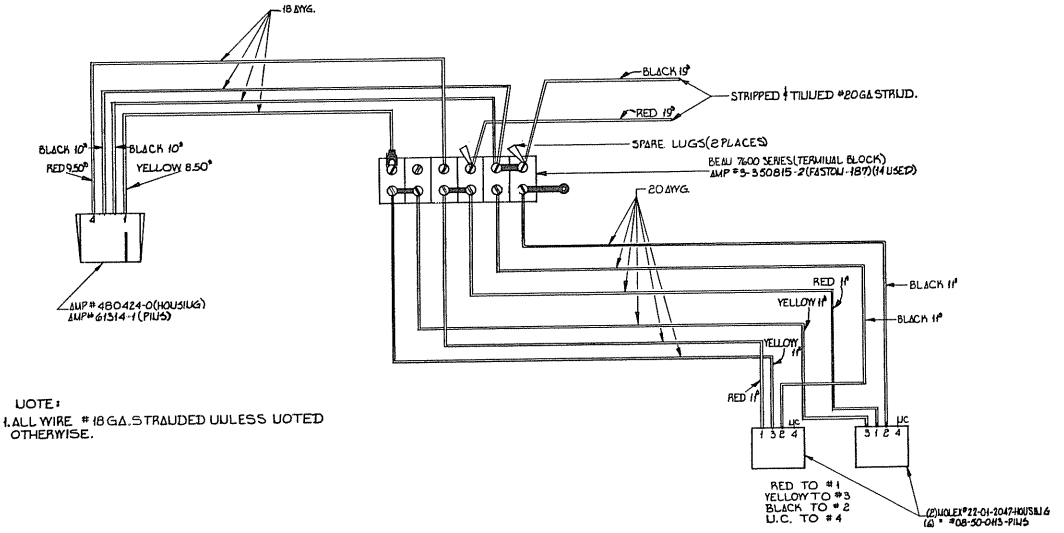
AC Wiring Harness (Primary/Master)



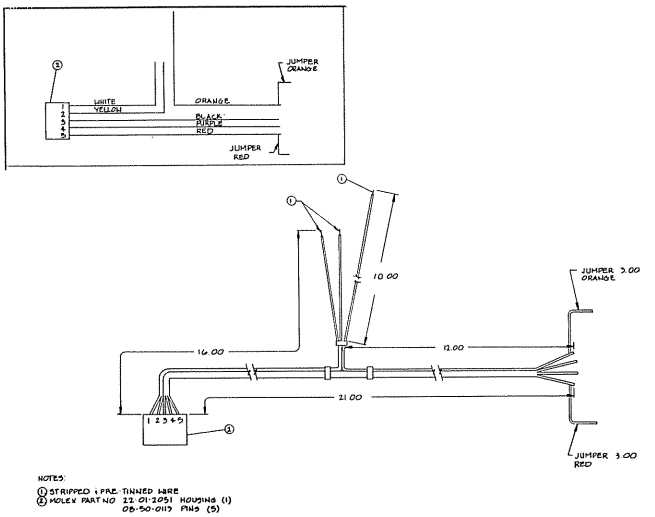
AC Wiring Harness (Secondary/Slave)



DC Power Harness (Primary/Master)



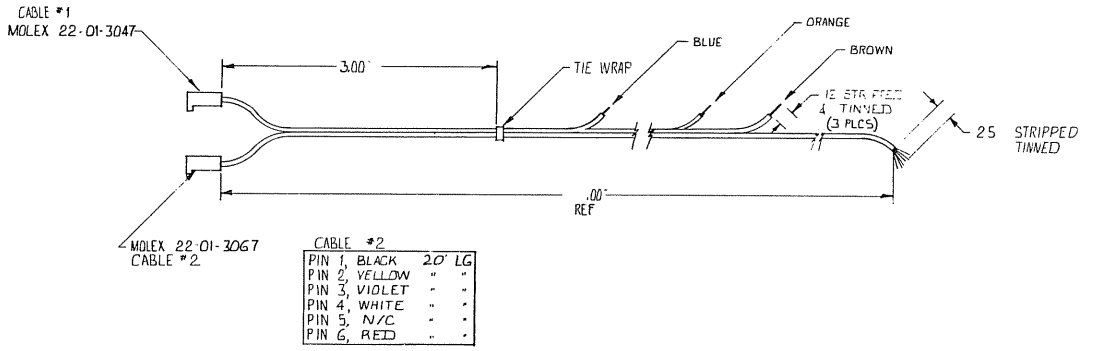
DC Power Harness (Secondary/Slave)



Lamp Driver Wiring Harness (Primary)

CABLE #1

PIN 1,	BLUE	10
PIN 2,	N/C	
PIN 3,	ORANGE	14
PIN 4,	BROWN	15



CABLE #2

PIN 1,	BLACK	20" LG
PIN 2,	YELLOW	" "
PIN 3,	VIOLET	" "
PIN 4,	WHITE	" "
PIN 5,	N/C	" "
PIN 6,	RED	" "

LED Driver Board Harness (Secondary)

11/ Parts Lists

PRODUCT DESCRIPTION
HARD DISK 5 1/4"
CAT. NO. 26-1130

QTY	DESCRIPTION	PART NUMBER
1	MANUAL, START-UP	8749389
1	REFERENCE, MANUAL	8749394
1	ADDENDUM	8759191
1	BINDER, MANUAL	8754082
1	SPLINE, INSERT	8789785
1	DISKETTE, SYSTEM 5M F/A	8896621
1	DISKETTE, BOOT 5M F/A	8896907
1	HOLDER, VINYL 5 1/4 DISKETTE	8719082
1	CARD, SOFTWARE REG	8759177
1	MANUAL ASSY	8896613
1	LABEL, TOP H.D. CONN	8789613
1	CORD, 8' POWER*	8709057
1	CABLE, EXT	8709341
1	BAG, 4 1/2 X 4 X 2 MIL(KEY)	8590056
1	BOX, ACCESSORIES	8769164
1	LABEL, ACCESSORY	8789817
1	KIT, ACCESSORY HDM	8896612
1	CASE, BOTTOM*	8729124
1	PLUG, 2 1/2" DIA.	8729148
1	LABEL, FCC PART 15	8789287
1	LABEL, FCC ID HDM	8789772
1	LABEL, S/N 26-1130	8789775
4	FOOT	8590123
4	WASHER, 1/2 O.D	8589074
4	FASTENER, #10 X 1/2"*	8569062
3	PLATE, COVER	8729147
6	SCREW, #4X1/4 PPH	8569120
1	CABLE, INT. CNTRL	8709330
1	CABLE, INT.CNTRLR	8709331
2	SCREW, #6 X 5/16	8569130
2	SCREW, #4-40 X 3/4"PPH	8569059
2	NUT, LOCK #4-40	8579003
2	WASHER, STAR #4	8589075

1	HARNESS, AC MSTR	8709332
1	SCREW, #6-32 X 1/4 (GRD)	8569098
2	SCREW, #4-40 X 1/2"PPH	8569033
2	NUT, LOCK #4-40	8579003
1	FAN, COOLING*	8790401
2	TAB, FASTON	8529008
1	FAN, 5M S/A	8896620
1	BEZEL, SWITCH*	8719230
1	SWITCH, KEYLOCK*	8489047
1	SWITCH, ON/OFF*	8489048
1	INDICATOR LIGHT*	8469009
1	BEZEL ASSY	8896610
1	DRIVE, 5 1/4 HARD	8790202
1	HARNESS, LAMP	8709347
2	MOUNT, DRIVE	8729131
4	WASHER, LOCK #6	8589018
4	SCREW, #6-32 X 1/4 PPH	8569098
1	DRIVE, S/A	8896609
1	FILTER	8739010
4	NUT,LOCK #6-32	8579004
4	SCREW, #6-32 X 2 F.CNTSK	8569155
2	SCREW, #6-32 X 1/2	8569126
2	SCREW, #6-32 X 1/4 THD FM	8569040
4	SCREW #6-32 X 1/4"PPH	8569098
4	WASHER, #6	8589018
2	CLIP, CORD .38" DIA.	8559010
7	TUBING 1/8DX1/2	8539025
1	PCB ASSY, CONTROLLER*	8896130
2	IC P2114 U17, U18	8042114
1	IC, 8X300 MICRO-CONT	8040300
1	IC 28S86 BPROM	8040086
1	IC 28S86 BPROM (U34)PRGMD	8896603
1	IC, 28S86 BPROM	8040086
1	IC, 28S86 BPROM (U40)PRGMD	8896602
1	IC, 28S86 BPROM	8040086
1	IC, 28S86 BPROM (U41)PRGMD	8896604
1	IC, WD 1100-01 (U9)	8040111
1	IC, WD 1100-12 (U5)	8041112
1	IC, WD 1100-03 (U11)	8040113

1	IC, WD 1100-04 (U6)	8040114
1	IC, WD 1100-05 (U7)	8040115
1	LABEL, CONTROL S/N	8789732
1	ASSEMBLY	8896600
1	VISUAL	8896600
1	TESTING	8896600
1	REPAIR	8896600
1	PCB, CONTROLLER 5M F/A	8896600
1	SHIELD, POWER SUPPLY*	8729132
1	INSULATOR	8539026
1	POWER, SUPPLY	8790043
4	SCREW, #6-32 X 1/4"PPH	8569098
4	WASHER, LOCK	8589018
2	SCREW, #10 X 1/4"PH	8569153
1	WASHER, .141 1DX .167 OD	8589072
5	SCREW, #6-32X3/8"PPH	8569003
1	SHIELD, PCB S/A	8896608
1	HARNESS DC MSTR	8709334
4	SCREW, #6-32X1/4 PPH	8569098
4	WASHER, #6 LOCK	8589018
1	MAP, MEDIA ERROR	8759131
1	HOLDER, PLASTIC MAP	8590109
1	CABLE, INT. DATA MSTR	8709324
1	COVER, TOP	8729123
2	CLIP, GRD.	8559040
5	SCREW, #8-32X3/8"	8569107
5	WASHER, #8 FLAT	8589027
1	LOGO STRIP*	8719221
1	BEZEL*	8719209
1	COVER, TOP S/A	8898403
3	SCREW, #6-32X3/8" PPH	8569026
1	LABEL, WARRANTY NOT.	8789090
1	BAG 6X15X22	8590124
1	LABEL, LINE TERMINATOR	8789597
1	CARTON, 5M HDM F/A	8896616
1	MANUAL, SERVICE	8749403

PRODUCT DESCRIPTION -- MODEL I HARD DISK ADAPTER

QTY	DESCRIPTION	PART NUMBER
1	PCB M I HD ADAPTER	8896503
2	RESISTOR 1K OHM 1/4 WATT 5%	8207210
2	TRANSISTOR 2N2222	8110222
1	CABLE, M I HD	8709021
1	PC BOARD M1 ADPTR W/CABLE	8896650
2	TAPE, FOAM 1/4X1X1	8690002
2	ENCLOSURE	8719027
1	LABEL, ADAPTER	8789810
1	ADAPTER F/A	8898428
1	SUPPLEMENT, MODEL I	8749411
1	DISKETTE, INTLATN SYS. S/A	8896653
1	DISKETTE, XTRA S/A	8896652
1	DISKETTE, OPRTR SYS S/A	8896651
2	FOAM	8779031
1	FOAM,DIE CUT 26-1132	8779118
1	CARTON, INDIVIDUAL	8769172
1	CABLE, EXT. DATA 20POS.	8709252
1	CABLE, EXT. CNTRL 34POS.	8709329
1	CORD, 8' POWER*	8709057
1	CABLE, INT. DATA 20 POS	8709326
1	BOX, ACCESSORIES	8769164
1	LABEL, ACCESSORY	8789820
1	KIT, ACCESSORY HDS	8896904

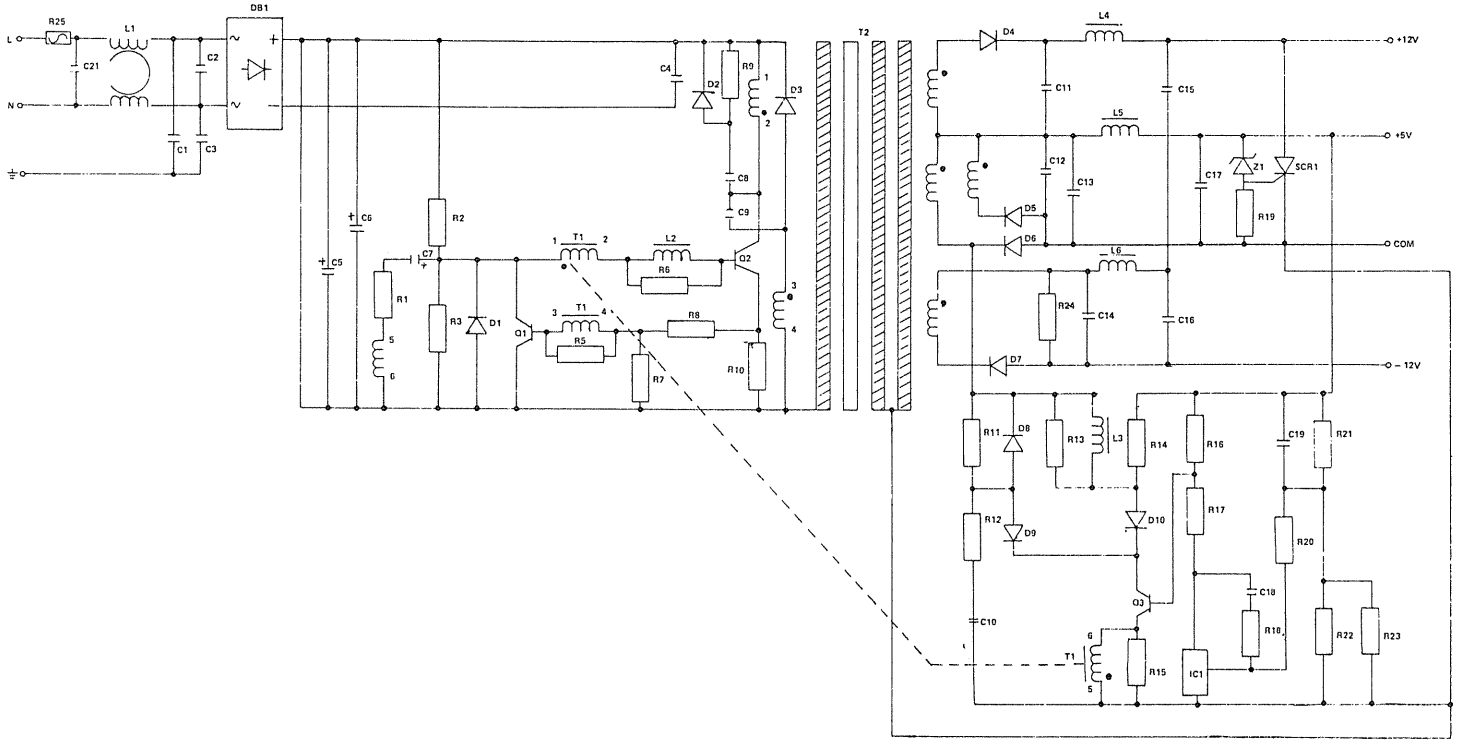
PRODUCT DESCRIPTION
5 1/4" HARD DISK
CAT. NO. 26-1131

1	CASE BOTTOM*	8729129
1	LABEL, FCC PART 15	8789287
1	LABEL, FCC ID HDS	8789773
4	FOOT	8590123
4	FASTENER, #10 X 1/2"	8569062
4	WASHER, 1/2 O.D.	8589074
1	LABEL, S/N 26-1131	8789783
1	PLUG, 2 1/2" DIA.	8729148
1	OPO10 5M HDS	8896901
1	CABLE, INT CNTRLR	8709325
1	CABLE, INT. CNTRL/SLV	8709328
2	SCREW, #6 X 5/16 BRICO IND.	8569130
2	SCREW, #4-40X3/4 PPH	8569059
2	NUT,#4-40 KEPS LOCK	8579003

2	WASHER, #4 STAR	8589075
1	OPO20 5M HDS	8896900
1	FAN, COOLING	8790401
2	TAB, FASTON	8529008
1	FAN, 5M S/A	8896620
4	SCREW, #6-32 X 2" FCNTR	8569155
1	FILTER	8739010
4	NUT, #6-32 LOCK*	8579004
1	HARNESS, AC SLV	8709333
2	SCREW, #4-40 X 1/2"PPH	8569033
2	NUT, LOCK #4-40	8579003
1	OPO30 5M HDS	8896902
1	BEZEL, SWITCH*	8719230
1	INDICATOR, PWR ON	8469011
1	SWITCH, ON/OFF*	8489048
1	INDICATOR LIGHT*	8469009
1	BEZEL ASSY	8896611
1	HARNESS DC ASSY	8709335
1	RELAY, 12V 70MA	8429104
4	SCREW, #6-32 X 1/2	8569126
2	SCREW, #6-32 X 1/4	8569098
2	SCREW, #6-32 X 1/4 THD FM	8569040
2	WASHER #6 LOCK	8589018
2	SCREW, #6-32 X 3/8	8569026
1	OPO40 5M HDS	8896905
2	CLIP CORD .38 DIA.	8559010
7	TUBING 1/8 DIA. X 1/2	8539025
1	OPO50 5M HDS SOLDER	8896906
1	DRIVE, 5 1/4 HARD	8790202
1	HARNESS, LED DRIVER	8709348
1	HARNESS, RELAY	8709355
2	MOUNT, DRIVE	8729131
4	WASHER, #6 LOCK	8589018
4	SCREW, #6-32 X 1/4 PPH	8569098
1	DRIVE, 5M HDS S/A	8896909
1	POWER SUPPLY	8790025
9	SCREW. #6-32 X 1/4 PPH	8569098
9	WASHER, #6 LOCK	8589018
1	SCREW, #6-32X1 PPH ZINC	8569159
2	NUT, #6-32 KEPS	8579004
1	PCB DRIVER F/A 5M	8896615
1	MAP, MEDIA ERROR	8759131

1	HOLDER, PLASTIC MAP	8590109
1	OPO60 5M HDS	8896908
1	OPO75 TESTING 5M	8896908
1	OPO85 BURN-IN 5M	8896908
1	COVER, TOP	8729123
2	CLIP, GRD.	8559040
3	SCREW, #6-32 X 3/8 PPH	8569026
5	SCREW, #8-32 X 3/8	8569107
5	WASHER, #8 FLAT	8589027
1	LOGO, STRIP	8719221
1	BEZEL	8719209
1	OPO90 5M HDS	8896910
1	OPO95 Q.C. 5M HDS	8896910
1	OP105 Q.A. 5M HDS	8896910
1	LABEL, WARRANTY NOT.	8789090
1	BAG, 6X15X22	8590124
1	LABEL, LINE TERMINATOR	8789597
1	CARTON, SECONDARY	8769166
.005	COMPONENT A	8669001
.005	COMPONENT B	8669002
.005	FILM, P-180 PACKAGING	8659014
1	CARTON, 5M HDS F/A	8896903

11/ Schematics



POWER SUPPLY SCHEMATIC DIAGRAM

REVISION				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED

J7 50 PIN CARD EDGE

U70 8304

HDBD0 19 → 1 → D0 IB
HDBD1 18 → 2 → D1 IB
HDBD2 17 → 3 → D2 IB
HDBD3 16 → 4 → D3 IB
HDBD4 15 → 5 → D4 IB
HDBD5 14 → 6 → D5 IB
HDBD6 13 → 7 → D6 IB
HDBD7 12 → 8 → D7 IB
DE, T/R → IFDEN

U71 LS 244

HDBA 0 2 → A0 IB
HDBA 1 4 → A1 IB
HDBA2 6 → A2 IB
HDBA 3 8 → A3 IB
HDBA 4 17 → A4 IB
HDBA 5 15 → A5 IB
HDBA 6 13 → A6 IB
HDBA 7 11 → A7 IB
EVEN

U73 LS 244

HDBRD # 2 → RD # IB
HDBWR # 4 → WR # IB
HDBMR # 6 → HDMR #
HDBMI # 8 → MI # IB
HDBIORQ # 18 → IORQ # IB
HDSEL # 13 → 7
HDWAIT # 15 → 5
MCLK # 17 → 3 → MCLK # PR

U74 5Ø4 → RD IB
U75 SØ4 → MI IB
U75 SØ4 → IORQ IB

41 HDBWAIT #
43 HDBSEL

INTRQ # → U52 → U65 S32 → U72 → HDWPINT #
DRQ # → U46 → U72 → 45 HDBDRQ #
39 HDBINTRQ #

IA0 IA9 →

U40 BPROM: IA0–IA10 → Q1–Q8; HIC

U39 S174: D0–D5 → Q0–Q5; CLR ← HI; CK ← MCLK

U44 S138: MCLKPR, WC # → RD0, DRQCLK, RD2, INTCLK, RD4, RD5, RD6, RD7

U45 S138: HI → WR0, WR1, WR2, WR3, WR4, WR5, WR6, WR7

U41 BPROM: IA0–IA10 → Q1–Q8; HIC

U34 BPROM: IA0–IA10 → Q1–Q8; HIC

U42:
IVB7 # 33 → IO 0
IVB6 # 34 → IO 1
IVB5 # 35 → IO 2
IVB4 # 36 → IO 3
IVB3 # 38 → IO 4
IVB2 # 39 → IO 5
IVB1 # 40 → IO 6
IVB0 # 41 → IO 7
RB # 32 → RB #

HALT 44 ← R26 10K ← +5v
SC 29 → SØ2 → WC #
WC 30
RESET # 42 → U46 → MCLK #
RESET # ← 43
MCLK → R38; R25; C32
MCLK # PR → U72 → MCLK PR; TP 14; 220Ω R39 → +5v

X1 10, X2 11 → 18 MHZ Y2
VCC 37 → +5v; C36 .1μF
VR 50; VCR 1 → Q2 2N5320; C21 .1μF

R23 1K → HIC
1K → HIS
1K → HI
1K R37 → HIS2

U59 RD Ø, WR Ø → SØ8 → RCS #

U69 S138: A4 IB, A5 IB, A7 IB, A6 IB, M1 IB, IORQ # IB → Y1–Y4; 15, 16, 17, 18 → M

U68 LS 139: A3 IB, A2 IB → Y3 → SØ8 U57 → SELDCR, SELDCR #; Y1 → NC; Y0 → SELDIR #; U58 → SELDIR

U67 LS 139: A0 IB, A1 IB → RDDIR0 #, RDDIR1 #
RD # IB, SELDIR # → S32 U65 → WR # IB
A0 IB, A1 IB → U66 LS 139

HIS → 8 → 425 U55 → D0 IB

+5 → R17 4.3K; C21 .68μF
CSAC → 200 nS LS 123 U25 → CSAC1 #; TP 2; HIC

DEVEN, SELDCR # → U58 → S32 U65 → DCRCS #

U59 SØ8: IA10 → RSTCR #
SFTRESET → U76 100 nS LS Z21 → RESET #
R42 10K → IN 4148 CR 1; 2.2 μF C 52
R41 10K → +5v; C56 .01μF

MATERIAL	UNLESS OTHERWISE SPECIFIED			DRAFT L. PENLAND	DATE 6-2-82	TITLE 5 1/4" HARD DISK CONTROLLER
FINISH	TOLERANCES .XX= ± .010 .XXX = ±.005 ANGLES=±1° HOLE DIA TOLERANCES .014 - .250 = +.005 -.001 .251 - .750 = +.008 -.001 .751 - UP = +.015 -.001			CHECK	DATE	
				DESIGN	DATE	
				APPD	DATE	
				APPD	DATE	
	DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING			tandy	DWG NO. 8000154	SIZE D
	DO NOT SCALE THIS DRAWING	NEXT ASSY.	USED ON		SCALE	SHEET 1 OF 4

R43 LINE TERMINATORS 220/330
9 HDBD Ø
8 HDBD 1
7 HDBD 2
6 HDBD 3
5 HDBD 4
4 HDBD 5
3 HDBD 6
2 HDBD 7

R44 LINE TERMINATORS 220/330
2 HDBA Ø
3 HDBA 1
4 HDBA 2
5 HDBA 3
6 HDBA 4
7 HDBA 5
8 HDBA 6
9 HDBA 7

R45 LINE TERMINATORS 220/330
HDBRD*
HDBWD*
HDBMD*
HDBMI*
HDBIORQ*

4 PIN J8
1 +12v
2 +5v
3 +5v
4

+12v — 47uF — +5v — 100uF — 100uF

LL61 LS 374
AØ IB
A1 IB
A2 IB
CSAC
CRCOK
WR* IB
BDDNE
RDVF*
RD2
MCLK
ØE
ØØ ØD
Ø1 ØQ
Ø2 1Q
Ø3 2Q
Ø4 3Q
Ø5 4Q
Ø6 5Q
Ø7 6Q
7Q
IDØ
ID1
ID2
ID3
ID4
ID5
ID6
ID7

WR* IB — LS32 — LL24 — BIC*
DCRCS* — LS32 — BOC*
RD* IB

LL58
BIC
BOC
WC
RC*
WR6
RD6

LL60 BT31
DØ IB
D1 IB
D2 IB
D3 IB
D4 IB
D5 IB
D6 IB
D7 IB
MCLK
ME
ØØ ØD
Ø1 ØQ
Ø2 1Q
Ø3 2Q
Ø4 3Q
Ø5 4Q
Ø6 5Q
Ø7 6Q
7Q
+5v

RA Ø - RA 9

LL27 LS 191
RCS*
IDØ
ID1
ID2
ID3
HIS
PE
U/D
CE
RC
RAØ
RA1
RA2
RA3

LL28 LS 191
RCS*
ID4
ID5
ID6
ID7
WR2
RA4
RA5
RA6
RA7

LL26 LS 191
RCS*
IDØ
ID1
RA8
RA9
ROVF*

LL29 LS 174
ID2
ID3
ID4
ID5
ID6
ID7
WR7
HIC
WAEN*
CRCIZ*
RGATE
WRITE*
IBLA*
SRCH

LL17 2114
LL18 2114
RAØ
RA1
RA2
RA3
RA4
RA5
RA6
RA7
RA8
RA9
IDØ
ID1
ID2
ID3
ID4
ID5
ID6
ID7
WE
WC*
RB*
CE

IOØ - IO7

LL63
LL64
HSELØ
HSEL 1
HSEL 2
DR 54
DR 53
DR 62
DR 51

LL62 LS 273
WR1
RESET
CP
MR

LL59
SDWP
WGI
WGATE
RWC
STEP
DIR IN

LL52 LS 174
WR1
RESET

J5 34PIN
J6 50PIN
ALL ODD

220/330 R40 — 5v
TP12
IND FX
READY
WF
SC
TRE Ø

LL74 LS 374
MCLK
RD5
DRSEL*
DRUN*
HFRQ*

LL22 LS 74
WIS
WR3

LL57 308
IORQ IB
SELDCR

S64 LL56
DEVEN
RD IB
SELDIR
MI IB
TP 13
LL58
IFDEN
HOSEL

DEVEN
WAITEN IB
SFTRESET
R9TCR*

LL47 LS 273
LL48 LS 244
DØ IB
D1 IB
D2 IB
D3 IB
D4 IB
D5 IB
D6 IB
D7 IB
WRDIR1*
RDDIR1*

R36 15Ω — +12v

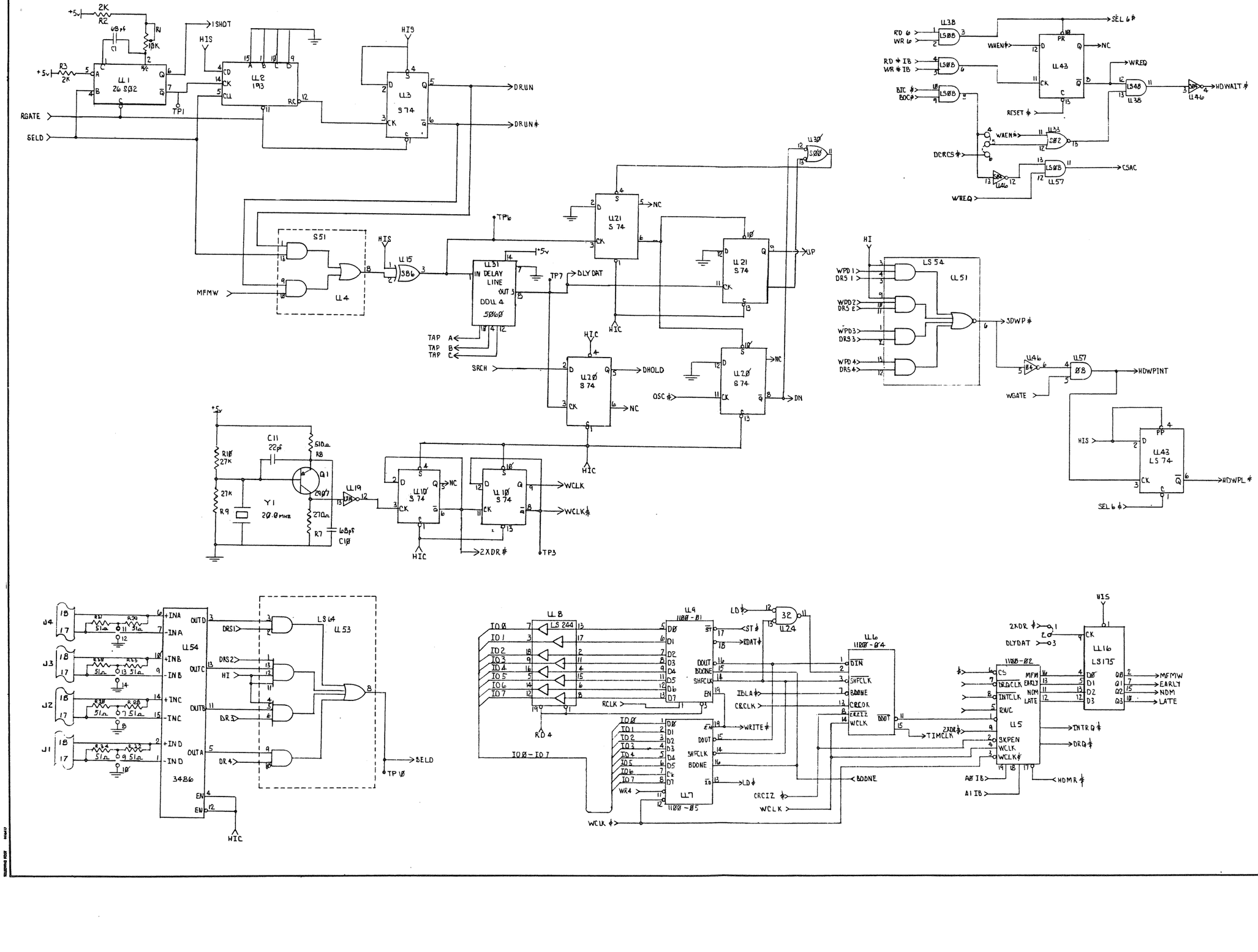
J1 J2 J3 J4
DRSEL*
1 2 4 6 8 11 12 15 16 19 20

R27 4.7K
WPD1
WPD2
WPD3
WPD4

LL50 LS240
WPD1* (Ø1-P5)
WPD2* (Ø2-P5)
WPD3* (Ø3-P5)
WPD4* (Ø4-P5)
NC
NC
HOWPL*
INTRQ*

LL49 LS 244
D7 IB
D6 IB
D5 IB
D4 IB
D3 IB
D2 IB
D1 IB
DØ IB
RDDIR Ø*

DWG NO	8000154
REV	
SCALE	
SHEET	2. OF 4



DWG NO	REV
8000154	
SCALE	SHEET 3 OF 4

U77
7805 OUT
GND
+12V
47uF C34
10uF C29
R11 180Ω
R18 180Ω
MPQ 6700
C19 10pF
2k R16
510Ω R15
U123
LP
C18 10pF
316Ω R13
240Ω R14
DN
1800Ω R12
1800Ω R19
R28 33Ω
TP8
.1uF
C33 7.6pF
C31 30pF
.0068uF C24
150pF C25
R21 680Ω
330pF C30
+5V
R24 4.7K
R27 5.6K
U9
LL 7B
7545J
U137 S124
FREQ CNT
RNG
VCC
VCCA
LL32
+5
U14 S74
PR
CK
HIS
RCLK
RCLK#
DHOLD
DOSC#
S04 LL46
TP9
U9
LL 7B
7545J
+5V
HIS
LL13 S74
LL12 S74
RCLK
RCLK#
DYL DAT
RGATE
RDATA#
TP4
1100-03
LL11
DRUN
ISHOT
DIN
RCLK
RCLK#
CLKIN
CP
RST
QOUT
ENDET
AMDET
HFRQ#
AMDET#
SRCH
TP5
LL14 S74
ST#
NC
HIC
LS 54
LL37
TAP C
EARLY
TAP B
NOM
TAP C
LATE
HI
WGI*
LL19
S86 LL15
TP11
TIMCLK
MC 3487
INA
INB
INC
IND
C35
J1
J2
J3
J4
+TIMCLK
-TIMCLK
+MFMD
-MFMD

DWG NO	REV
8000154	
SCALE	SHEET 4 OF 4

13/Supplement

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