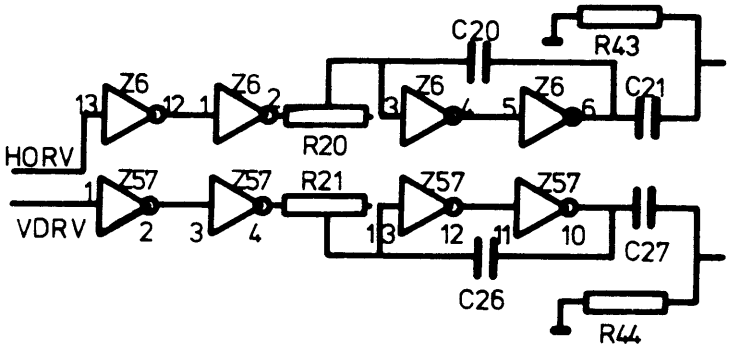
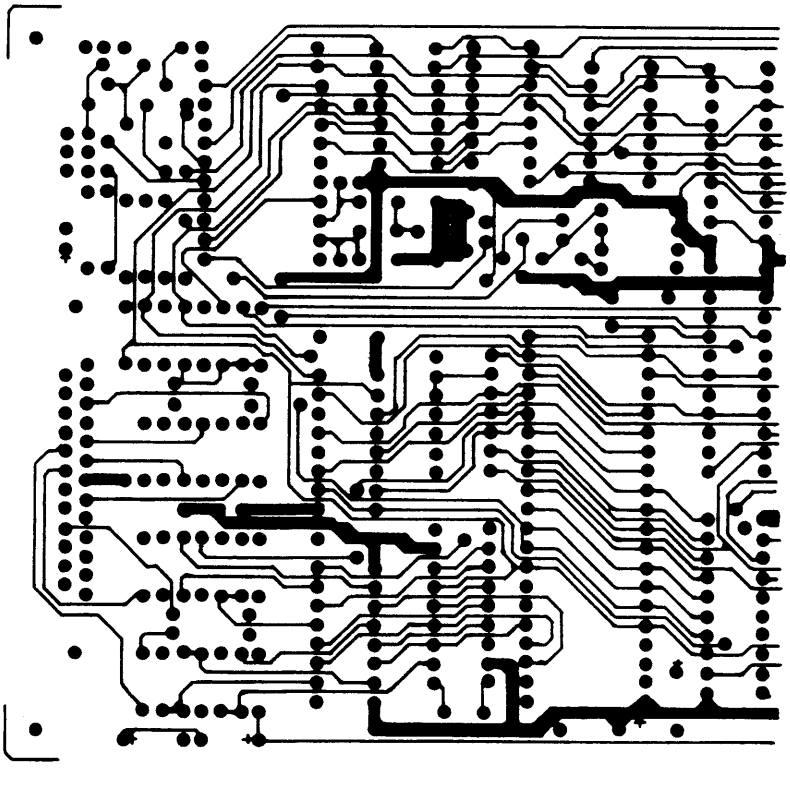
COMPUTER

TRS&BØ

GEBRUIKERS VERENIGING AFDELING: WEST

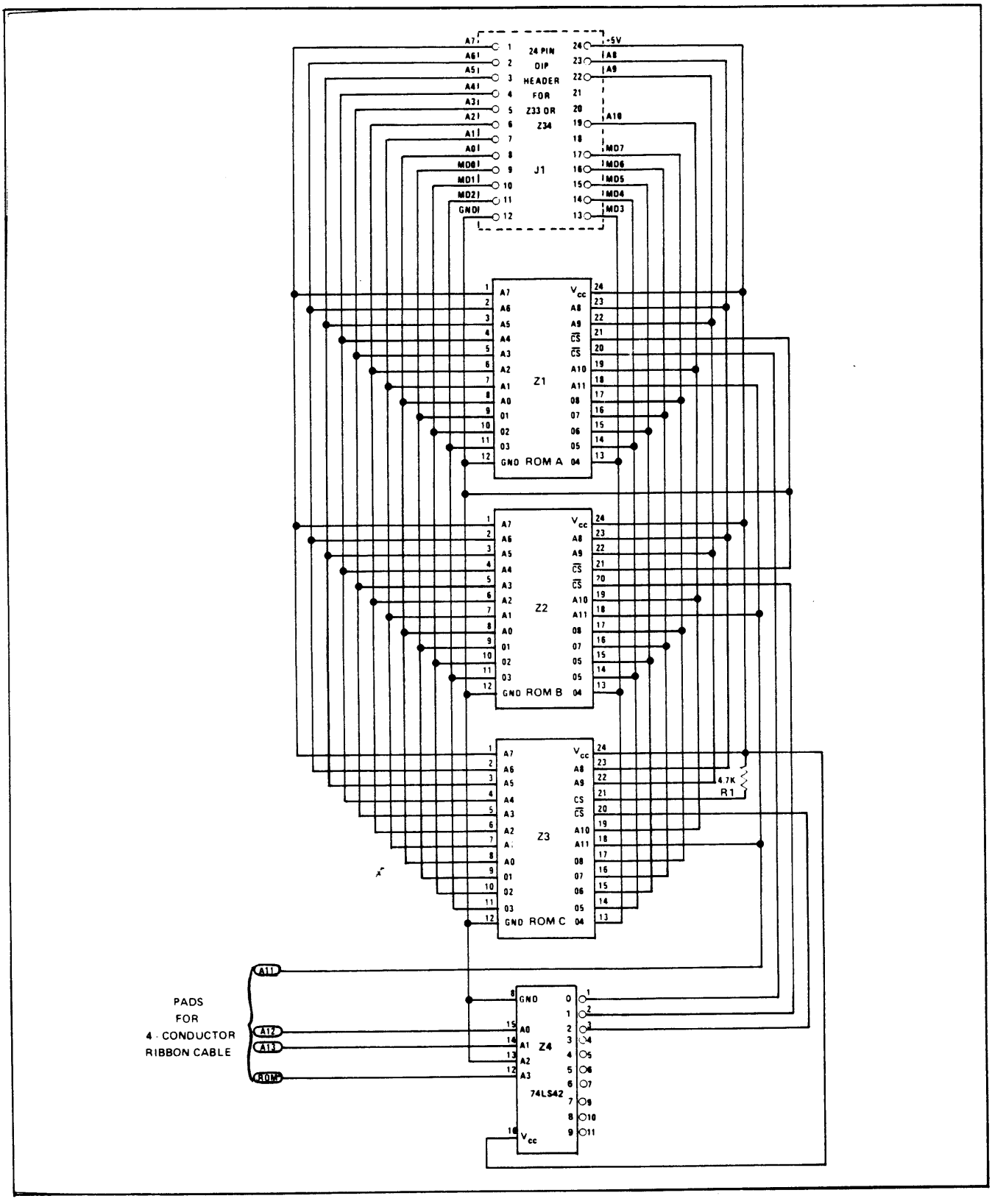
MODEL I HARDWARE





TRS-80 model I paperware. Schema's en Connectoren.

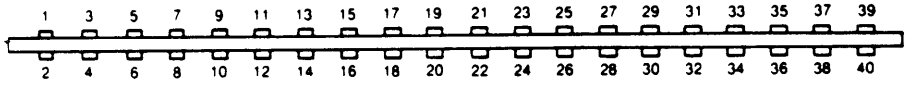
Inhoud.


24 PIN
DIP
HEADER
FOR
Z33 OR
Z34
J1
+5V
A8
A9
A10
MD7
MD6
MD5
MD4
MD3
A7
A6
A5
A4
A3
A2
A1
A0
MD0
MD1
MD2
GND
Z1
ROM A
Z2
ROM B
Z3
ROM C
4.7K
R1
PADS
FOR
4 CONDUCTOR
RIBBON CABLE
A11
A12
A13
ROM
Z4
74LS42
GND
Vcc

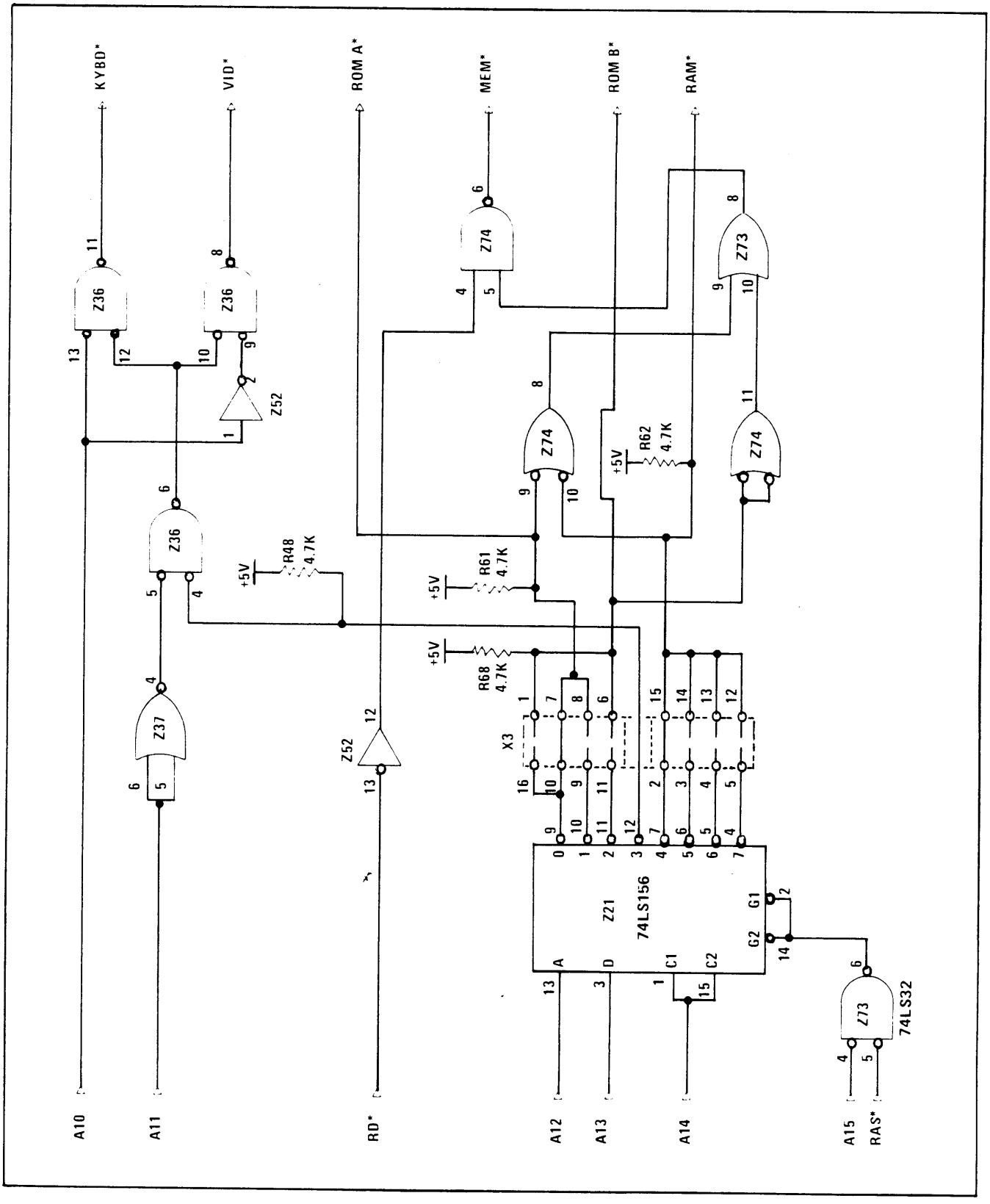
Pin Connections for Expansion-Port Edge Card

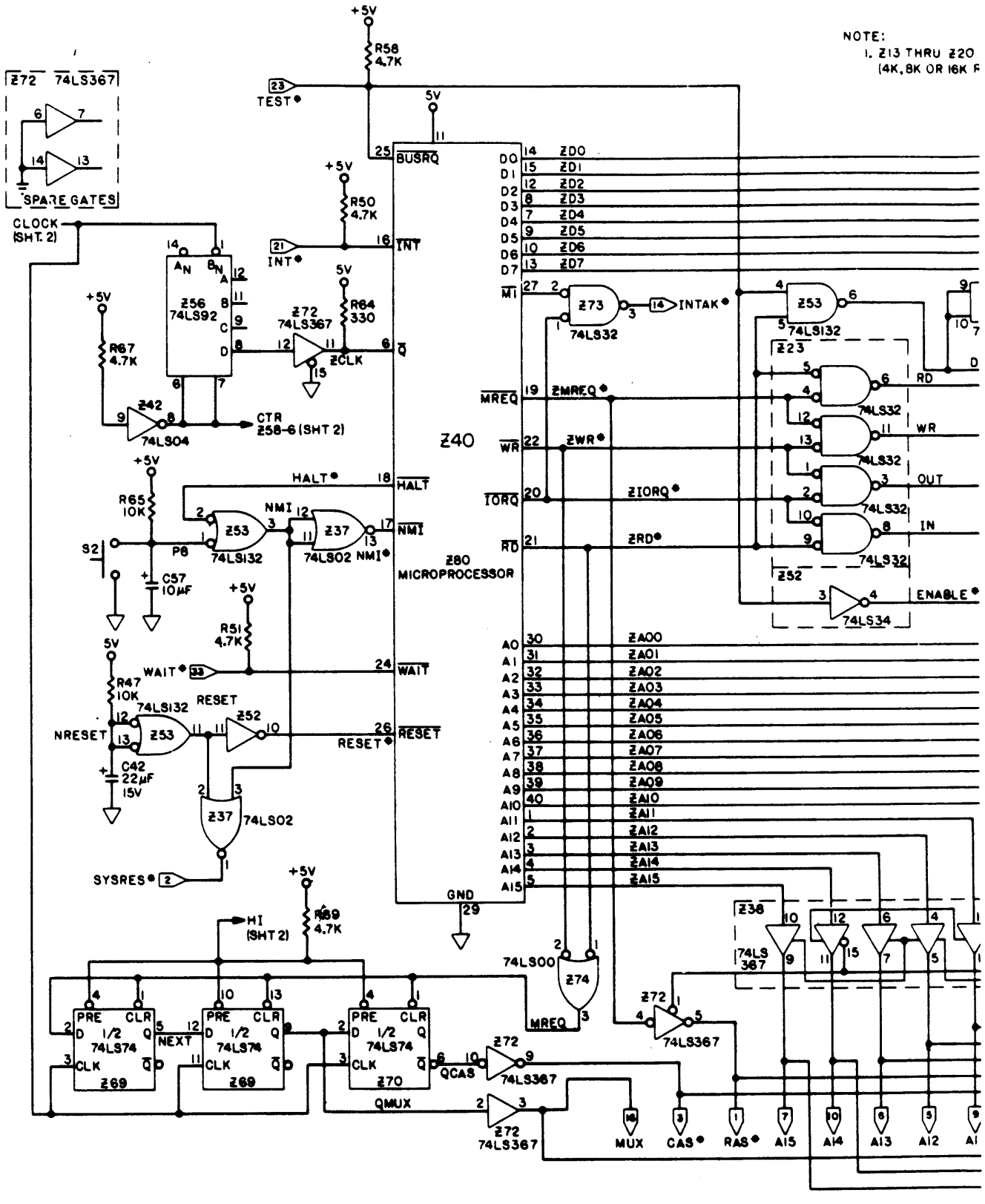
P/N	SIGNAL NAME	DESCRIPTION
1	RAS*	Row Address Strobe Output for 16-Pin Dynamic Rams
2	SYSRES*	System Reset Output, Low During Power Up Initialize or Reset Depressed
3	CAS*	Column Address Strobe Output for 16-Pin Dynamic Rams
4	A1Ø	Address Output
5	A12	Address Output
6	A13	Address Output
7	A15	Address Output
8	GND	Signal Ground
9	A11	Address Output
10	A14	Address Output
11	A8	Address Output
12	OUT*	Peripheral Write Strobe Output
13	WR*	Memory Write Strobe Output
14	INTAK*	Interrupt Acknowledge Output
15	RD*	Memory Read Strobe Output
16	MUX	Multiplexor Control Output for 16-Pin Dynamic Rams
17	A9	Address Output
18	D4	Bidirectional Data Bus
19	IN*	Peripheral Read Strobe Output
20	D7	Bidirectional Data Bus
21	INT*	Interrupt Input (Maskable)
22	D1	Bidirectional Data Bus
23	TEST*	A Logic "Ø" on TEST* Input Tri-States AØ-A15, DØ-D7, WR*, RD*, IN*, OUT*, RAS*, CAS*, MUX*
24	D6	Bidirectional Data Bus
25	AØ	Address Output
26	D3	Bidirectional Data Bus
27	A1	Address Output
28	D5	Bidirectional Data Bus
29	GND	Signal Ground
30	DØ	Bidirectional Data Bus
31	A4	Address Bus
32	D2	Bidirectional Data Bus
33	WAIT*	Processor Wait Input, to Allow for Slow Memory
34	A3	Address Output
35	A5	Address Output
36	A7	Address Output
37	GND	Signal Ground
38	A6	Address Output
39	+5V	5 Volt Output (Limited Current)
40	A2	Address Output

NOTE: *means Negative (Logical "Ø") True Input or Output

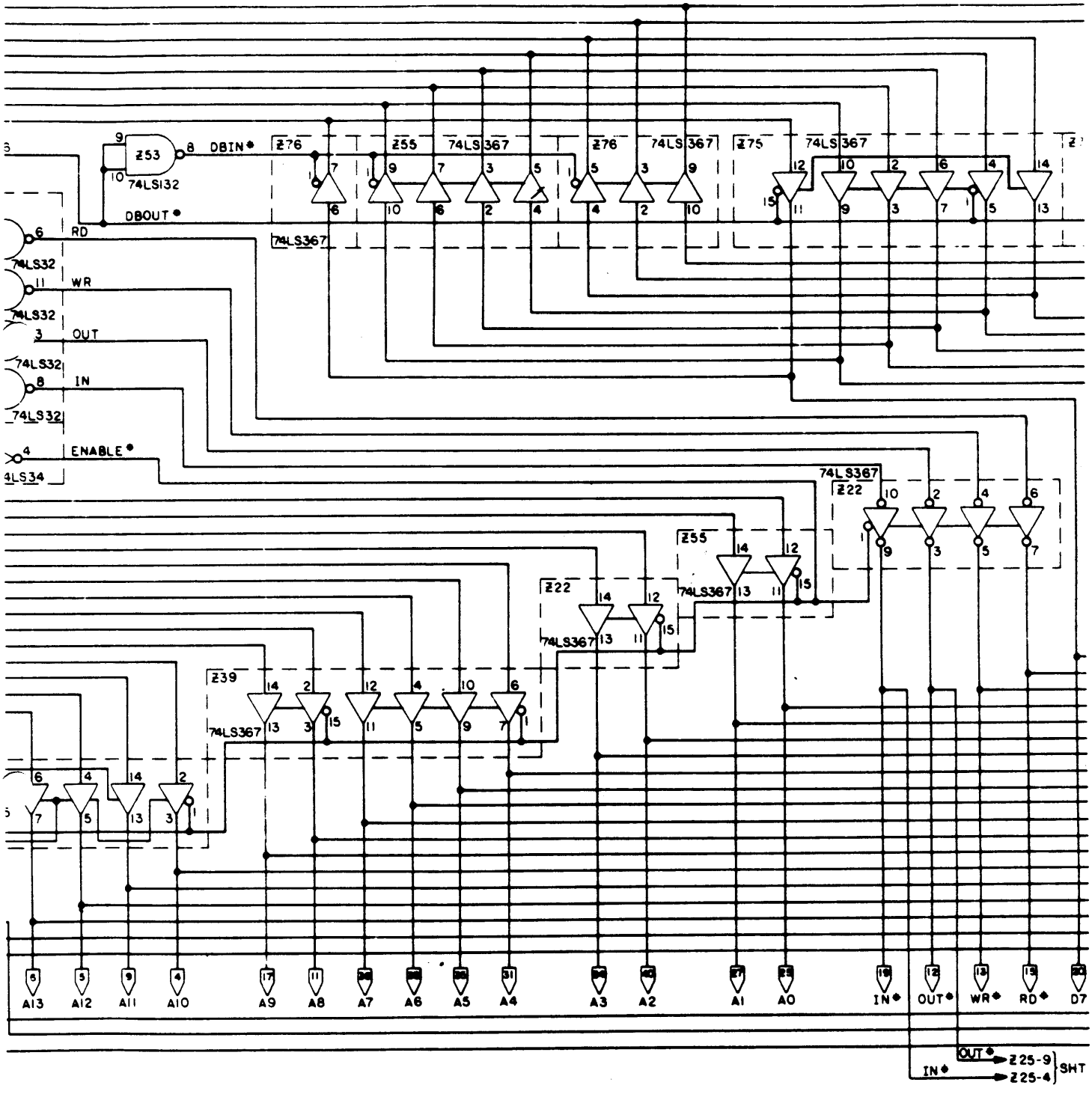


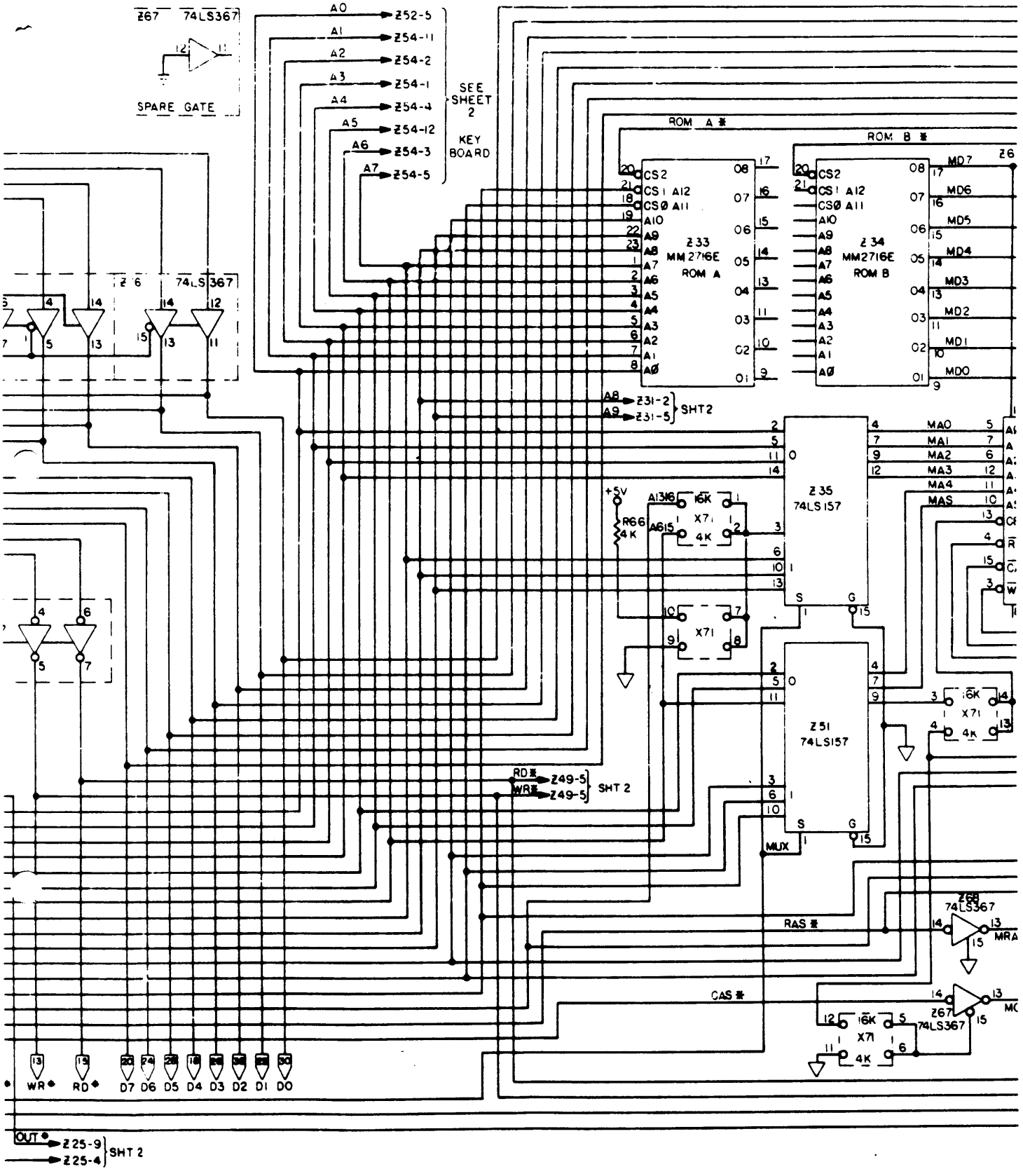
Mates with AMP P/N 88103-1 Card Edge Connector or Equivalent

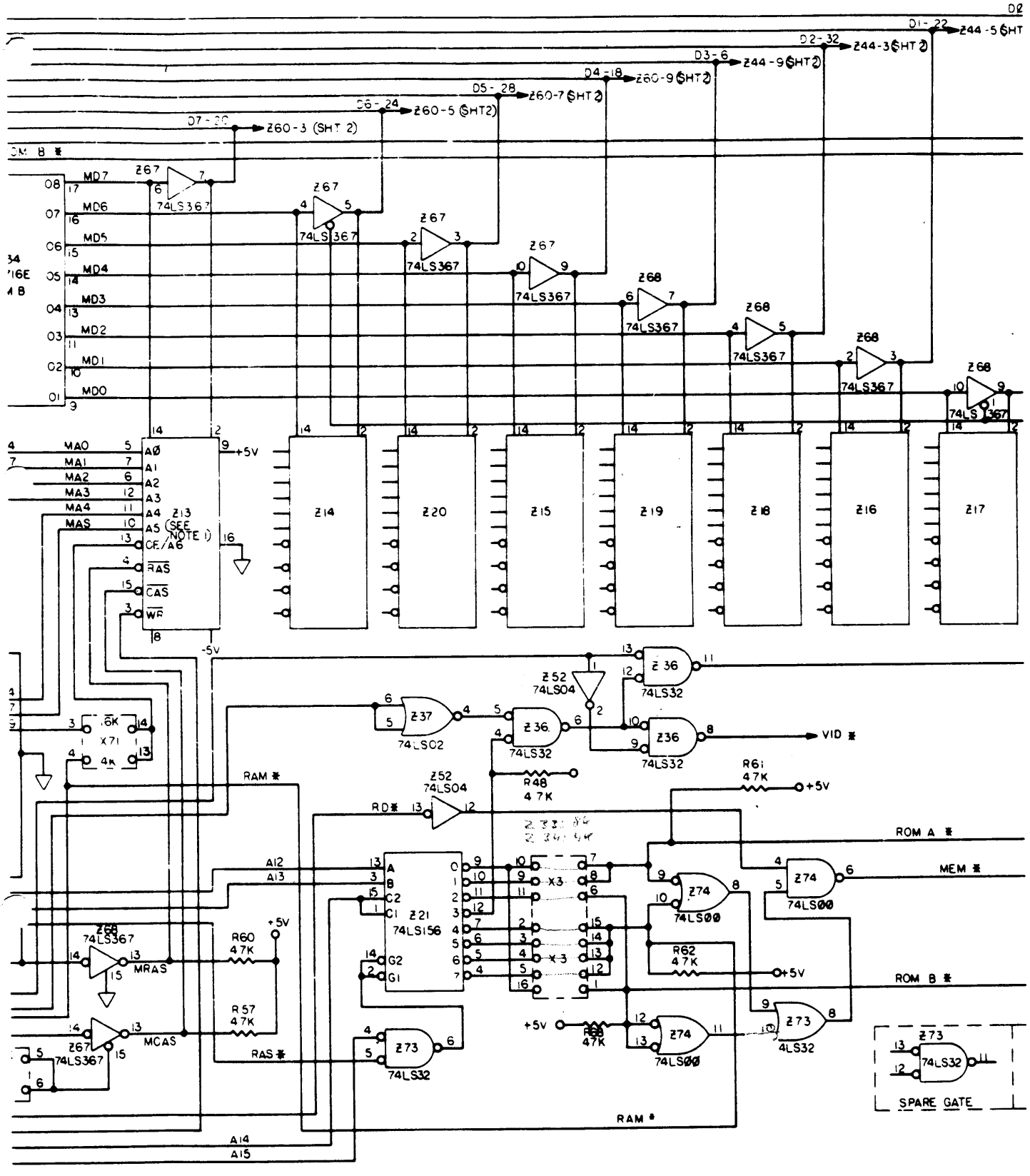

KYBD*
VID*
ROM A*
MEM*
ROM B*
RAM*
Z36
Z52
Z74
Z73
Z37
R48 4.7K
R61 4.7K
R62 4.7K
R68 4.7K
+5V
X3
Z21
74LS156
74LS32
A10
A11
RD*
A12
A13
A14
A15
RAS*


NOTE:
1. Z13 THRU Z20
(4K, 8K OR 16K R
Z72 74LS367
SPARE GATES
CLOCK
(SHT. 2)
+5V
R58
4.7K
TEST*
BUSRQ
INT*
INT
R50
4.7K
R64
330
Z72
74LS367
ZCLK
Q
Z56
74LS92
R67
4.7K
Z42
74LS04
CTR
Z58-6 (SHT 2)
Z40
HALT*
HALT
R65
10K
NMI
Z53
74LS132
Z37
74LS02
NMI*
S2
P8
C57
10µF
R51
4.7K
WAIT*
WAIT
R47
10K
RESET
NRESET
Z52
RESET*
C42
22µF
15V
SYSRES*
HI
(SHT 2)
R69
4.7K
Z80
MICROPROCESSOR
ZD0
ZD1
ZD2
ZD3
ZD4
ZD5
ZD6
ZD7
M1
Z73
74LS32
INTAK*
MREQ
ZMREQ*
WR
ZWR*
IORQ
ZIORQ*
RD
ZRD*
GND
ZA00
ZA01
ZA02
ZA03
ZA04
ZA05
ZA06
ZA07
ZA08
ZA09
ZA10
ZA11
ZA12
ZA13
ZA14
ZA15
Z53
74LS132
Z23
RD
WR
OUT
IN
74LS32
Z52
ENABLE*
74LS34
Z38
74LS
367
Z74
74LS00
Z72
74LS367
PRE
CLR
D
1/2
Q
CLK
74LS74
Z69
NEXT
Z70
QCAS
QMUX
MUX
CAS*
RAS*
A15
A14
A13
A12
A1

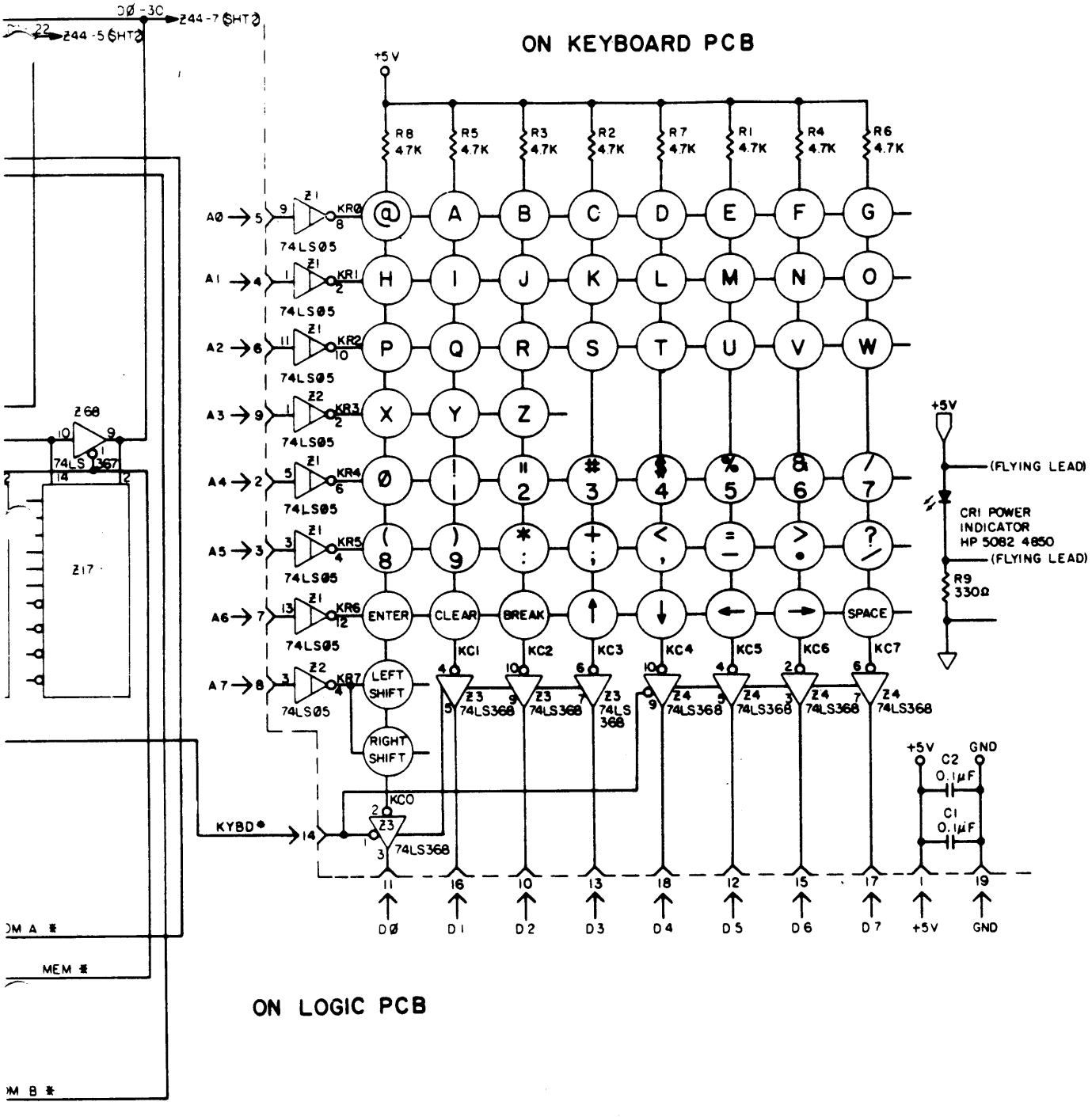
Z13 THRU Z20 ARE RANDOM ACCESS MEMORIES
(4K, 8K OR 16K RAM'S)

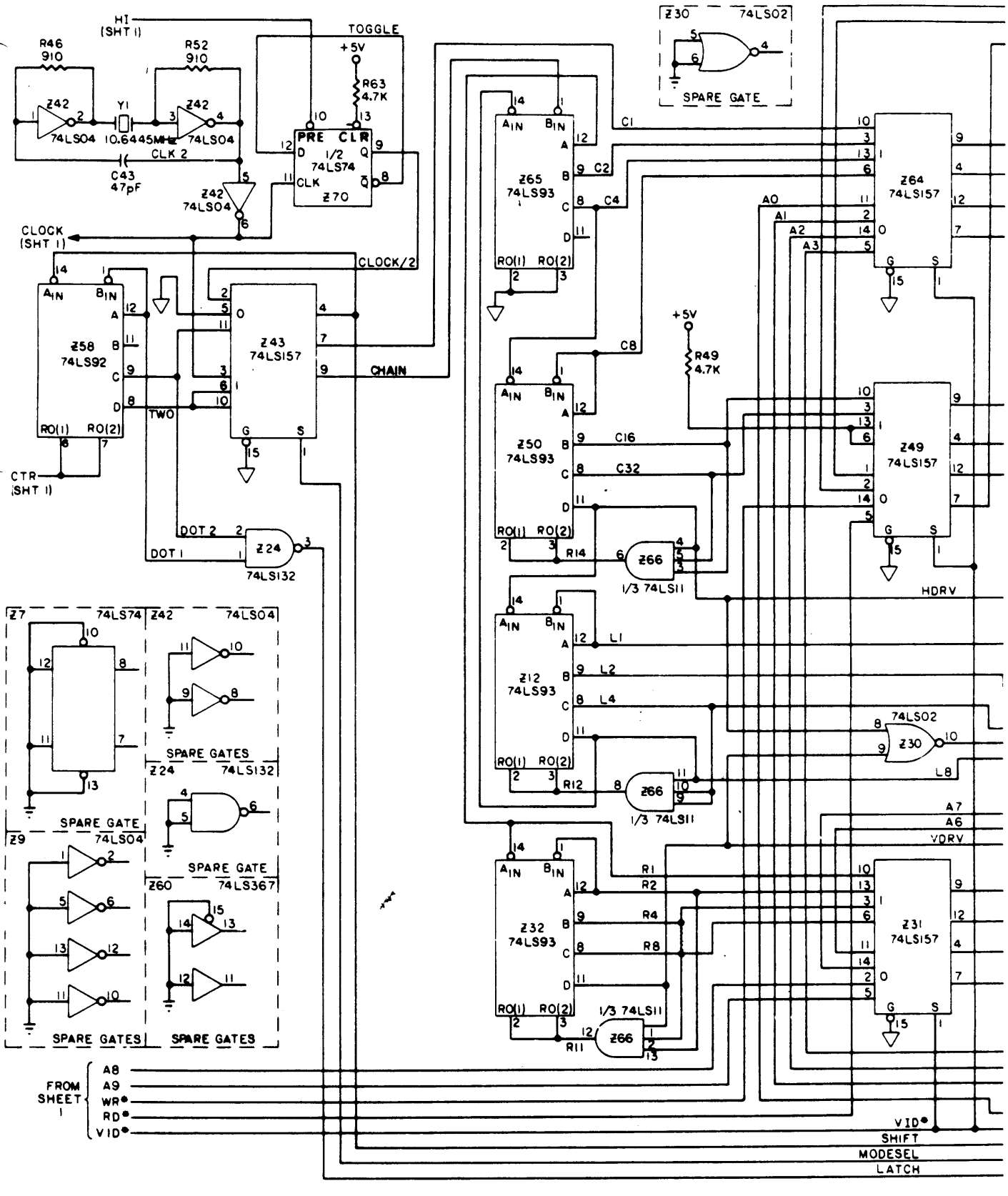


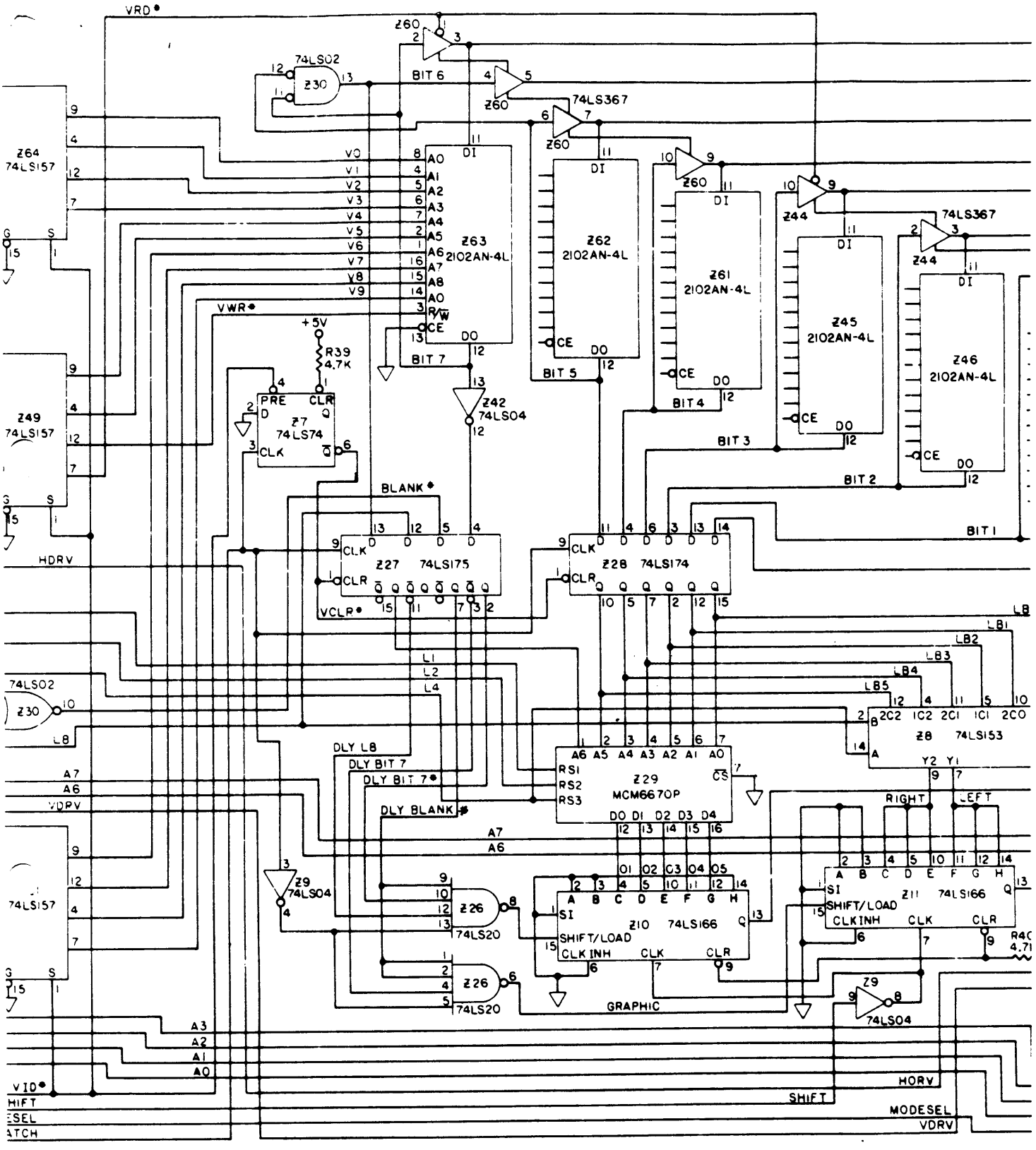

Z67 74LS367
SPARE GATE
A0 → Z52-5
A1 → Z54-11
A2 → Z54-2
A3 → Z54-1
A4 → Z54-4
A5 → Z54-12
A6 → Z54-3
A7 → Z54-5
SEE SHEET 2
KEY BOARD
ROM A *
ROM B *
Z33 MM2716E ROM A
Z34 MM2716E ROM B
CS2
CS1 A12
CSØ A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
AØ
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MDO
A8 → Z31-2
A9 → Z31-5
SHT2
Z35 74LS157
Z51 74LS157
MA0
MA1
MA2
MA3
MA4
MA5
+5V
R66 4K
A1316
A615
16K
4K
X71
MUX
RD* → Z49-5
WR* → Z49-5
SHT 2
RAS *
CAS *
Z68 74LS367
Z67 74LS367
MRA
WR*
RD*
D7 D6 D5 D4 D3 D2 D1 DO
OUT* → Z25-9
Z25-4
SHT 2



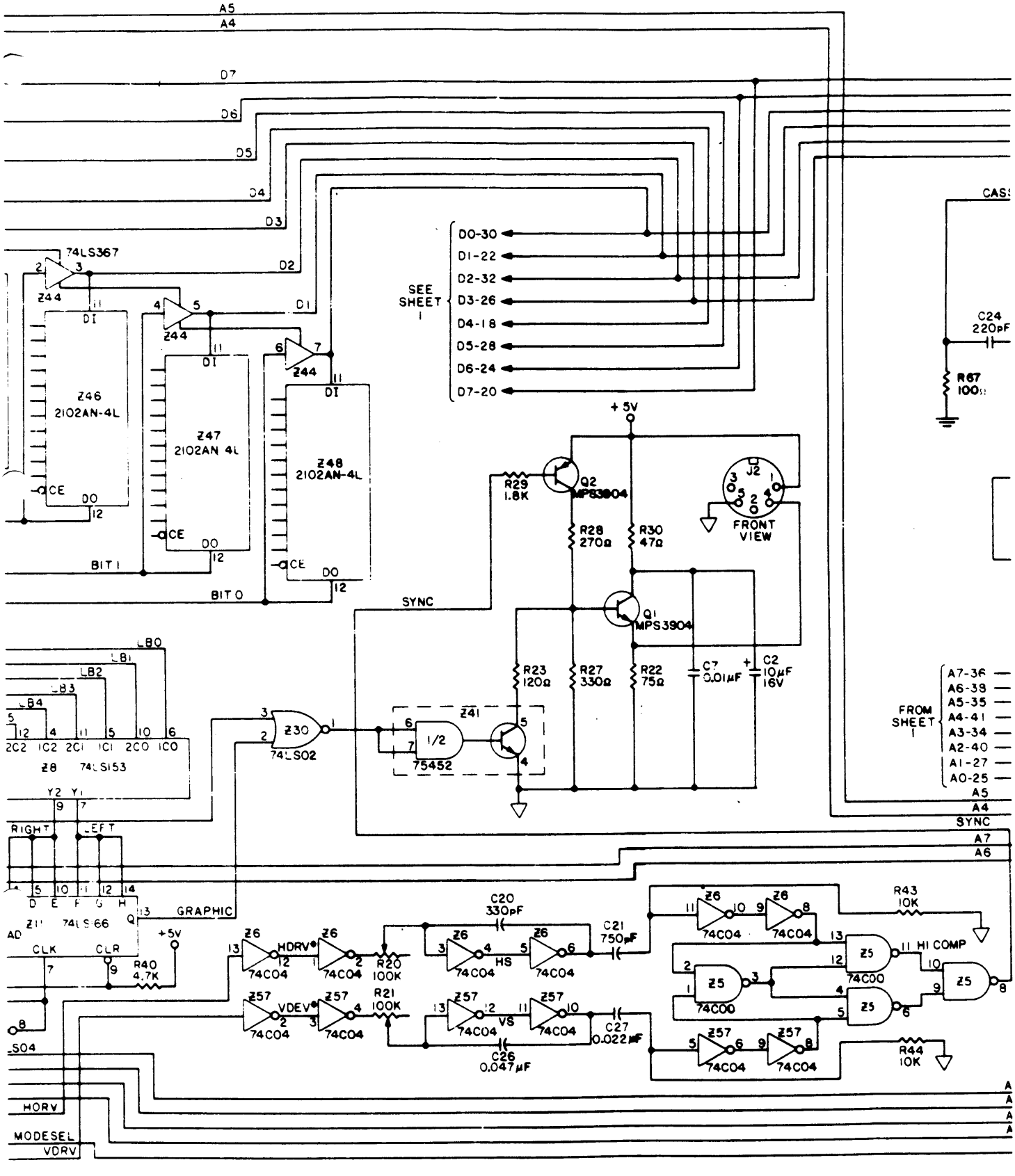
TRS-80 Amerikaanse model I. Schema. Sheet 1 D. 7


ON KEYBOARD PCB
+5V
R8 4.7K
R5 4.7K
R3 4.7K
R2 4.7K
R7 4.7K
R1 4.7K
R4 4.7K
R6 4.7K
A0
A1
A2
A3
A4
A5
A6
A7
74LS05
74LS368
KR0
KR1
KR2
KR3
KR4
KR5
KR6
KR7
KC1
KC2
KC3
KC4
KC5
KC6
KC7
KC0
@ A B C D E F G
H I J K L M N O
P Q R S T U V W
X Y Z
0 1 2 3 4 5 6 7
8 9 : ; , - . /
ENTER
CLEAR
BREAK
SPACE
LEFT SHIFT
RIGHT SHIFT
KYBD*
(FLYING LEAD)
CR1 POWER INDICATOR HP 5082 4850
R9 330Ω
C2 0.1μF
C1 0.1μF
GND
D0
D1
D2
D3
D4
D5
D6
D7
ON LOGIC PCB
74LS32
74LS04
74LS00
SPARE GATE

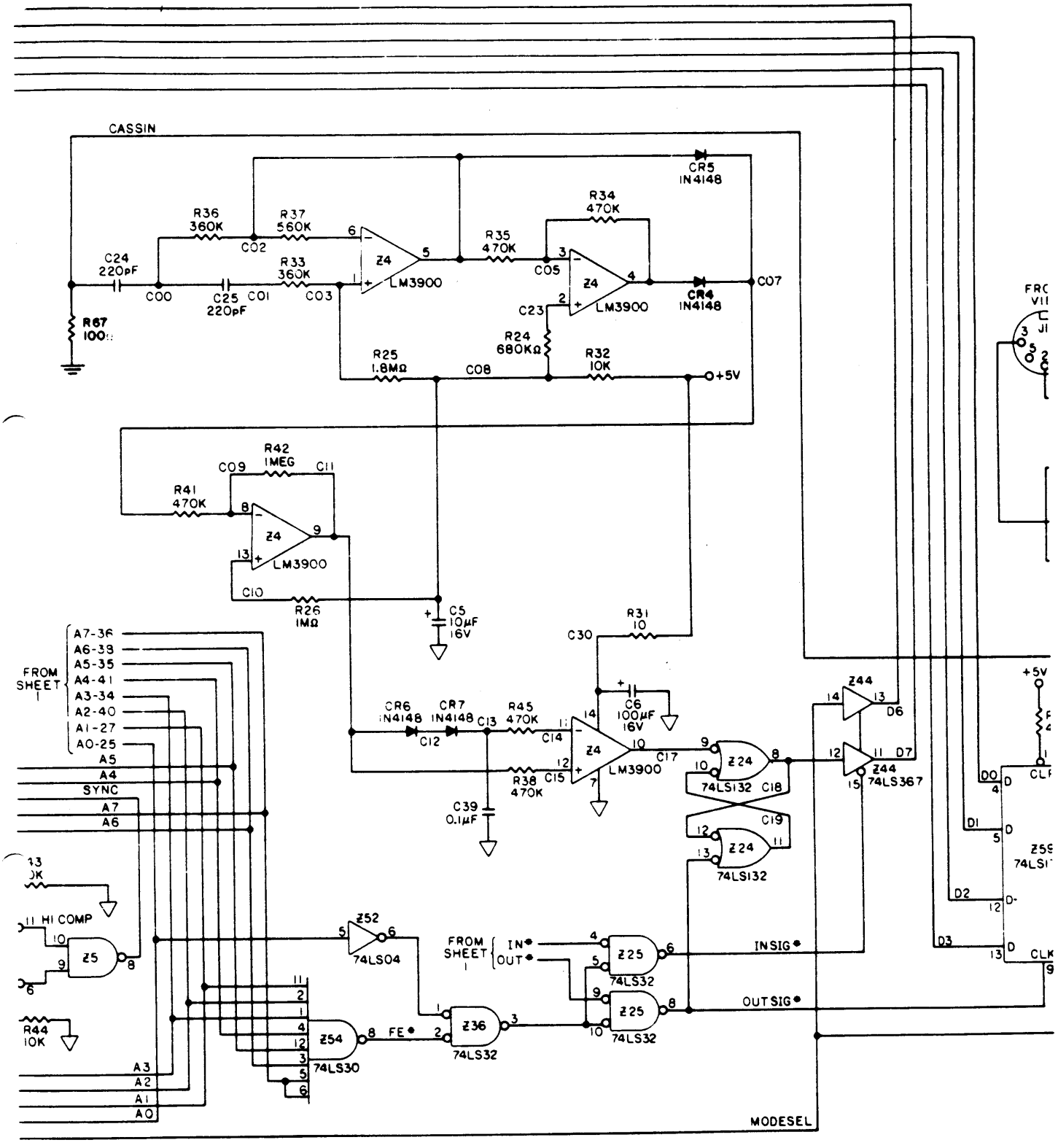

HI (SHT 1)
R46 910
R52 910
Z42 74LS04
Y1 10.6445MHz
CLK 2
C43 47pF
TOGGLE
+5V
R63 4.7K
PRE CLR
1/2 74LS74
Z70
CLOCK (SHT 1)
CLOCK/2
Z58 74LS92
Z43 74LS157
CHAIN
TWO
CTR (SHT 1)
DOT 2
DOT 1
Z24 74LS132
Z30 74LS02
SPARE GATE
Z65 74LS93
Z64 74LS157
C1
C2
C4
C8
C16
C32
A0
A1
A2
A3
R49 4.7K
Z50 74LS93
Z49 74LS157
R14
Z66
1/3 74LS11
HDRV
Z12 74LS93
L1
L2
L4
L8
R12
A7
A6
VDRV
Z232 74LS93
Z31 74LS157
R1
R2
R4
R8
R11
Z7 74LS74
Z42 74LS04
SPARE GATES
Z24 74LS132
Z9 74LS04
SPARE GATE
Z60 74LS367
SPARE GATES
FROM SHEET 1
A8
A9
WR*
RD*
VID*
VID*
SHIFT
MODESEL
LATCH

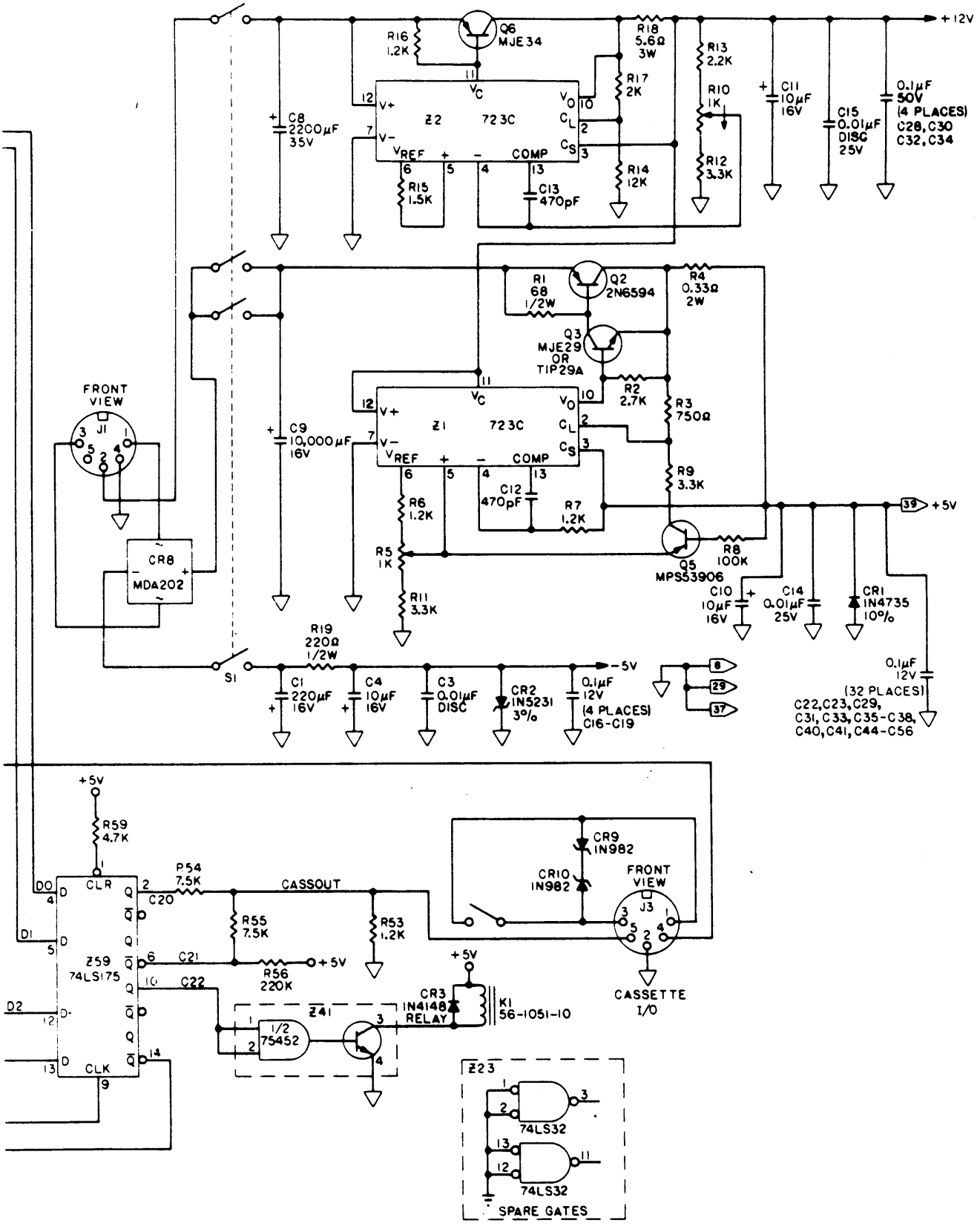


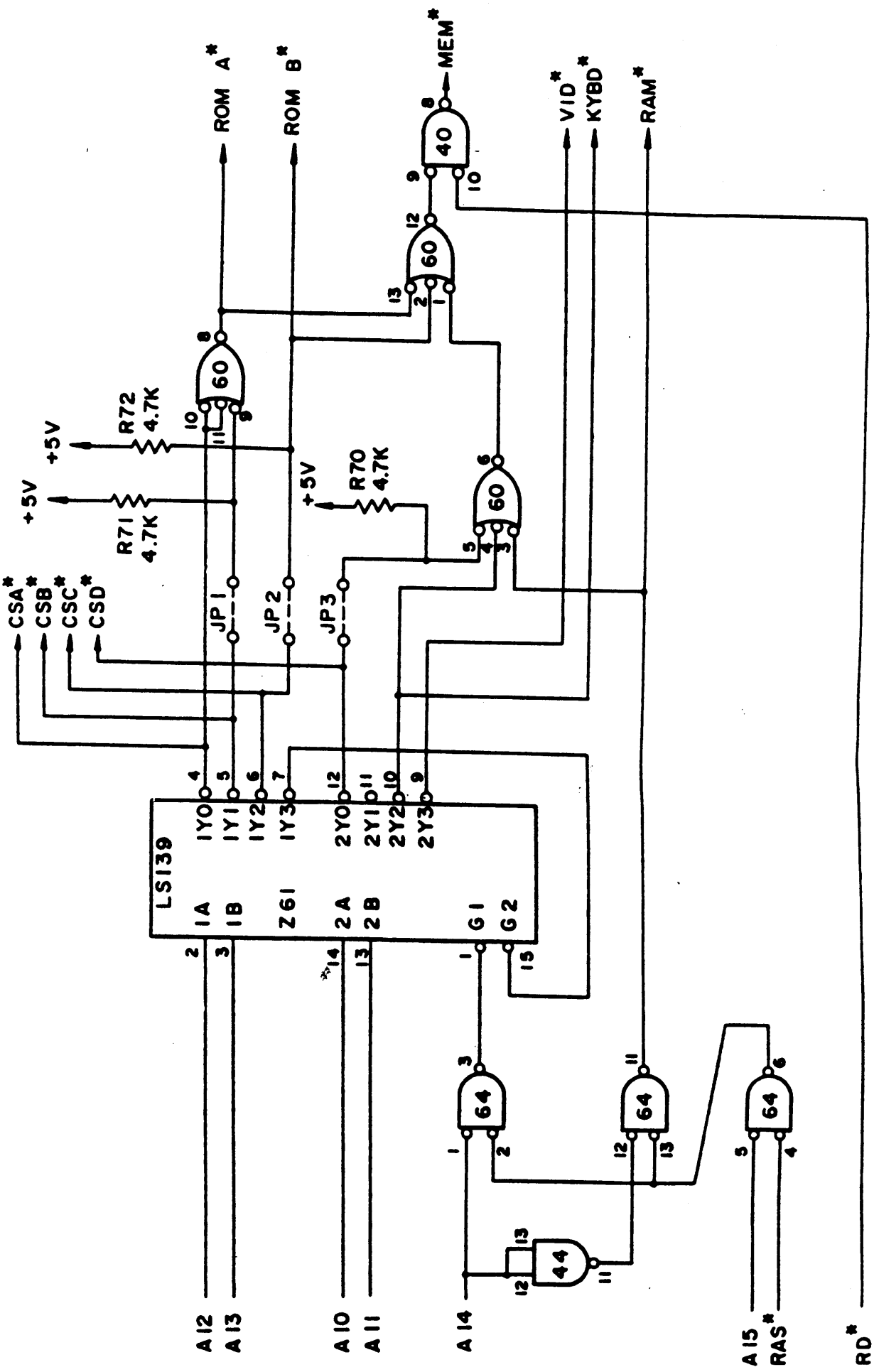
TRS-80 Amerikaanse model I. Schema. Sheet 2 B. 10

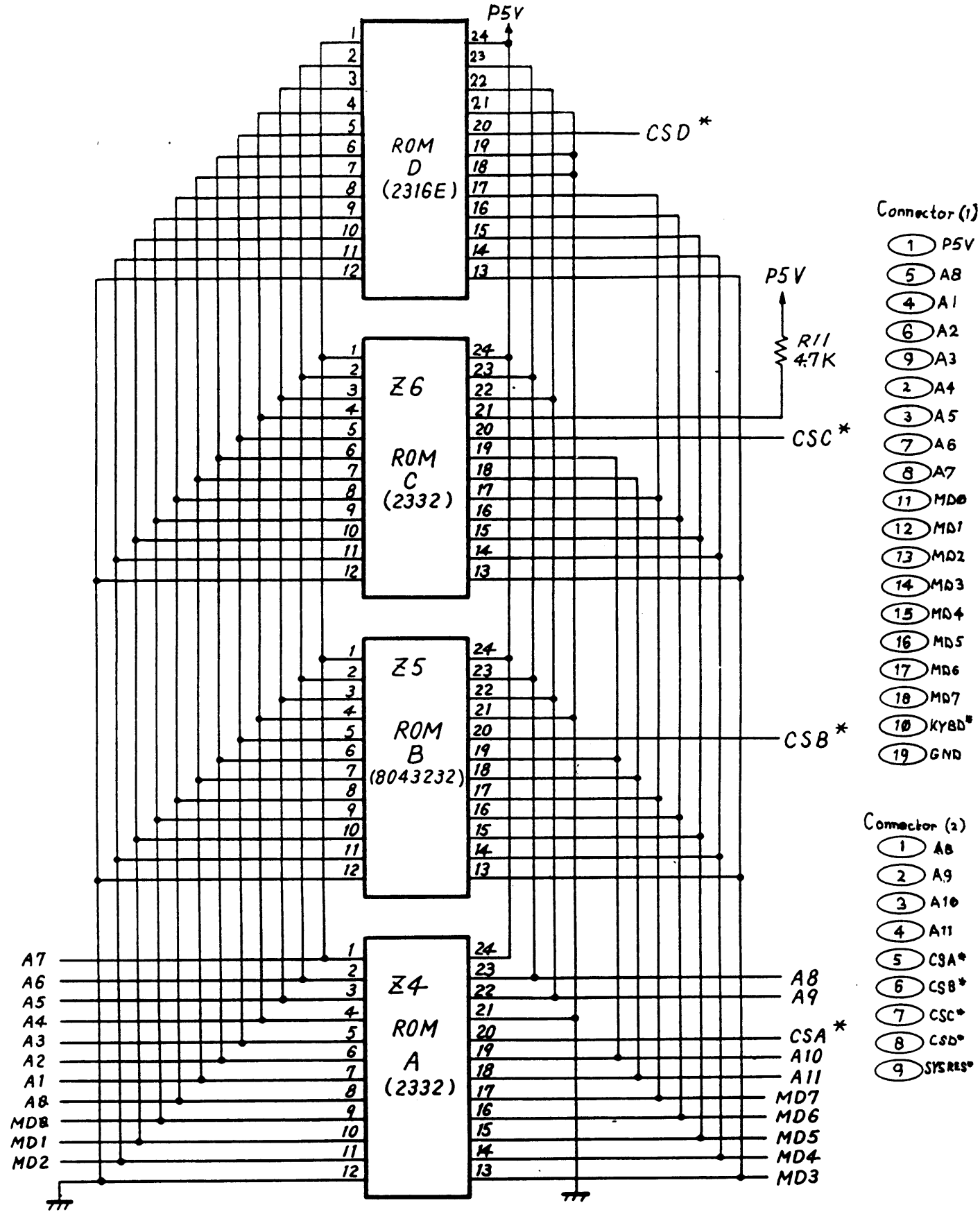


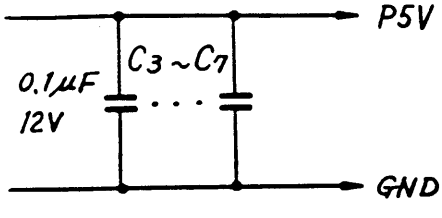
TRS-80 Amerikaanse model I. Schema. Sheet 2 C. 11


CASSIN
CR5 IN4148
R34 470K
R36 360K
R37 560K
R35 470K
C24 220pF
R33 360K
Z4 LM3900
C25 220pF
CR4 IN4148
C07
R67 100Ω
R24 680KΩ
R25 1.8MΩ
R32 10K
+5V
R42 1MEG
R41 470K
C5 10µF 16V
R31 10
C30
C6 100µF 16V
CR6 IN4148
CR7 IN4148
R45 470K
R38 470K
C39 0.1µF
Z24 74LS132
Z44 74LS367
D6
D7
FROM SHEET 1
A7-36
A6-38
A5-35
A4-41
A3-34
A2-40
A1-27
A0-25
A5
A4
SYNC
A7
A6
HI COMP
Z5
Z52 74LS04
Z54 74LS30
FE*
Z36 74LS32
IN*
OUT*
Z25 74LS32
INSIG*
OUTSIG*
R44 10K
A3
A2
A1
A0
MODESEL

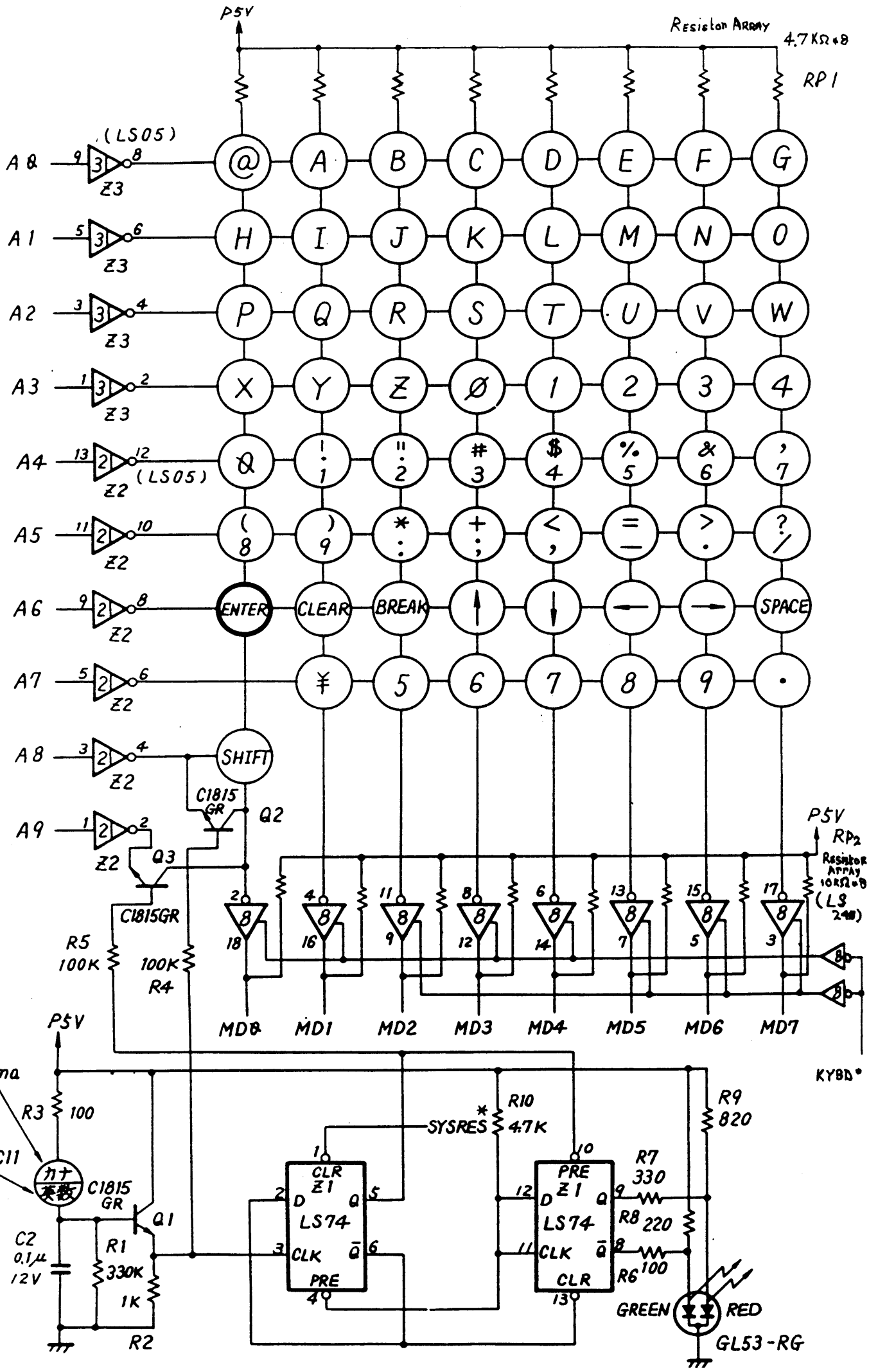

+12V
R16 1.2K
Q6 MJE34
R18 5.6Ω 3W
R17 2K
R13 2.2K
R10 1K
R12 3.3K
C11 10µF 16V
C15 0.01µF DISC 25V
0.1µF 50V (4 PLACES) C28, C30 C32, C34
C8 2200µF 35V
Z2 723C
R14 12K
R15 1.5K
C13 470pF
R1 68 1/2W
Q2 2N6594
R4 0.33Ω 2W
Q3 MJE29 OR TIP29A
R2 2.7K
R3 750Ω
FRONT VIEW
J1
C9 10,000µF 16V
Z1 723C
R9 3.3K
C12 470pF
R7 1.2K
R6 1.2K
R5 1K
R11 3.3K
39 +5V
CR8 MDA202
Q5 MPS53906
R8 100K
C10 10µF 16V
C14 0.01µF 25V
CR1 IN4735 10%
R19 220Ω 1/2W
S1
-5V
C1 220µF 16V
C4 10µF 16V
C3 0.01µF DISC
CR2 IN5231 3%
0.1µF 12V (4 PLACES) C16-C19
8
29
37
0.1µF 12V (32 PLACES) C22,C23,C29, C31,C33,C35-C38, C40,C41,C44-C56
+5V
R59 4.7K
P54 7.5K
CASSOUT
C20
R55 7.5K
R53 1.2K
CR9 IN982
CR10 IN982
FRONT VIEW
J3
D0
D1
D2
CLR
CLK
Z59 74LS175
C21
C22
R56 220K
+5V
CR3 IN4148 RELAY
K1 56-1051-10
CASSETTE I/O
Z41
1/2 75452
Z23
74LS32
74LS32
SPARE GATES

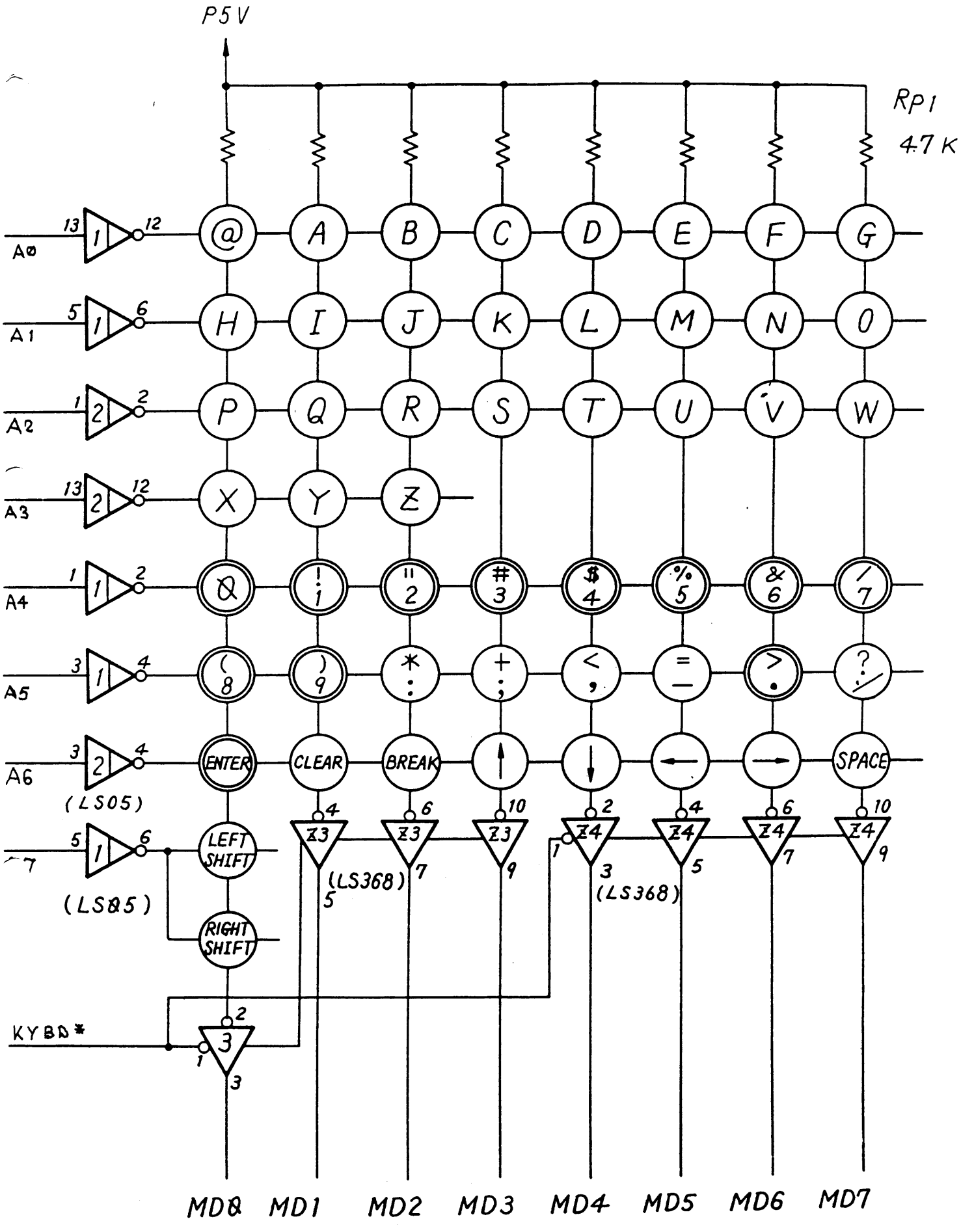

ROM A*
ROM B*
MEM*
VID*
KYBD*
RAM*
40
60
60
60
64
64
64
44
+5V
+5V
+5V
R72 4.7K
R71 4.7K
R70 4.7K
CSA*
CSB*
CSC*
CSD*
JP1
JP2
JP3
LS139
1A
1B
1G
2A
2B
2G
1Y0
1Y1
1Y2
1Y3
2Y0
2Y1
2Y2
2Y3
A12
A13
A10
A11
A14
A15
RAS*
RD*

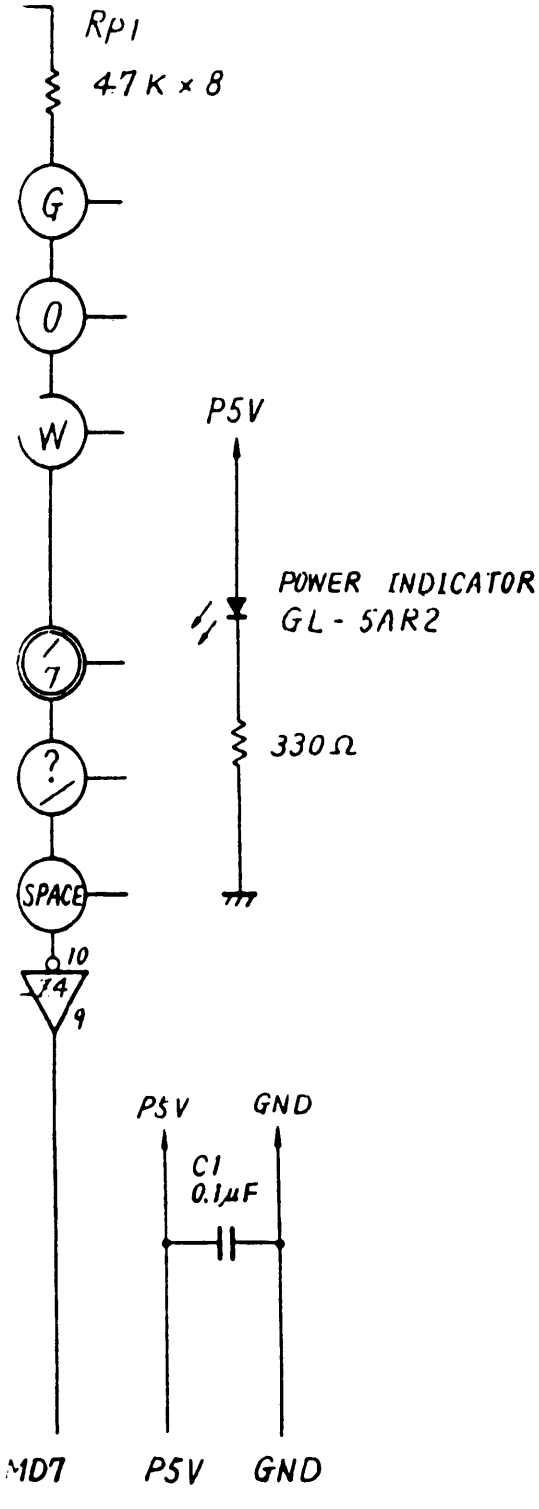




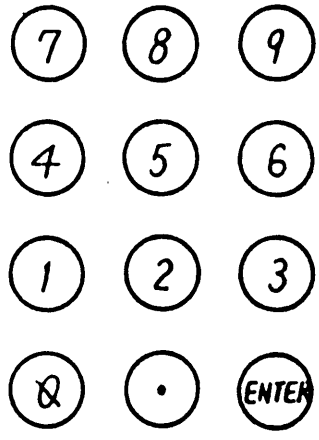
Note : ENTER KEY is Connected Parallel with Main KEY.


P5V
Resistor Array
4.7KΩ×8
RP1
(LS05)
A8
A1
A2
A3
A4
A5
A6
A7
A8
A9
Z3
Z2
@ A B C D E F G
H I J K L M N O
P Q R S T U V W
X Y Z Ø 1 2 3 4
Q ! 1 " 2 # 3 $ 4 % 5 & 6 ' 7
(8) 9 * : + ; < , = - > . ? /
ENTER
CLEAR
BREAK
SPACE
¥ 5 6 7 8 9 .
SHIFT
C1815 GR
Q2
Q3
C1815GR
P5V
RP2
Resistor Array 10KΩ×8
(LS 240)
R5 100K
100K R4
MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7
KYBD*
kana
R3 100
ASCII
カナ 英数
C1815 GR
Q1
C2 0.1μ 12V
R1 330K
1K
R2
SYSRES*
R10 4.7K
CLR Z1 LS74 PRE
PRE Z1 LS74 CLR
R7 330
R8 220
R6 100
R9 820
GREEN
RED
GL53-RG


P5V
RP1
4.7K
A0
A1
A2
A3
A4
A5
A6
(LS05)
7
(LS05)
KYBD*
@ A B C D E F G
H I J K L M N O
P Q R S T U V W
X Y Z
Q ! 1 " 2 # 3 $ 4 % 5 & 6 ' 7
(8) 9 * : + ; < , = - > . ? /
ENTER CLEAR BREAK SPACE
LEFT SHIFT
RIGHT SHIFT
Z3 (LS368)
Z4 (LS368)
MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7



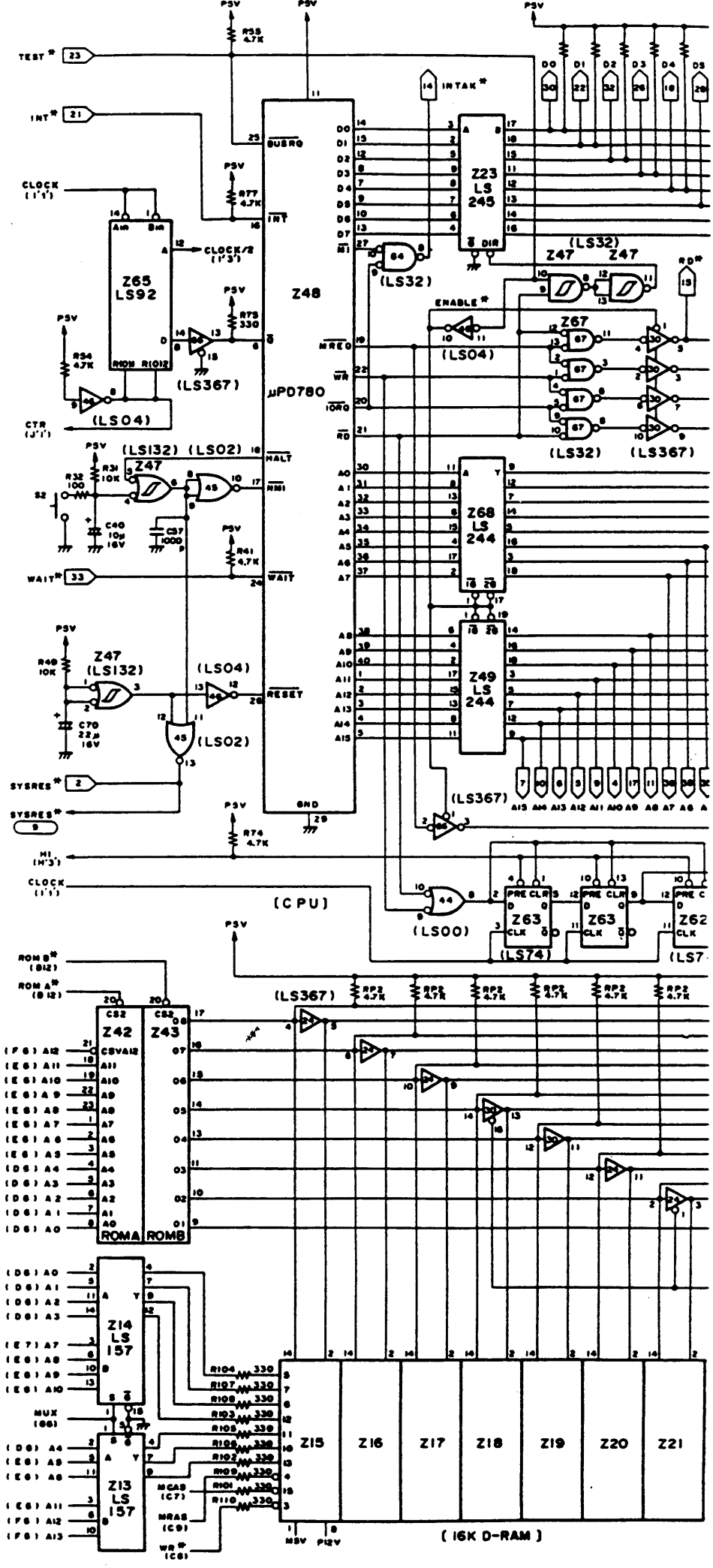
TEN KEY



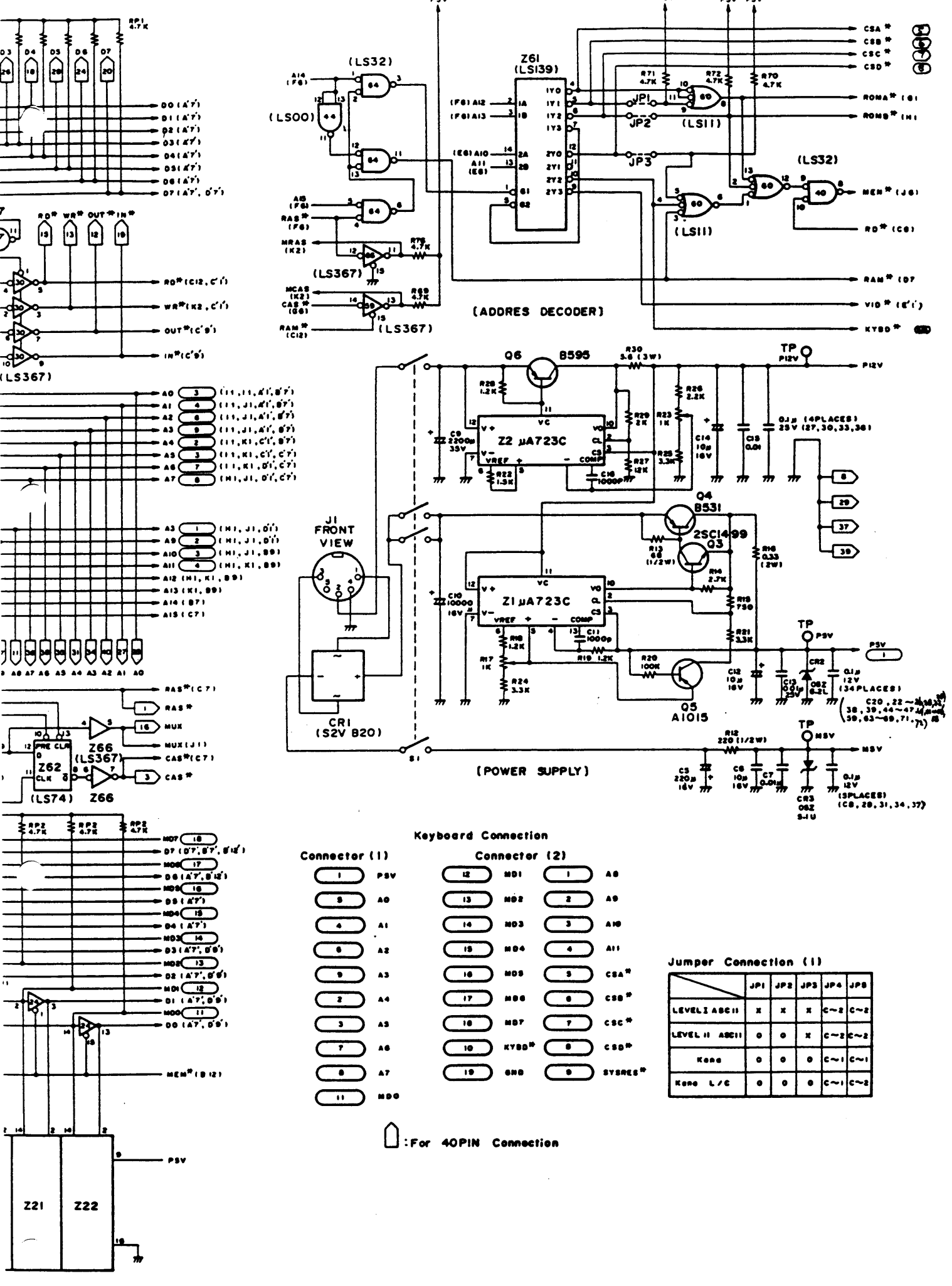
Connector 1

1	P5ST	12	MD1
5	A0	13	MD2
4	A1	14	MD3
6	A2	15	MD4
9	A3	16	MD5
2	A4	17	MD6
3	A5	18	MD7
7	A6	10	KYBD*
8	A7	19	GND
11	MD0		

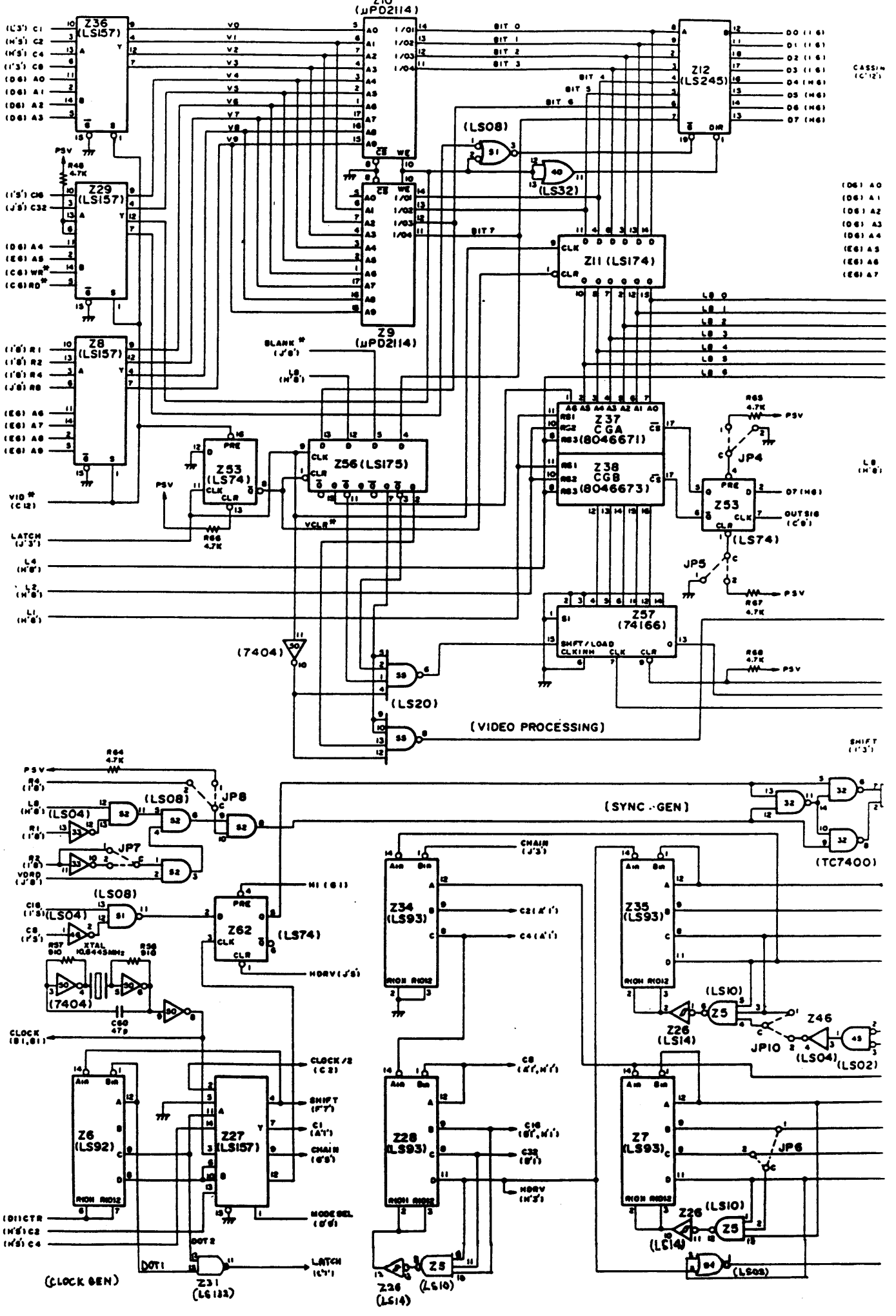
Note : TEN KEY is Connected Parallel with Main KEY.



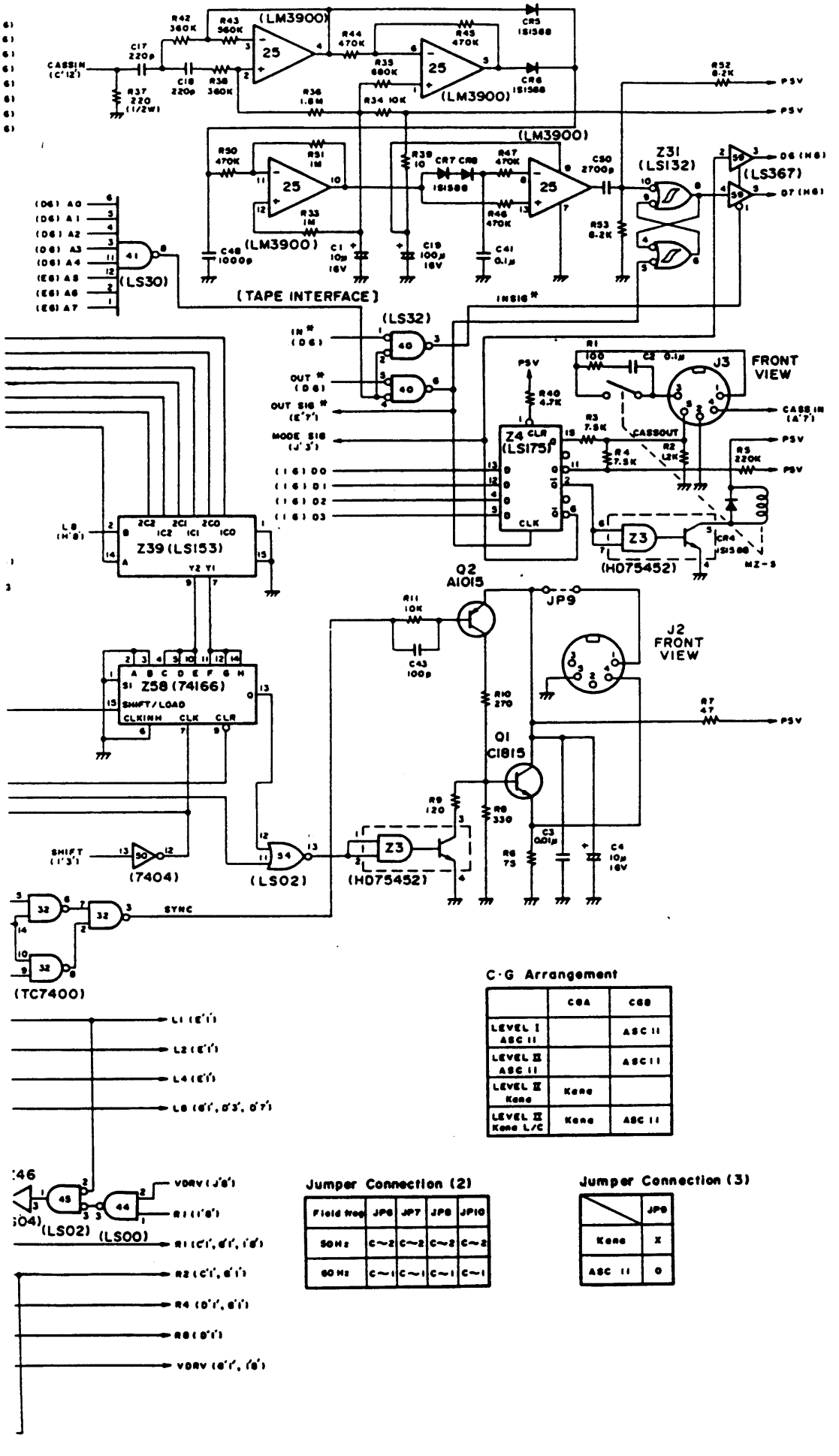
TRS-80 Japanse model I. Schema. Sheet 1 A. 19



	JP1	JP2	JP3	JP4	JP5
LEVEL I ASCII	X	X	X	C~2	C~2
LEVEL II ASCII	0	0	X	C~2	C~2
Kana	0	0	0	C~1	C~1
Kana L/C	0	0	0	C~1	C~2



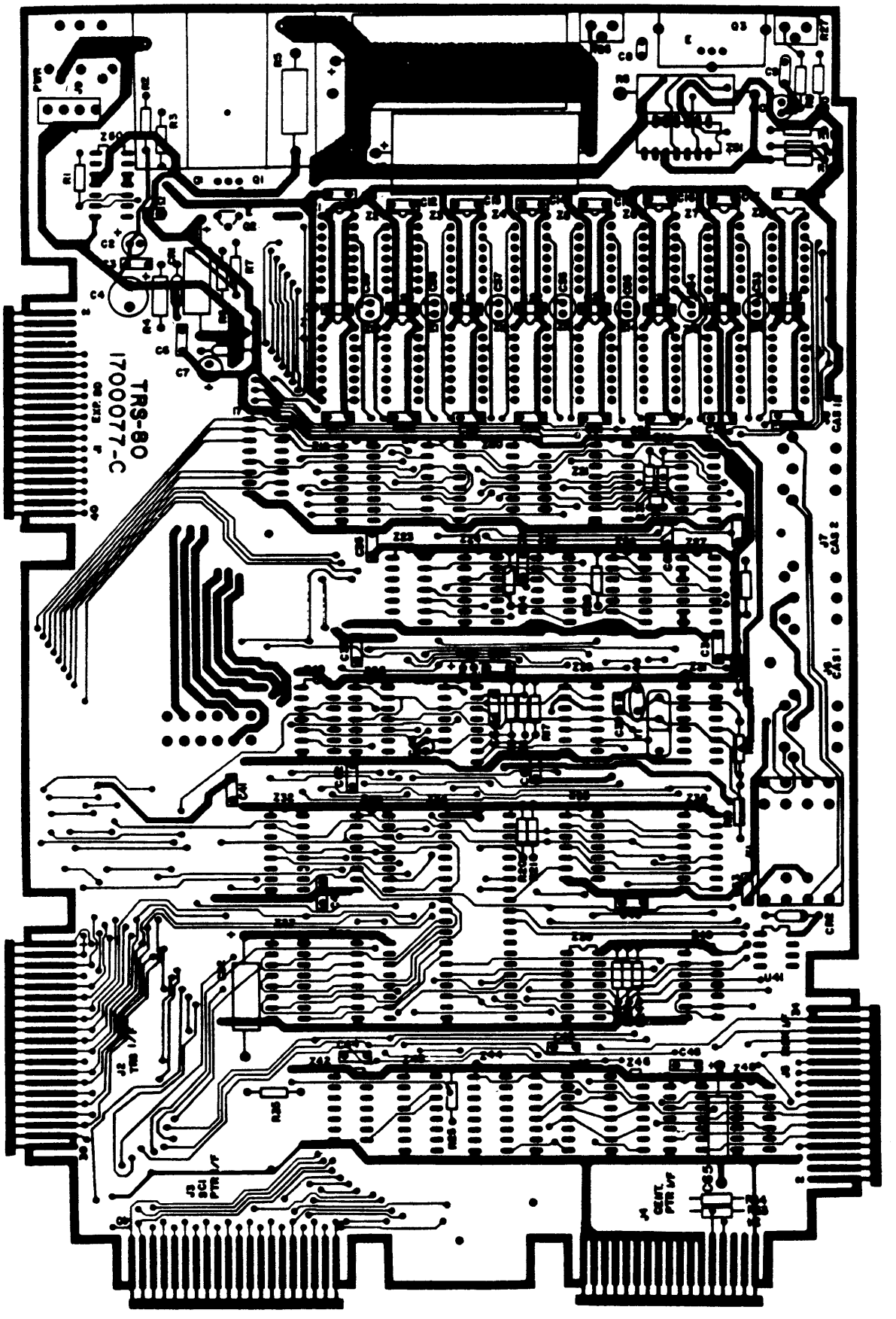
TRS-80 Japanse model I. Schema. Sheet 2 A.



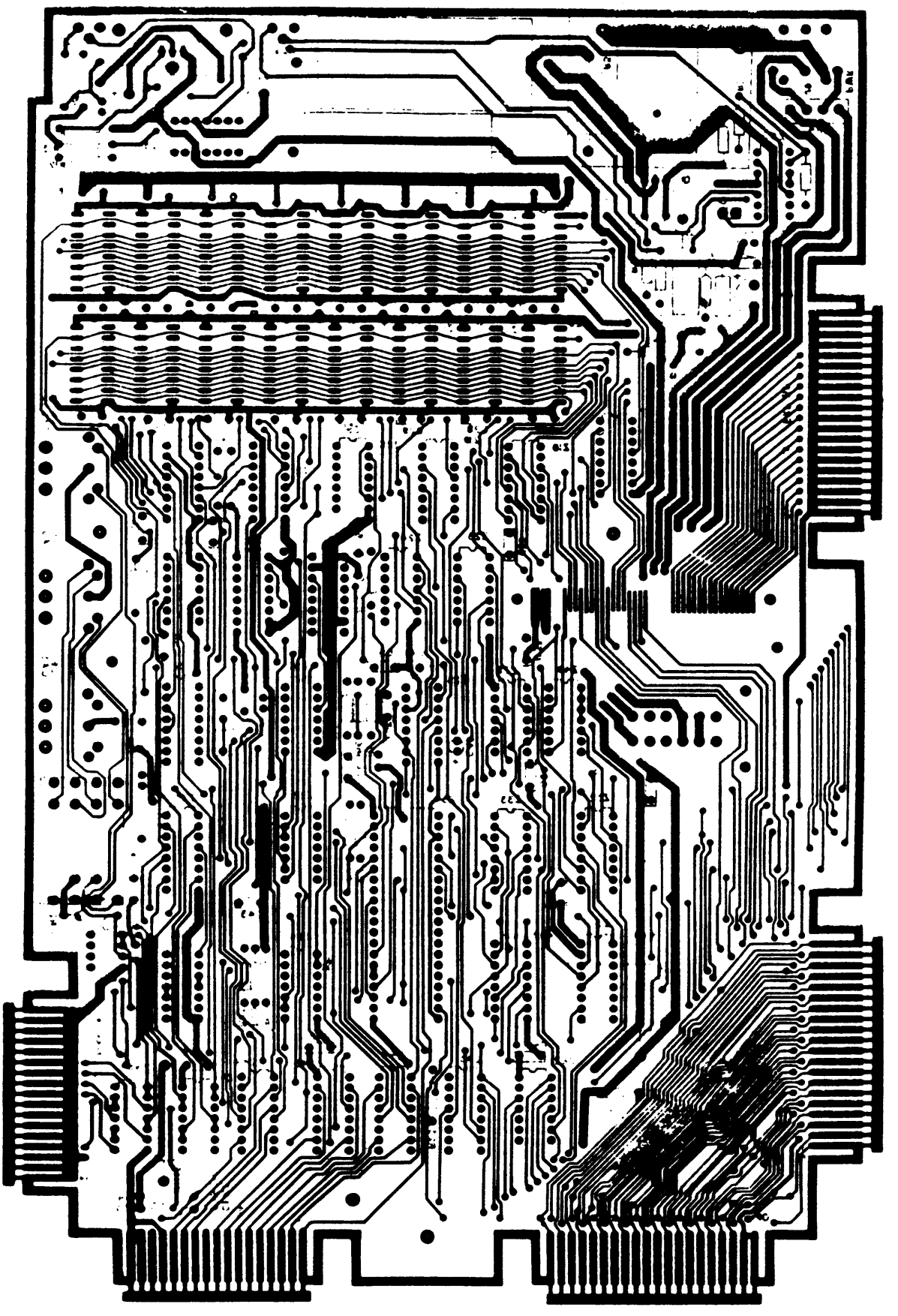
	CGA	CGB
LEVEL I ASC II		ASC II
LEVEL II ASC II		ASC II
LEVEL II Kana	Kana	
LEVEL II Kana L/C	Kana	ASC II

Field freq	JP6	JP7	JP8	JP10
50Hz	C~2	C~2	C~2	C~2
60 Hz	C~1	C~1	C~1	C~1

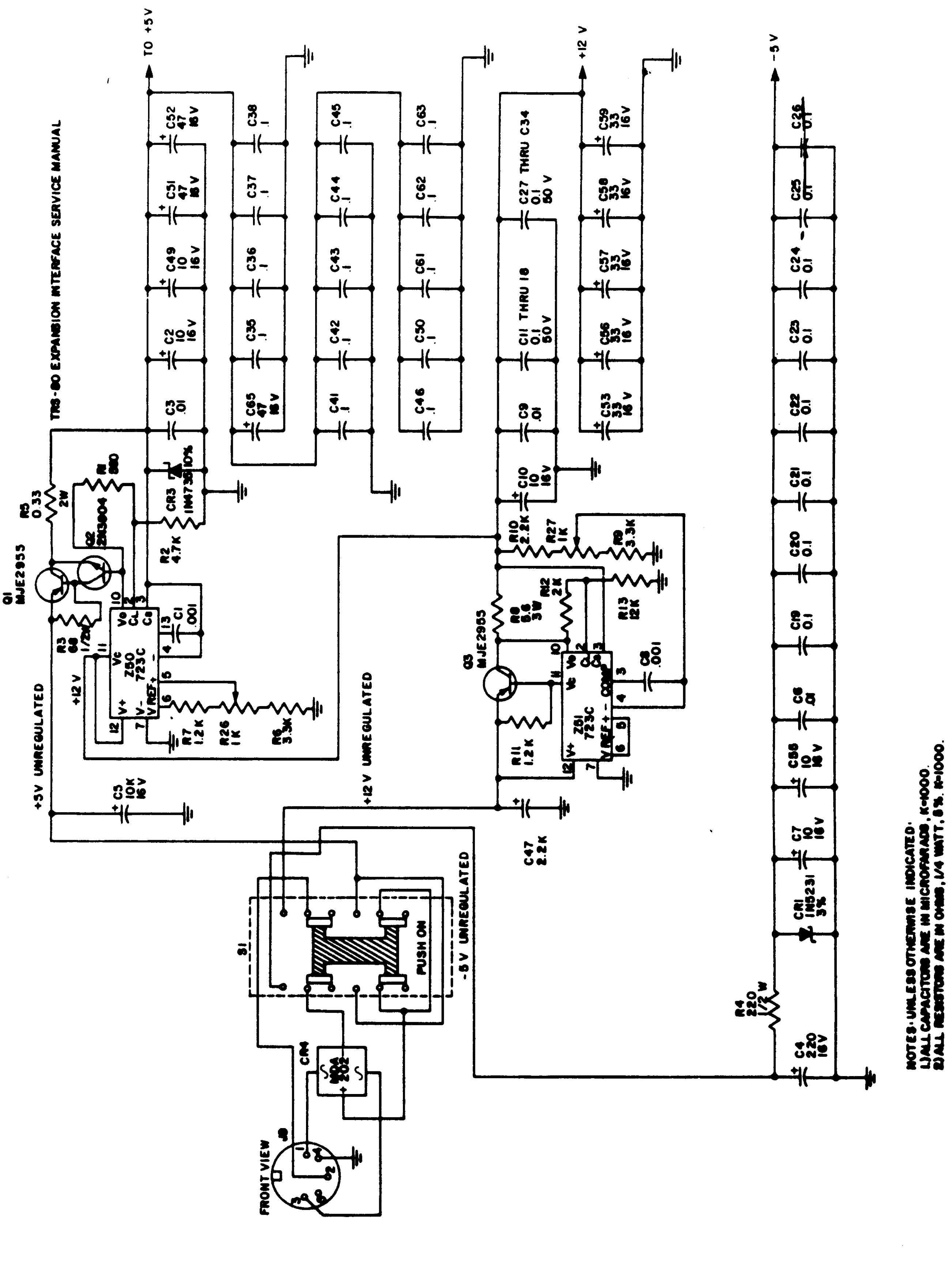
	JP9
Kana	X
ASC II	0

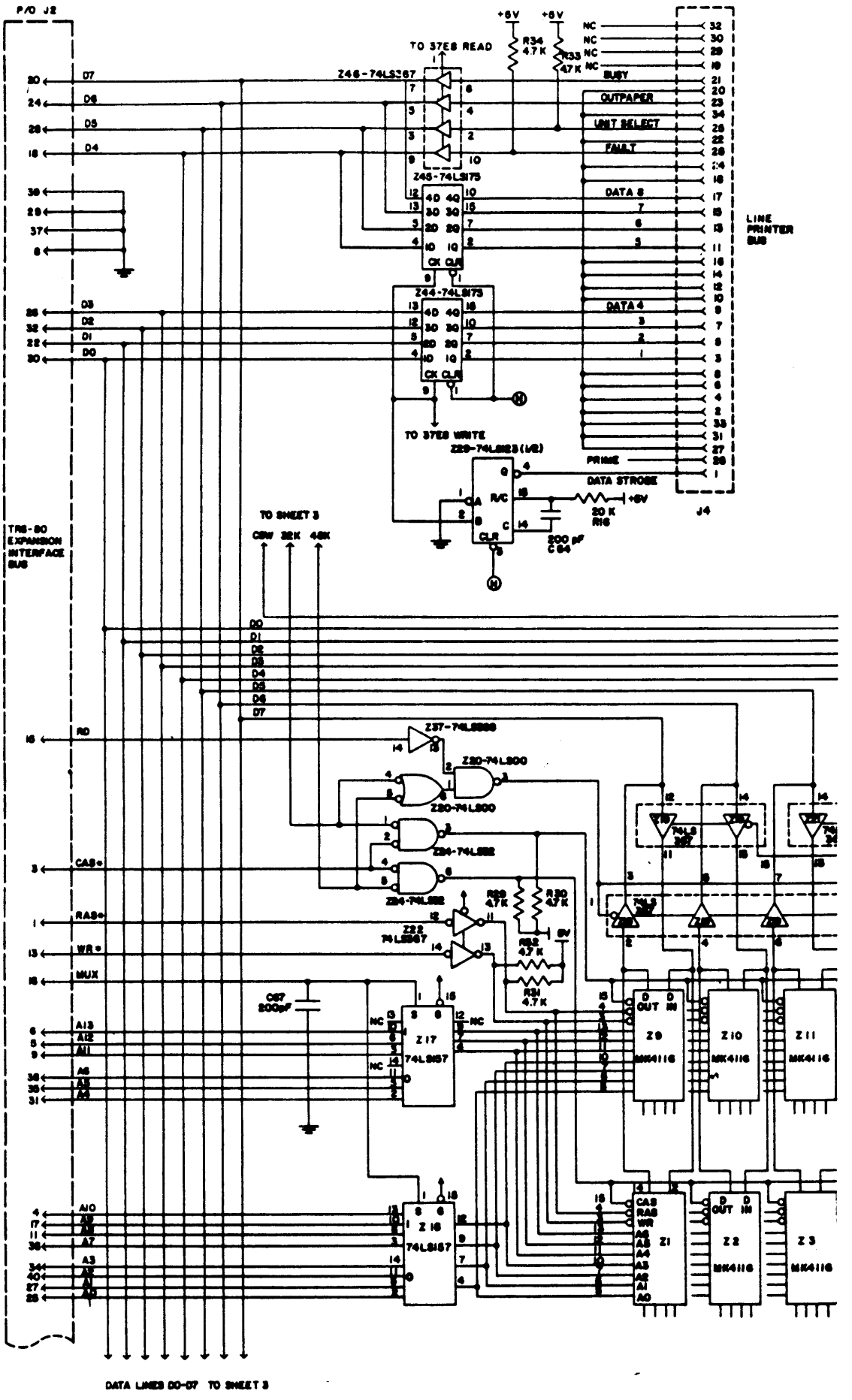


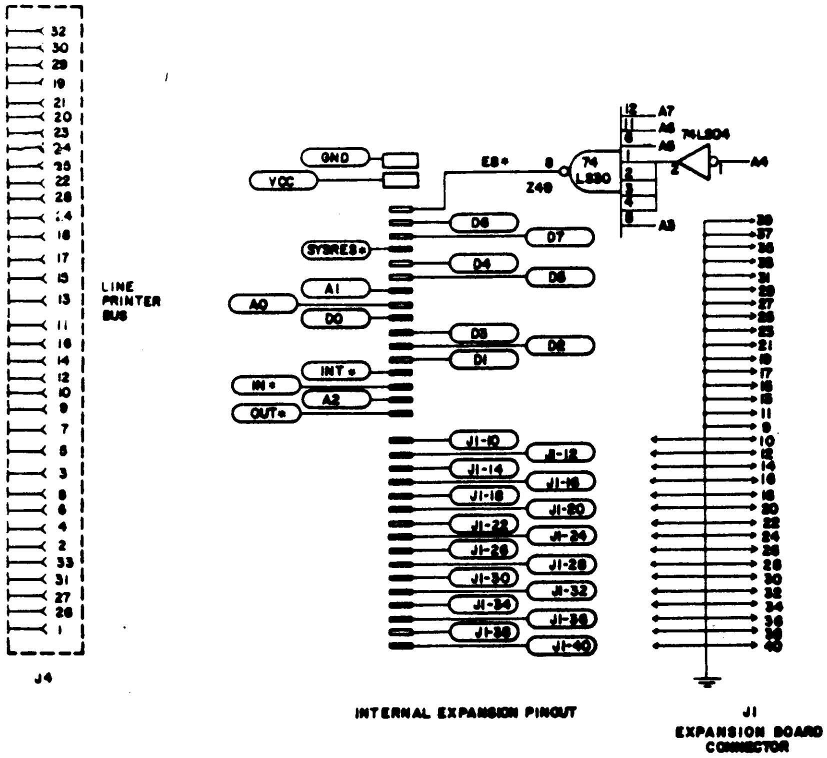
TRS-80 Oude Exp.int. Print layout (boven aanzicht). 23

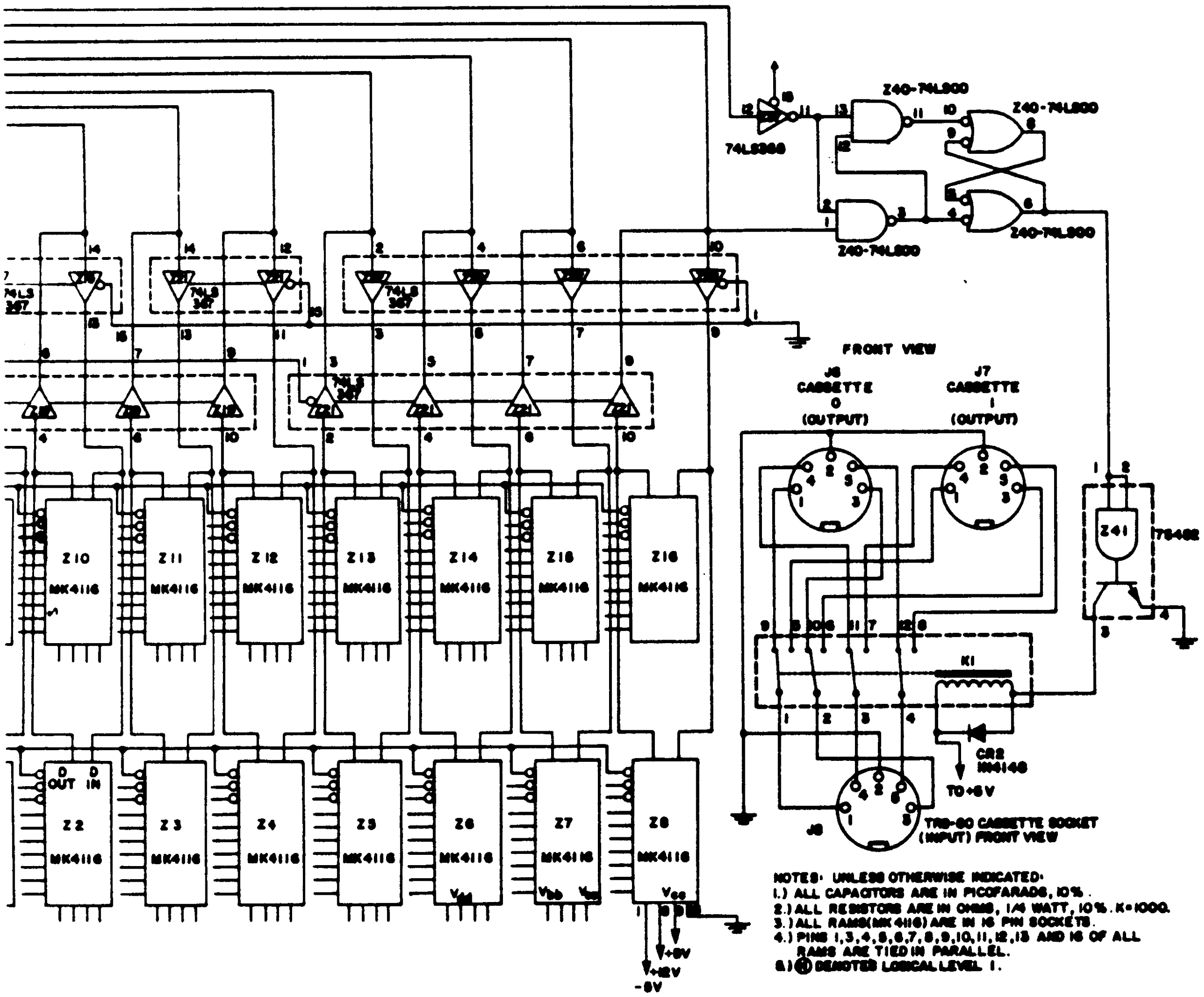


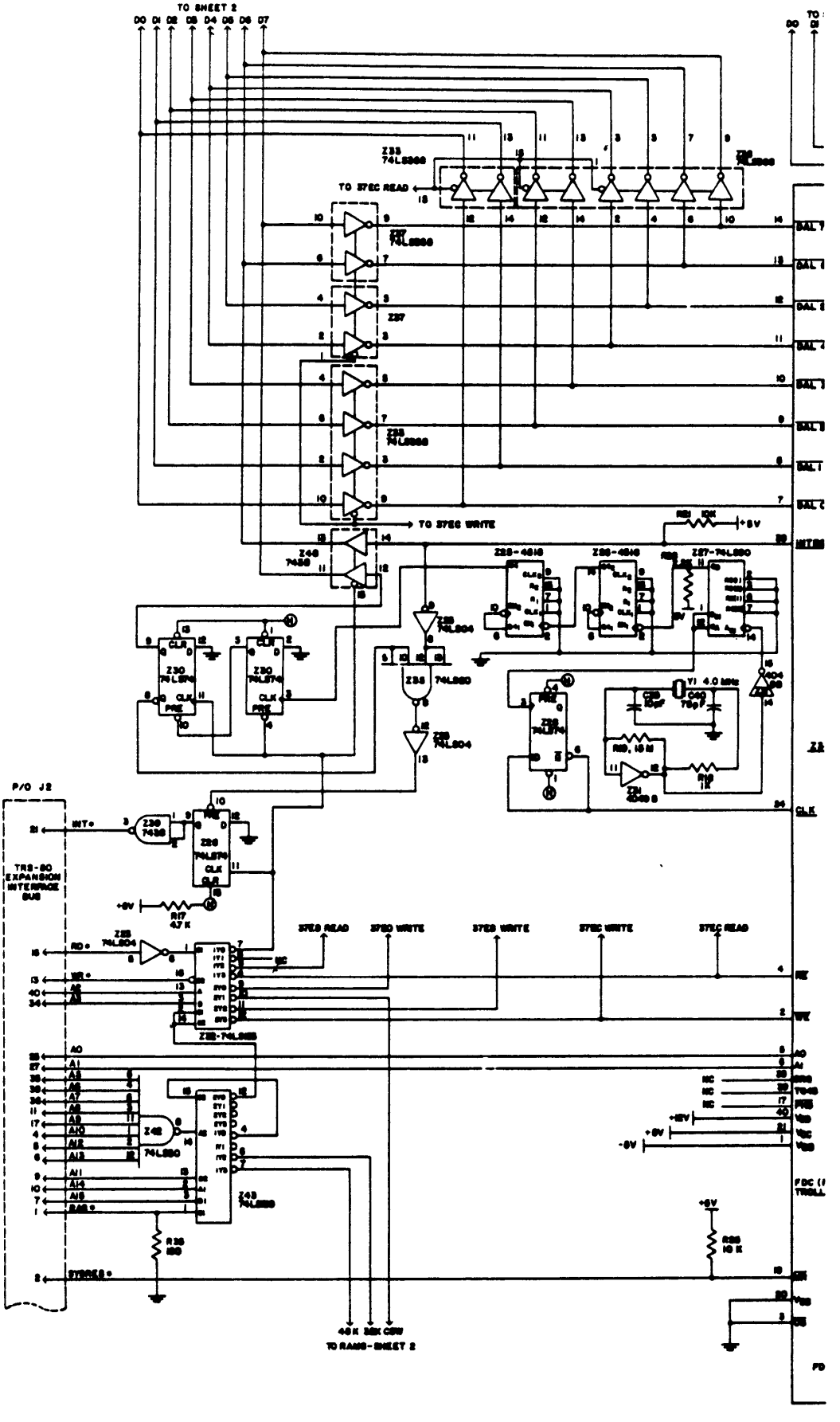
TRS-80 Oude Exp.int. Print layout (bodem aanzicht). 24

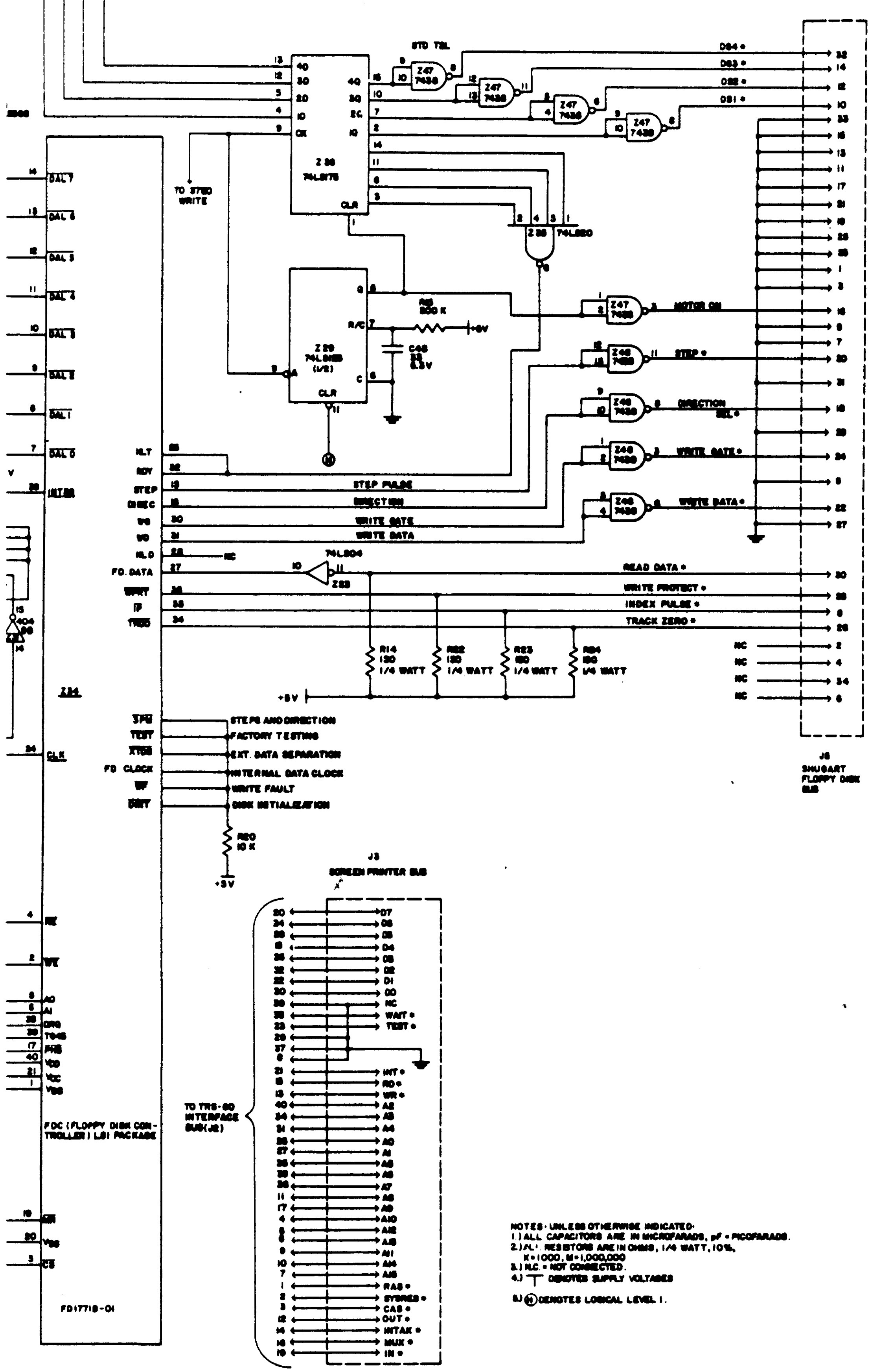

TRS-80 EXPANSION INTERFACE SERVICE MANUAL
TO +5V
+12 V
-5 V
+5V UNREGULATED
+12 V UNREGULATED
-5 V UNREGULATED
PUSH ON
FRONT VIEW
Q1 MJE2955
Q2 2N3904
Q3 MJE2955
Z50 723C
Z51 723C
C27 THRU C34 0.1 50 V
C11 THRU 18 0.1 50 V
NOTES: UNLESS OTHERWISE INDICATED:
1.) ALL CAPACITORS ARE IN MICROFARADS, K=1000.
2.) ALL RESISTORS ARE IN OHMS, 1/4 WATT, 5%, K=1000.


P/O J2
TO 37E8 READ
Z46-74LS367
Z45-74LS175
Z44-74LS175
TO 37E8 WRITE
Z29-74LS123 (1/2)
DATA STROBE
20 K
R16
200 pF
C64
+5V
R34
4.7 K
R33
47 K
BUSY
OUTPAPER
UNIT SELECT
FAULT
DATA 8
DATA 4
LINE
PRINTER
BUS
J4
TRS-80
EXPANSION
INTERFACE
BUS
TO SHEET 3
CBW 32K 48K
D0
D1
D2
D3
D4
D5
D6
D7
RD
Z37-74LS368
Z30-74LS00
Z30-74LS00
Z24-74LS32
Z24-74LS32
CAS*
RAS*
WR*
MUX
R29
4.7 K
R30
4.7 K
Z22
74LS367
R32
4.7 K
R31
4.7 K
C67
200pF
A13
A12
A11
A6
A5
A4
A10
A9
A8
A7
A3
A2
A1
A0
Z17
74LS157
Z16
74LS157
Z9
Z10
Z11
Z1
Z2
Z3
MK4116
CAS
RAS
WR
A6
A5
A4
A3
A2
A1
A0
D OUT
D IN
DATA LINES D0-D7 TO SHEET 3


LINE PRINTER BUS
J4
GND
VCC
ES*
Z40
74LS30
74LS04
SYSRES*
INT*
IN*
OUT*
INTERNAL EXPANSION PINOUT
J1
EXPANSION BOARD CONNECTOR


Z40-74LS00
74LS368
FRONT VIEW
J6
CASSETTE
0
(OUTPUT)
J7
CASSETTE
1
(OUTPUT)
Z41
75452
K1
CR2
1N4148
TO +5V
J8
TRS-80 CASSETTE SOCKET
(INPUT) FRONT VIEW
Z10
Z11
Z12
Z13
Z14
Z15
Z16
Z2
Z3
Z4
Z5
Z6
Z7
Z8
MK4116
D OUT
D IN
+5V
+12V
-5V
NOTES: UNLESS OTHERWISE INDICATED:
1.) ALL CAPACITORS ARE IN PICOFARADS, 10%.
2.) ALL RESISTORS ARE IN OHMS, 1/4 WATT, 10%. K=1000.
3.) ALL RAMS(MK4116) ARE IN 16 PIN SOCKETS.
4.) PINS 1,3,4,5,6,7,8,9,10,11,12,13 AND 16 OF ALL RAMS ARE TIED IN PARALLEL.
5.) ① DENOTES LOGICAL LEVEL 1.

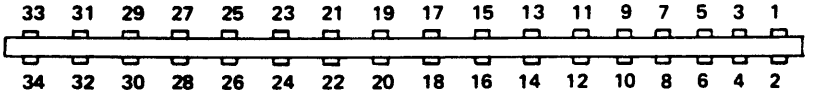

TO SHEET 2
D0 D1 D2 D3 D4 D5 D6 D7
TO 5YEC READ
TO 5YEC WRITE
5YEC READ
5YEC WRITE
5YEC WRITE
5YEC WRITE
5YEC READ
P/O J2
TRS-80 EXPANSION INTERFACE BUS
INT*
STROBE*
40K 32K CSW
TO RAM80-SHEET 2
+8V
-8V
+12V


TO SHEET 2
D0 D1 D2 D3
Z36
74LS175
Z47 7438
Z46 7438
Z38 74LS20
Z29
74LS123
(1/2)
R15
300 K
C48
+5V
TO 3790 WRITE
DS4 *
DS3 *
DS2 *
DS1 *
MOTOR ON
STEP *
DIRECTION SEL *
WRITE GATE *
WRITE DATA *
READ DATA *
WRITE PROTECT *
INDEX PULSE *
TRACK ZERO *
STEP PULSE
DIRECTION
WRITE GATE
WRITE DATA
74LS04
R14 150 1/4 WATT
R22 150 1/4 WATT
R23 150 1/4 WATT
R24 150 1/4 WATT
NC
J6
SHUGART FLOPPY DISK BUS
Z34
STEPS AND DIRECTION
FACTORY TESTING
EXT. DATA SEPARATION
INTERNAL DATA CLOCK
WRITE FAULT
DISK INITIALIZATION
R20
10 K
+5V
J3
SCREEN PRINTER BUS
TO TRS-80 INTERFACE BUS(J2)
FDC (FLOPPY DISK CONTROLLER) LSI PACKAGE
FD1771B-01
NOTES: UNLESS OTHERWISE INDICATED:
1.) ALL CAPACITORS ARE IN MICROFARADS, pF = PICOFARADS.
2.) ALL RESISTORS ARE IN OHMS, 1/4 WATT, 10%,
K=1000, M=1,000,000
3.) NC = NOT CONNECTED.
4.) DENOTES SUPPLY VOLTAGES
5.) (H) DENOTES LOGICAL LEVEL 1.

Line Printer Card-Edge Signals

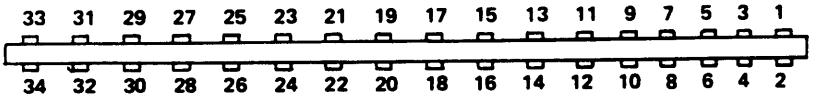
PIN	SIGNAL NAME	DESCRIPTION
1	DATA STROBE*	A 1.0 microsecond pulse used to clock the data from the processor to the printer logic.
2	GND	Signal Ground
3	D1	Input data levels. A high represents a binary one, a low represents a zero. All printable characters (i.e., codes having a one in DATA 6 or DATA 7) are stored in the printer buffer. Control characters (i.e., codes having a zero in both DATA 6 and DATA 7) are used to specify special control functions. These codes are not stored in the buffer except when they specify a print command and are preceded by at least one printable character in that line.
4	GND	
5	D2	
6	GND	
7	D3	
8	GND	
9	D4	
10	GND	
11	D5	
12	GND	
13	D6	
14	GND	
15	D7	
16	GND	
17	D8	
18	GND	
19	NC	Not Connected
20	GND	Signal Ground
21	BUSY	A level indicating that the printer cannot receive data.
22	GND	Signal Ground
23	OUT OF PAPER PE	A level indicating that the printer is out of paper.
24	GND	Signal Ground
25	UNIT SELECT SLCT	A level indicating that the printer is selected.
26	PRIME*	A level which clears the printer buffer and initializes the logic.
27	GND	Signal Ground
28	FAULT*	A level that indicates a printer fault condition such as paper empty, light detect or a deselect condition.
29	NC	Not Connected
30	NC	Not Connected
31	GND	Signal Ground
32	NC	Not Connected
33	GND	Signal Ground
34	GND	Signal Ground

NOTE: All GND signals are common.



Mini Disk Card-Edge Signals

PIN	SIGNAL NAME	DESCRIPTION
1	GND	Signal Ground
2	NC	Not Connected
3	GND	Signal Ground
4	NC	Not Connected
5	GND	Signal Ground
6	NC	Not Connected
7	GND	Signal Ground
8	INDEX PULSE*	Indicates the physical beginning of a track.
9	GND	Signal Ground
10	DSØ*	When active, locks the mini-disk R/W head against the mini-diskette (disk drive no. Ø).
11	GND	Signal Ground
12	DS1*	When active, locks the mini-disk R/W head against the mini-diskette (disk drive no. 1).
13	GND	Signal Ground
14	DS2*	When active, locks the mini-disk R/W head against the mini-diskette (disk drive no. 2).
15	GND	Signal Ground
16	MOTOR ON	Turns ON all drive motors.
17	GND	Signal Ground
18	DIRECTION SEL*	Defines direction of motion the R/W head will take when the STEP line is pulsed.
19	GND	Signal Ground
20	STEP*	Causes the R/W head to move with the direction of motion as defined by DIRECTION SEL.
21	GND	Signal Ground
22	WRITE DATA*	Provides data to be written on diskette.
23	GND	Signal Ground
24	WRITE GATE*	Enables WRITE DATA to be written on the diskette.
25	GND	Signal Ground
26	TRACK ZERO*	A logical zero state indicates that the drive's R/W head is positioned at track zero.
27	GND	Signal Ground
28	WRITE PROTECT*	Gives the user an indication that a write protected diskette is installed.
29	GND	Signal Ground
30	READ DATA*	Provides the "raw data" (clock and data together) as detected by the drive electronics.
31	GND	Signal Ground
32	DS3*	When active, locks the mini-disk R/W head against the mini-diskette (disk drive no. 3).
33	GND	Signal Ground
34	NC	Not Connected

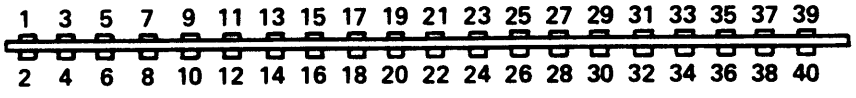


Bus Card-Edge Signals

This card edge duplicates the card edge on the TRS-80 Computer.

PIN	SIGNAL NAME	DESCRIPTION
1	RAS*	Row Address Strobe Output for 16-Pin Dynamic Rams.
2	SYSRES*	System Reset Output, Low During Power Up Initialize or Reset Depressed.
3	NC	No Connection
4	A1Ø	Address Output
5	A12	Address Output
6	A13	Address Output
7	A15	Address Output
8	GND	Signal Ground
9	A11	Address Output
10	A14	Address Output
11	A8	Address Output
12	OUT*	Peripheral Write Strobe Output.
13	WR*	Memory Write Strobe Output.
14	INTAK*	Interrupt Acknowledge Output.
15	RD*	Memory Read Strobe Output.
16	NC	No Connection
17	A9	Address Output
18	D4	Bidirectional Data Bus.
19	IN*	Peripheral Read Strobe Output.
20	D7	Bidirectional Data Bus.
21	INT*	Interrupt Input (Maskable).
22	D1	Bidirectional Data Bus.
23	TEST*	A Logic "Ø" on TEST* Input Tri-States AØ - A15, DØ - D7, WR*, RD*, IN*, OUT*, RAS*, CAS*, MUX*.
24	D6	Bidirectional Data Bus.
25	AØ	Address Output
26	D3	Bidirectional Data Bus.
27	A1	Address Output
28	D5	Bidirectional Data Bus.
29	GND	Signal Ground
30	DØ	Bidirectional Data Bus.
31	A4	Address Bus
32	D2	Bidirectional Data Bus.
33	WAIT*	Processor Wait Input, to Allow for Slow Memory.
34	A3	Address Output
35	A5	Address Output
36	A7	Address Output
37	GND	Signal Ground
38	A6	Address Output
39	+5V	5-Volt Output (Limited Current)
40	A2	Address Output

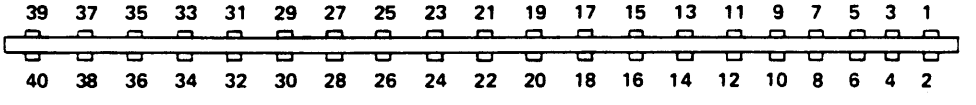
NOTE: * means Negative (Logical "Ø") True Input or Output.

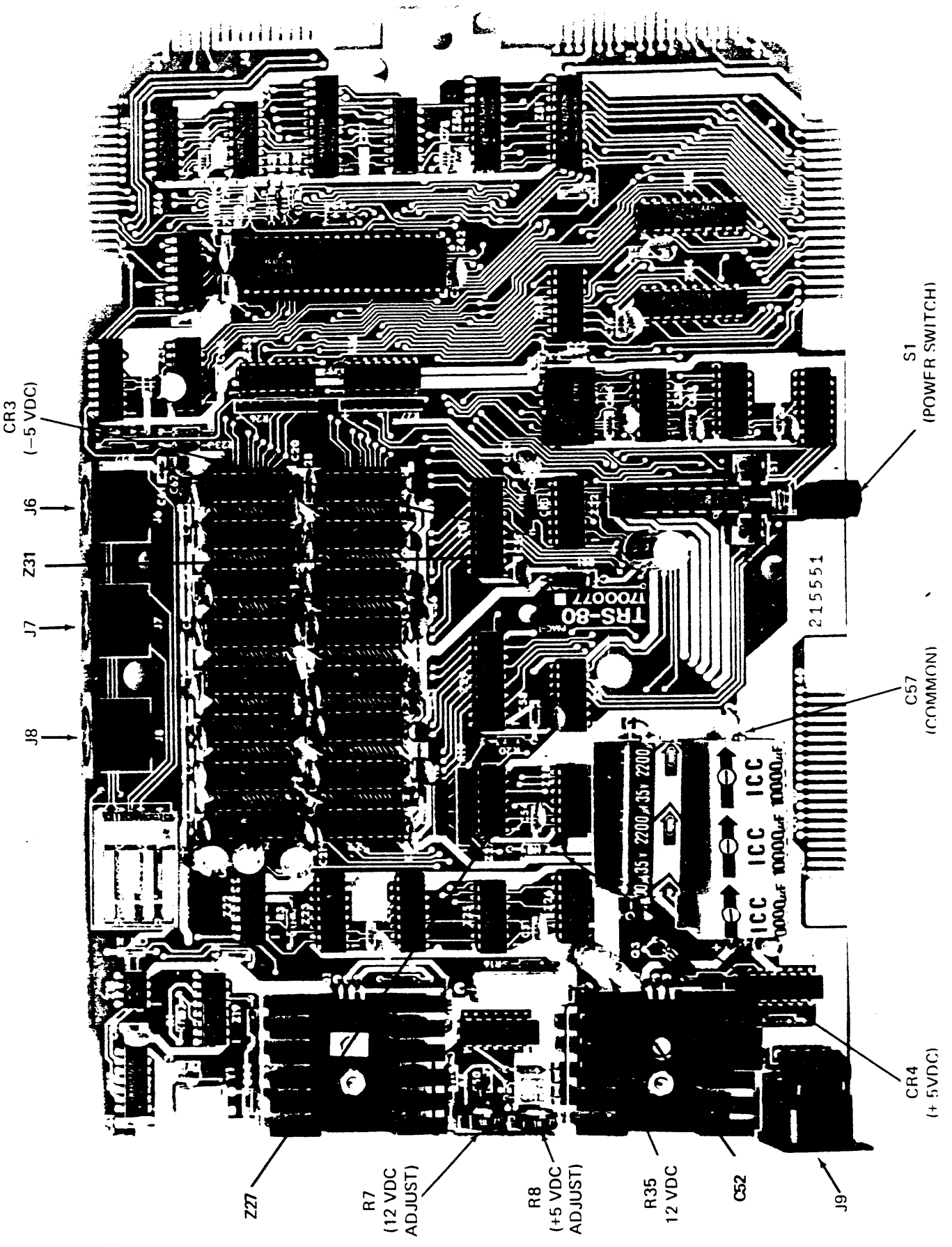


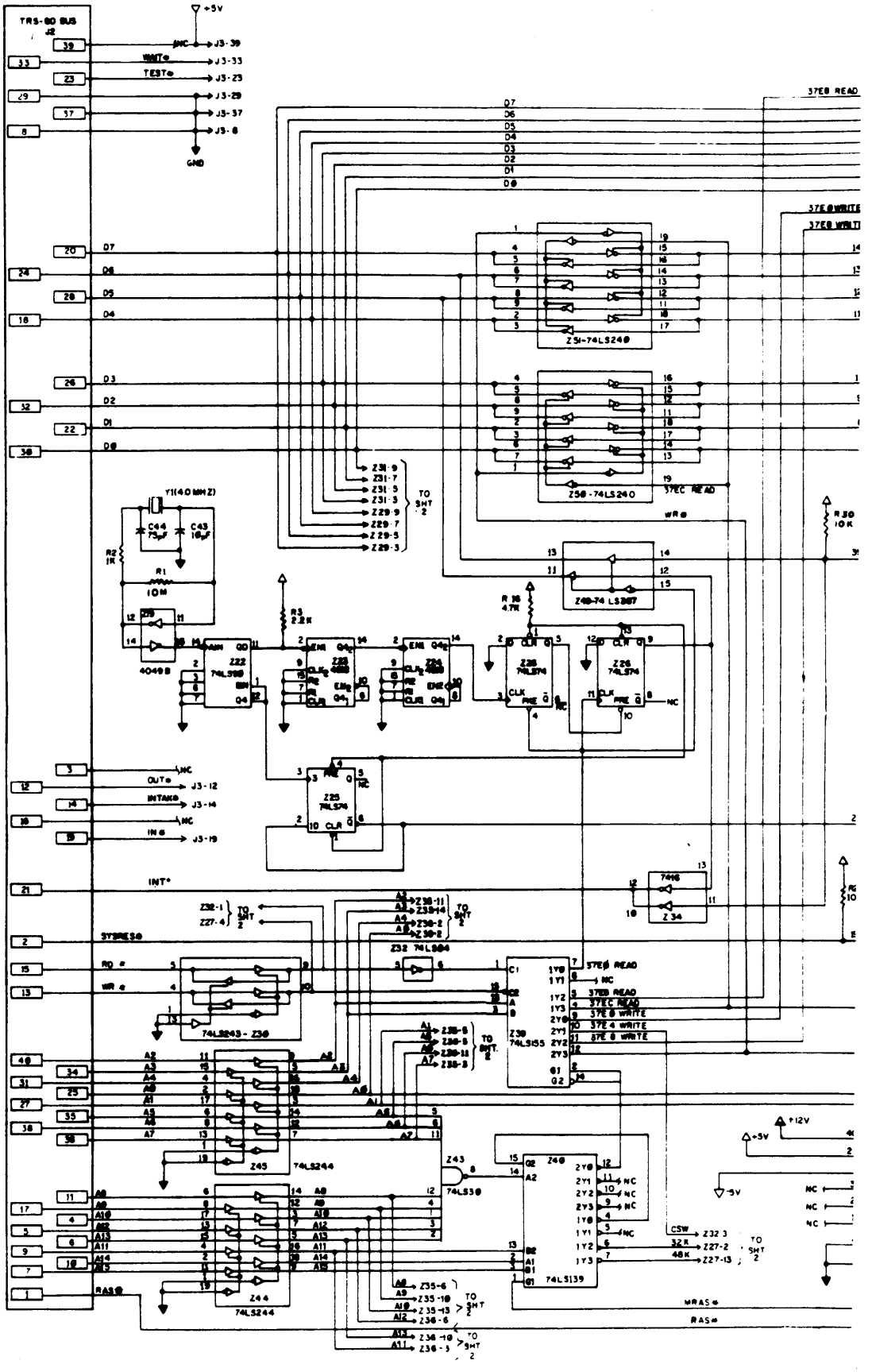
Expansion Board Card-Edge Signals (RS-232C Installed)

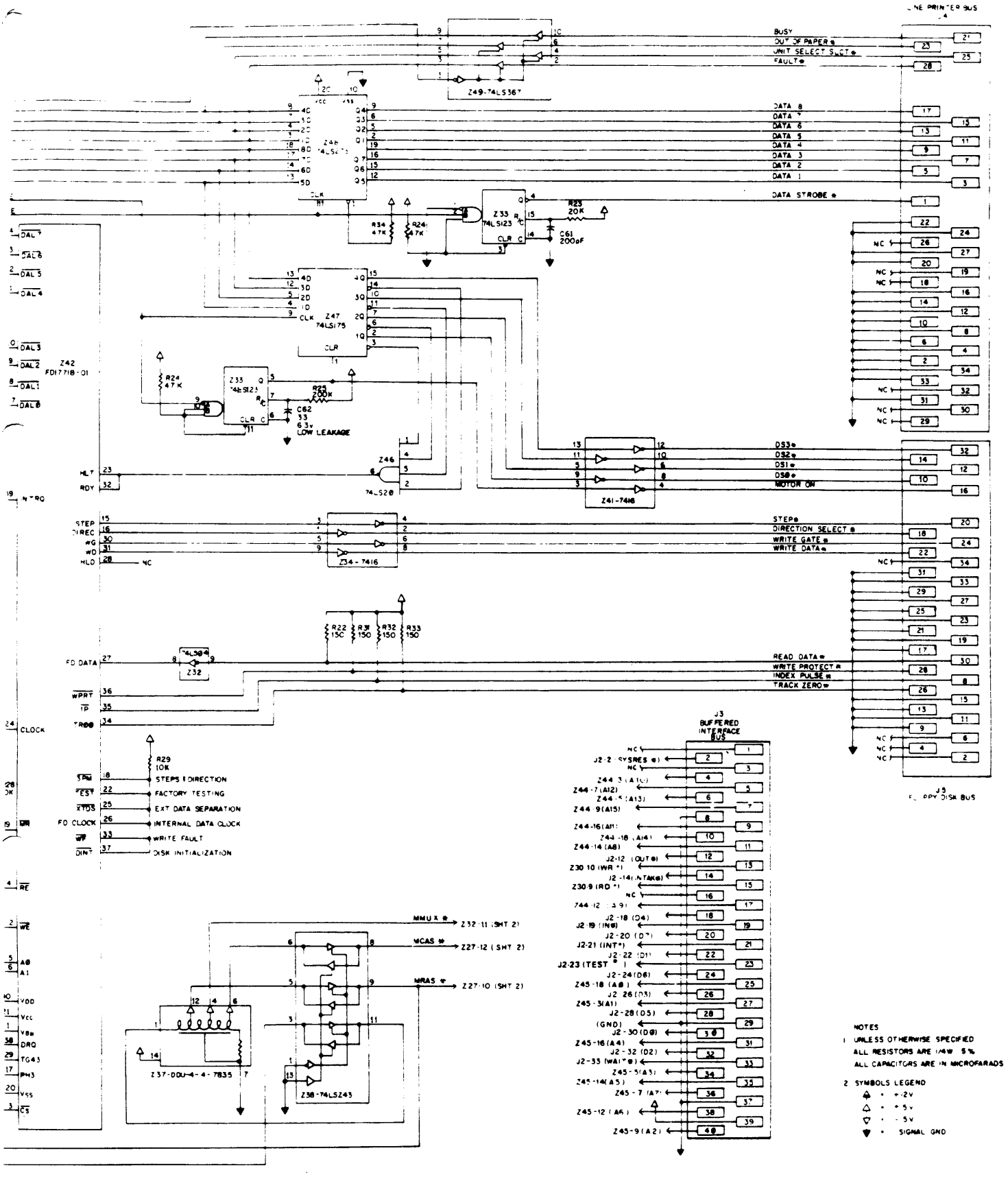
PIN	*SIGNAL NAME	DESCRIPTION
1	GND	Signal Ground
2	NC	
3	GND	Signal Ground
4	NC	
5	GND	Signal Ground
6	NC	
7	GND	Signal Ground
8	NC	
9	GND	Signal Ground
10	---	Internal Expansion Connector - Pin 16 (not used).
11	GND	Signal Ground
12	---	Internal Expansion Connector - Pin 15 (not used).
13	GND	Signal Ground
14	---	Internal Expansion Connector - Pin 14 (not used).
15	GND	Signal Ground
16	PGND	Protective Ground
17	GND	Signal Ground
18	TD	Transmit Data - Signals on this Circuit are sent to remote Equipment.
19	GND	Signal Ground
20	SGND	Signal Ground from Data Communications Equipment.
21	GND	Signal Ground
22	RD	Signals on this Circuit are received from Data Communications (remote) Equipment.
23	GND	Signal Ground
24		Internal Expansion Connector - Pin 9 (not used).
25	GND	Signal Ground
26	---	Internal Expansion Connector - Pin 8 (not used).
27	SIG GND	
28	---	Internal Expansion Connector - Pin 7 (not used).
29	GND	Signal Ground
30	CD	Carrier Detect (Received Line Signal Detector) indicates that the Data Set is receiving a character from a remote Data Set via the Communications Channel.
31	GND	Signal Ground
32	CTS	The Clear to Send signal is generated by the Data Communications Equipment. It indicates whether or not the Data Set (modem) is ready to transmit Data.
33	GND	Signal Ground
34	DTR	The Data Terminal Ready signal to the Data Communications Equipment controls switching of Data Communications Equipment to the Communications Channel.
35	GND	Signal Ground
36	RTS	The Request to Send signal to the Data Communications Equipment controls direction of Data Transmission by the Data Communications Equipment.
37	GND	Signal Ground
38	RI	The Ring Indicator signal from the Data Communications Equipment means that the Data Set is being polled and that the polling service wants to communicate.
39	GND	Signal Ground
40	DSR	Data Set Ready indicates the status of the local Data Set.

* Signal Names used in this chart are those related to Radio Shack's RS-232-C Interface.

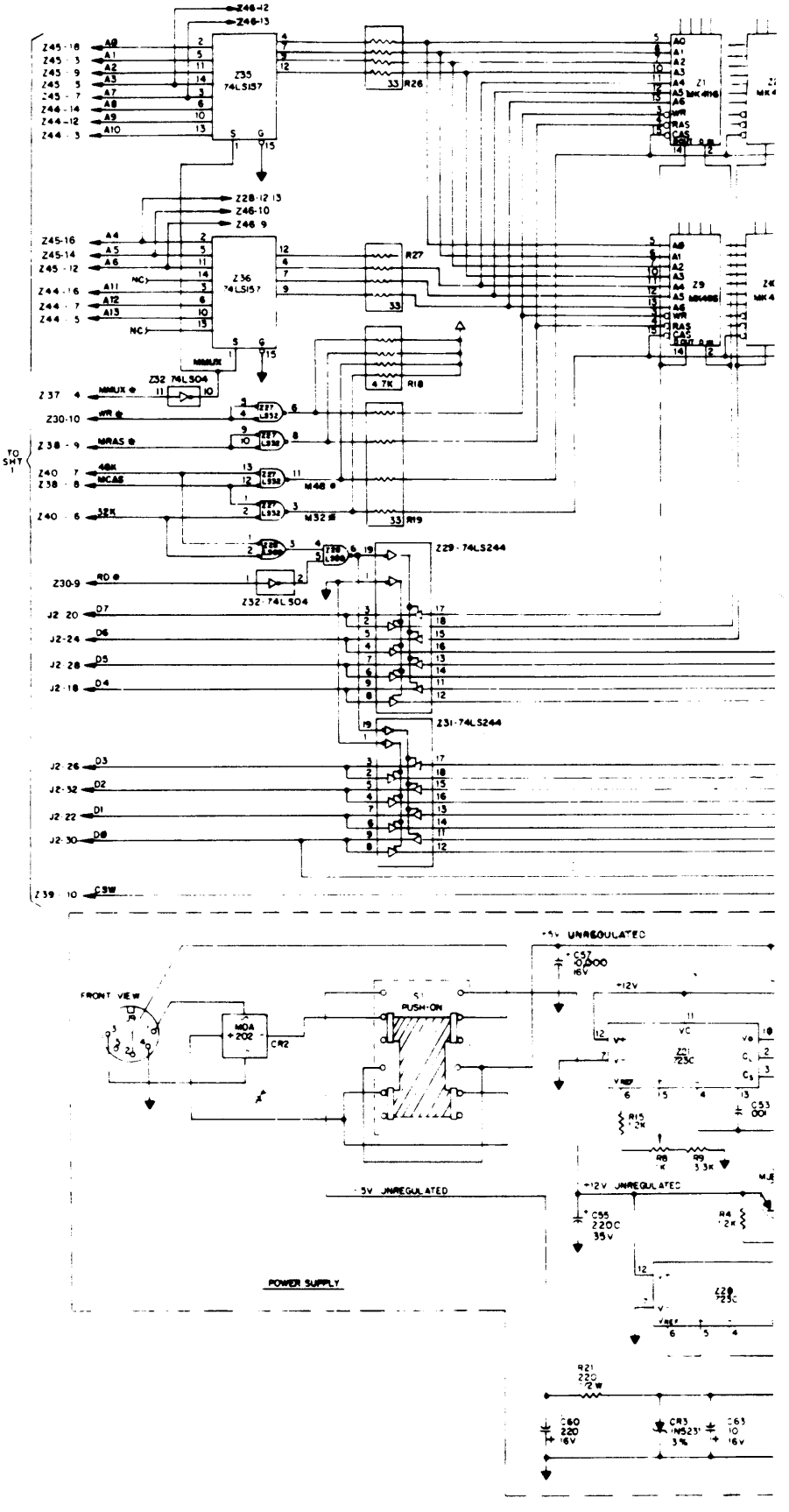


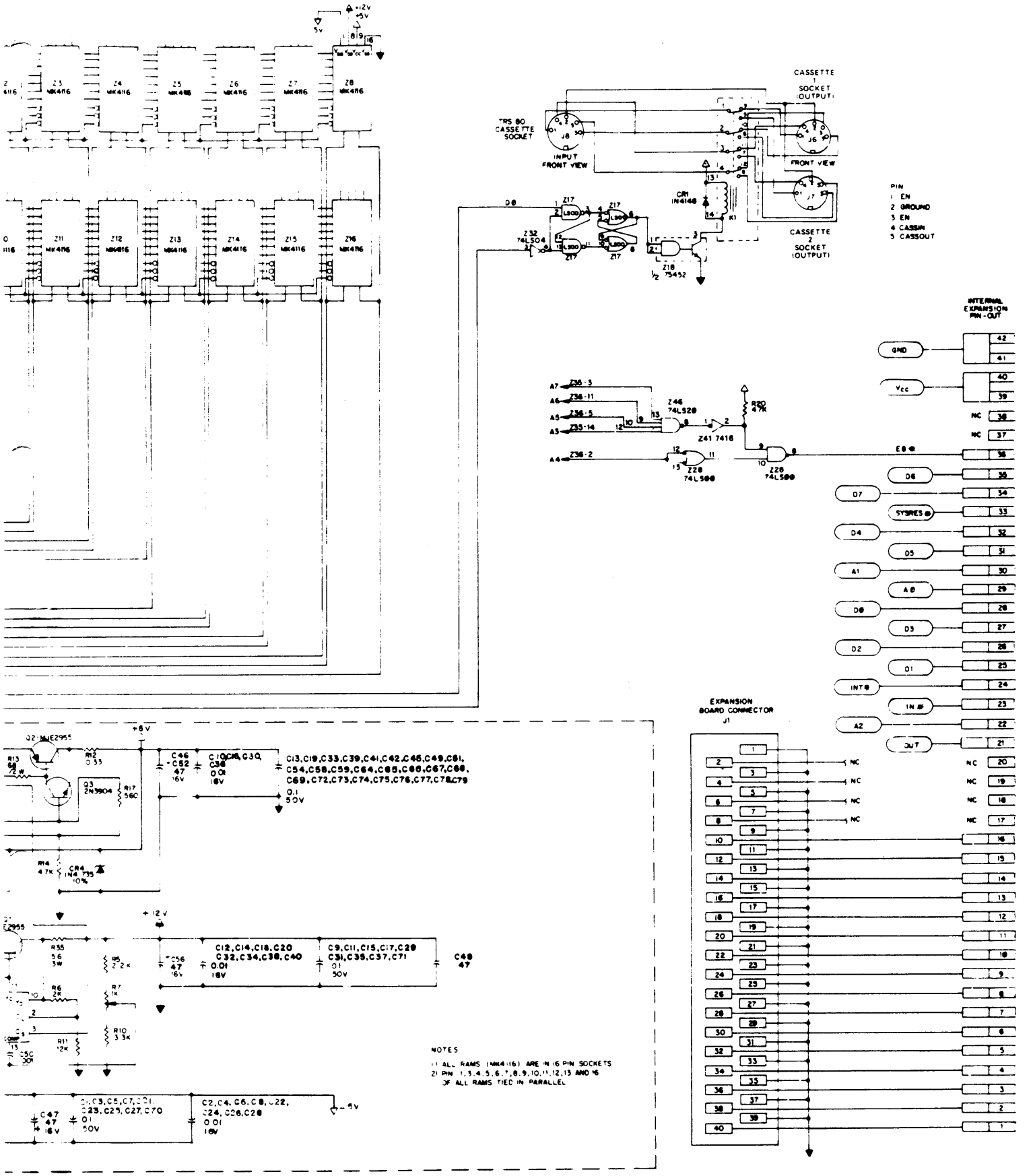

CR3
(-5 VDC)
J6
Z31
J7
J8
S1
(POWER SWITCH)
C57
(COMMON)
CR4
(+5VDC)
Z27
R7
(12 VDC
ADJUST)
R8
(+5 VDC
ADJUST)
R35
12 VDC
C52
J9
TRS-80
215551

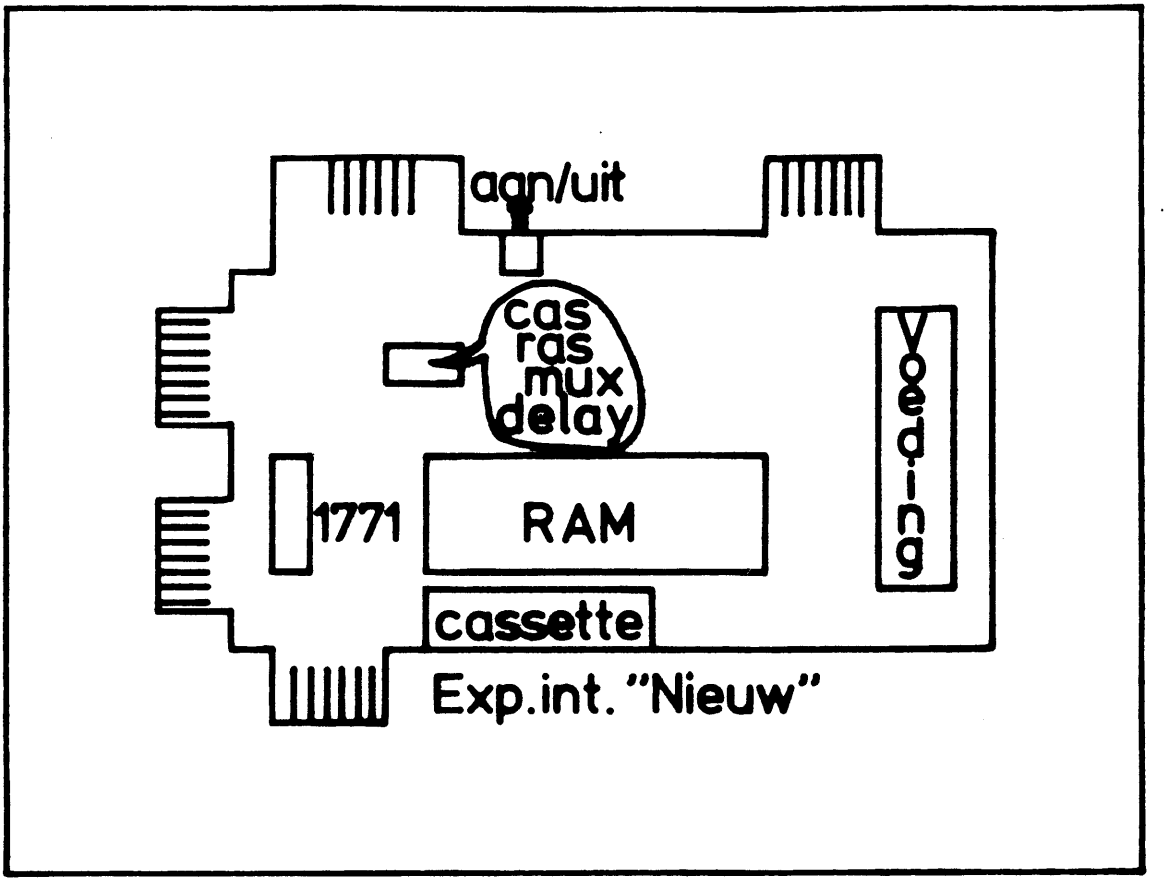

TRS-80 BUS
J2
+5V
GND
WAIT*
TEST*
INT*
SYSRES*
RD*
WR*
RAS*
OUT*
INTAK*
IN*
NC
D7
D6
D5
D4
D3
D2
D1
D0
37E8 READ
37E8 WRITE
37EC READ
37E4 WRITE
Z51-74LS240
Z50-74LS240
Y1(40 MHZ)
C44
C43
R1
10M
R2
1K
R3
2.2K
R30
10K
4049B
Z22
74LS08
Z25
74LS74
Z26
74LS74
Z28
74LS74
Z48-74 LS367
7416
Z34
Z32 74LS04
74LS243 - Z30
Z30
74LS155
Z45
74LS244
Z44
74LS244
Z43
74LS30
Z40
74LS139
TO SHT 2
CSW
32K
48K
MRAS*
RAS*
+12V
-5V

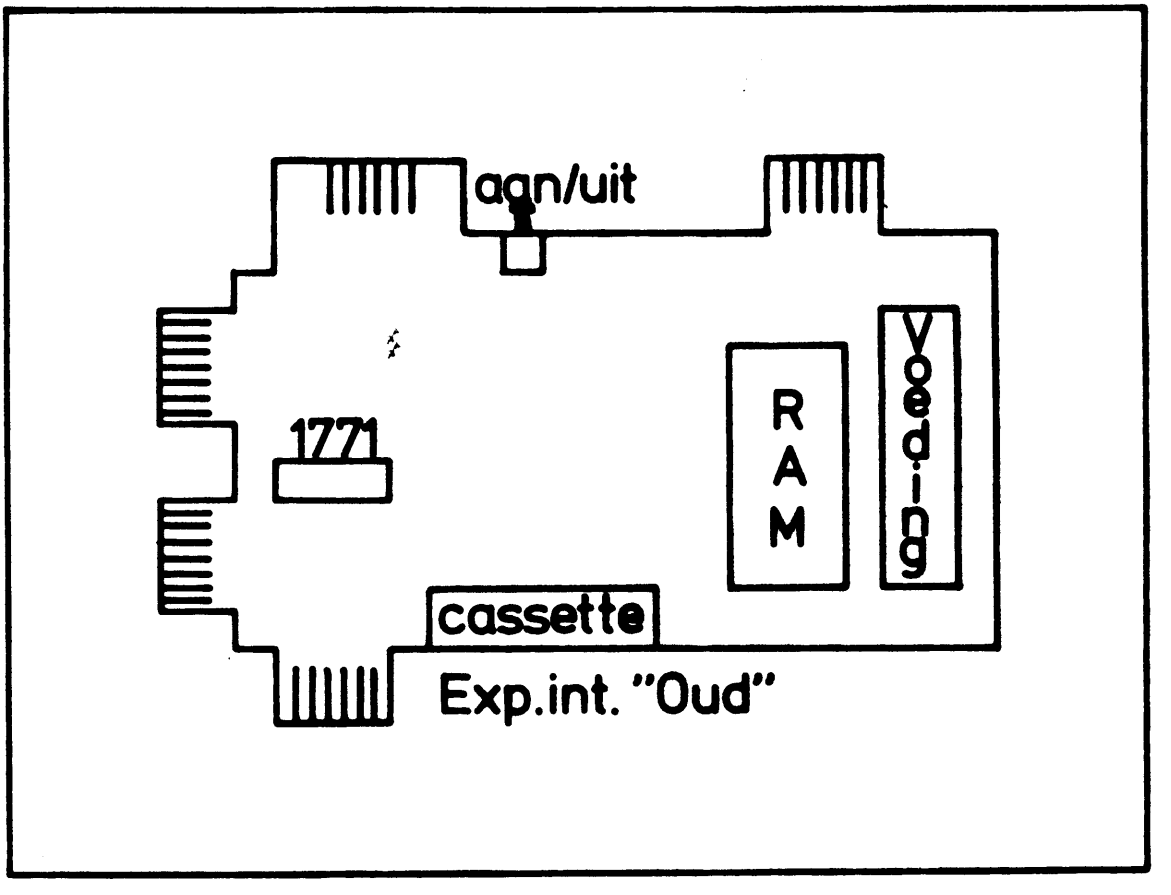


TRS-80 Nieuwe Exp.int. Schema. Sheet 1 B. 36

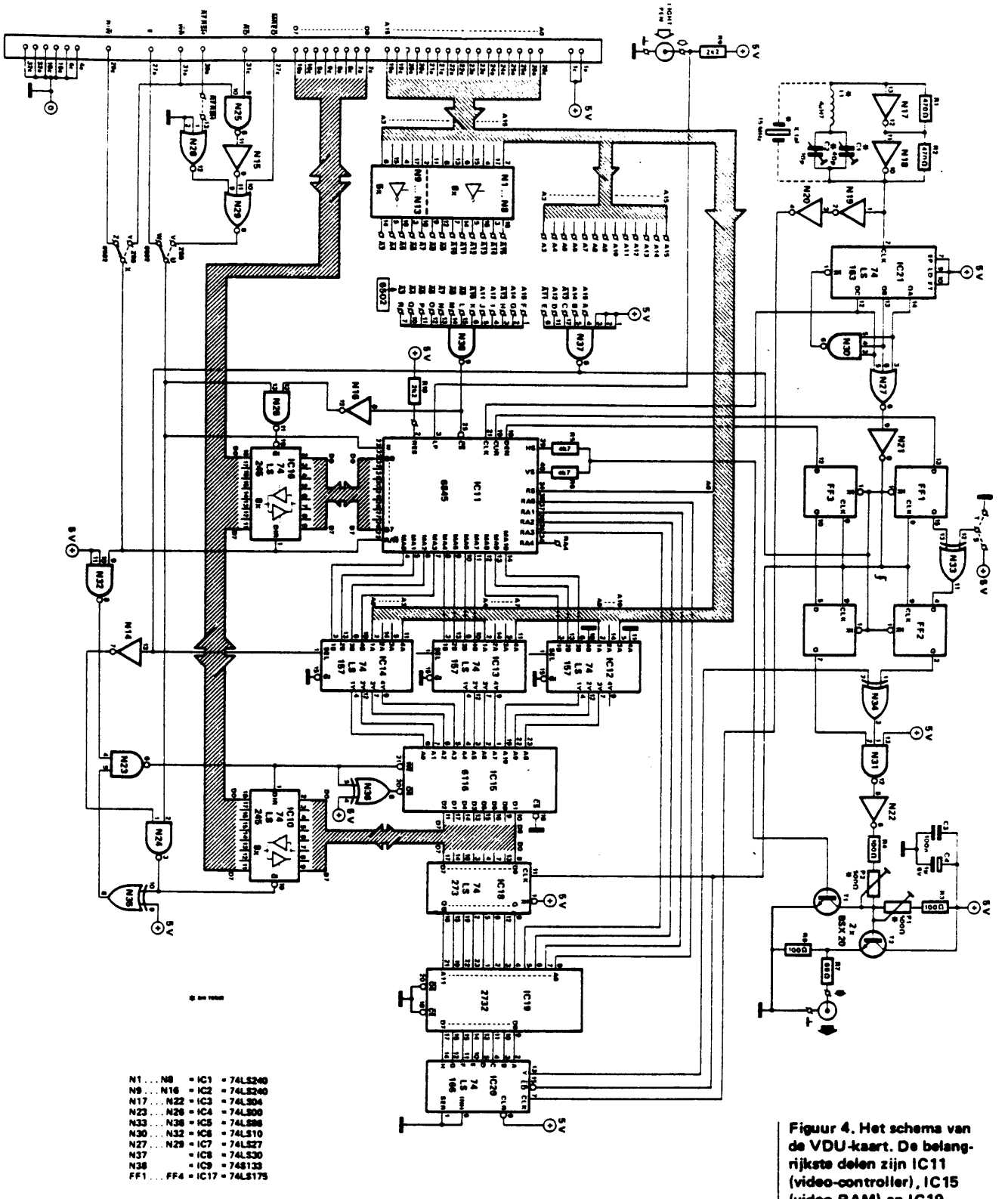

Z35 74LS157
Z36 74LS157
Z32 74LS04
Z29 · 74LS244
Z31 · 74LS244
Z32 · 74LS04
R26
R27
R18
R19
4.7K
TO SHT 1
FRONT VIEW
MDA +202 -
CR2
S1 PUSH-ON
+5V UNREGULATED
+12V
-5V UNREGULATED
+12V UNREGULATED
POWER SUPPLY
C57 10000 16V
C55 2200 35V
C60 220 16V
C63 10 16V
R15 2K
R8 1K
R9 3.3K
R4 12K
R21 220 2W
CR3 IN5231 5%


CASSETTE 1 SOCKET (OUTPUT)
TRS 80 CASSETTE SOCKET
INPUT FRONT VIEW
FRONT VIEW
CASSETTE 2 SOCKET (OUTPUT)
PIN
1 EN
2 GROUND
3 EN
4 CASSIN
5 CASSOUT
INTERNAL EXPANSION PIN-OUT
EXPANSION BOARD CONNECTOR J1
GND
Vcc
NC
D6
D7
SYSRES
D4
D5
A1
A0
D0
D3
D2
D1
INT
IN
A2
OUT
+12V
+5V
-5V
NOTES
1) ALL RAMS (MK4116) ARE IN 16 PIN SOCKETS
2) PIN 1,3,4,5,6,7,8,9,10,11,12,13 AND 16 OF ALL RAMS TIED IN PARALLEL

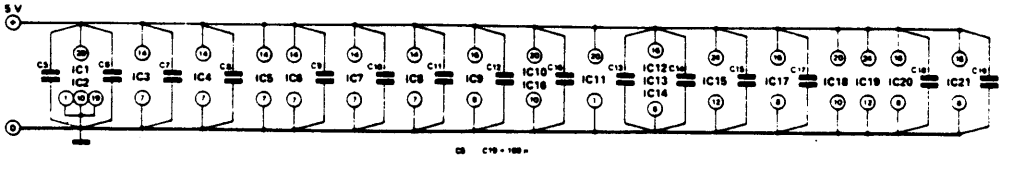




Vergelijkings tekening Exp.int oud-nieuw.

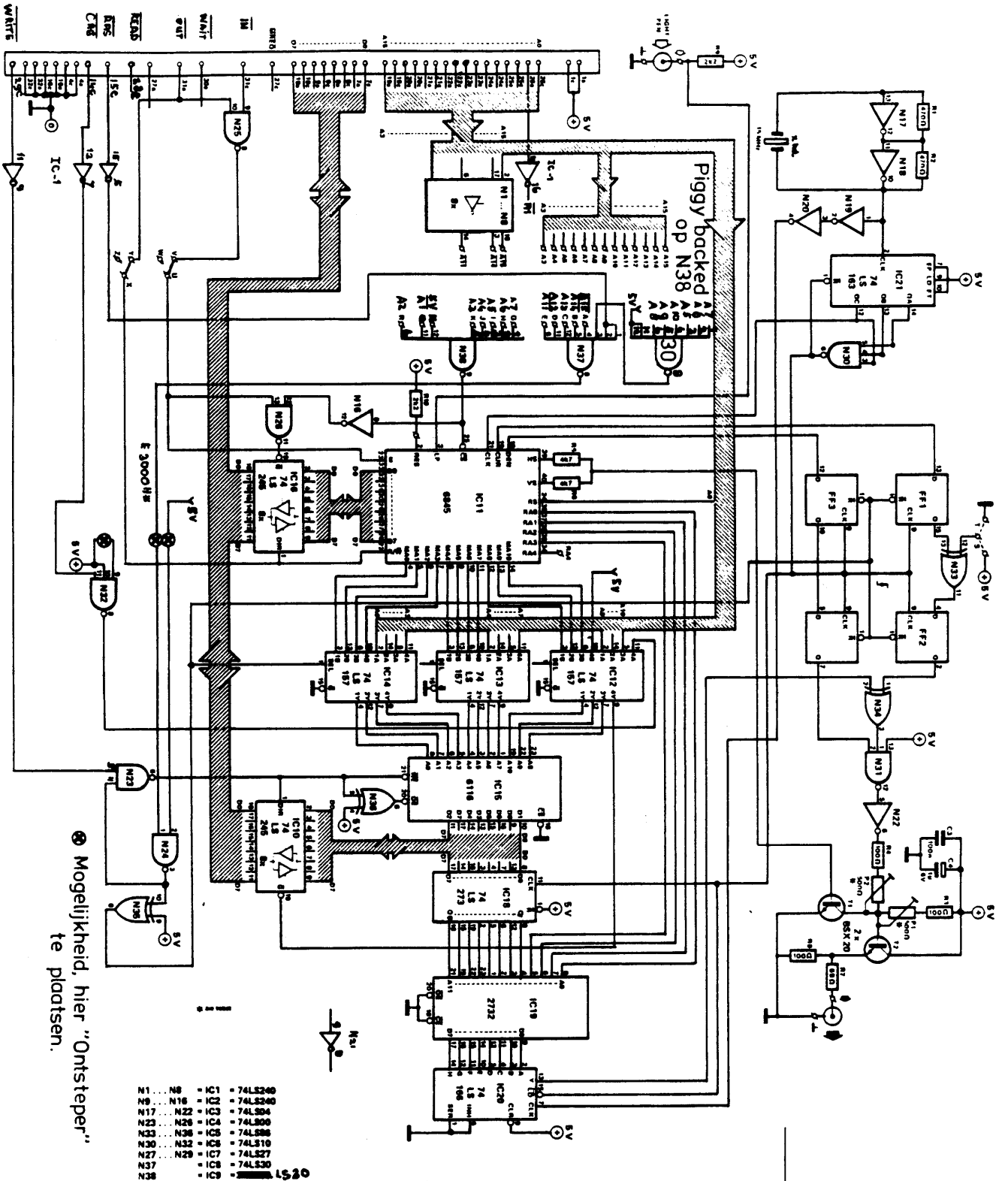


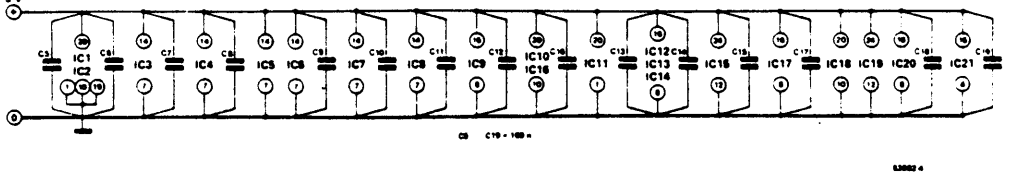
Figuur 4. Het schema van de VDU-kaart. De belangrijkste delen zijn IC11 (video-controller), IC15 (video-RAM) en IC19 (karaktergenerator).



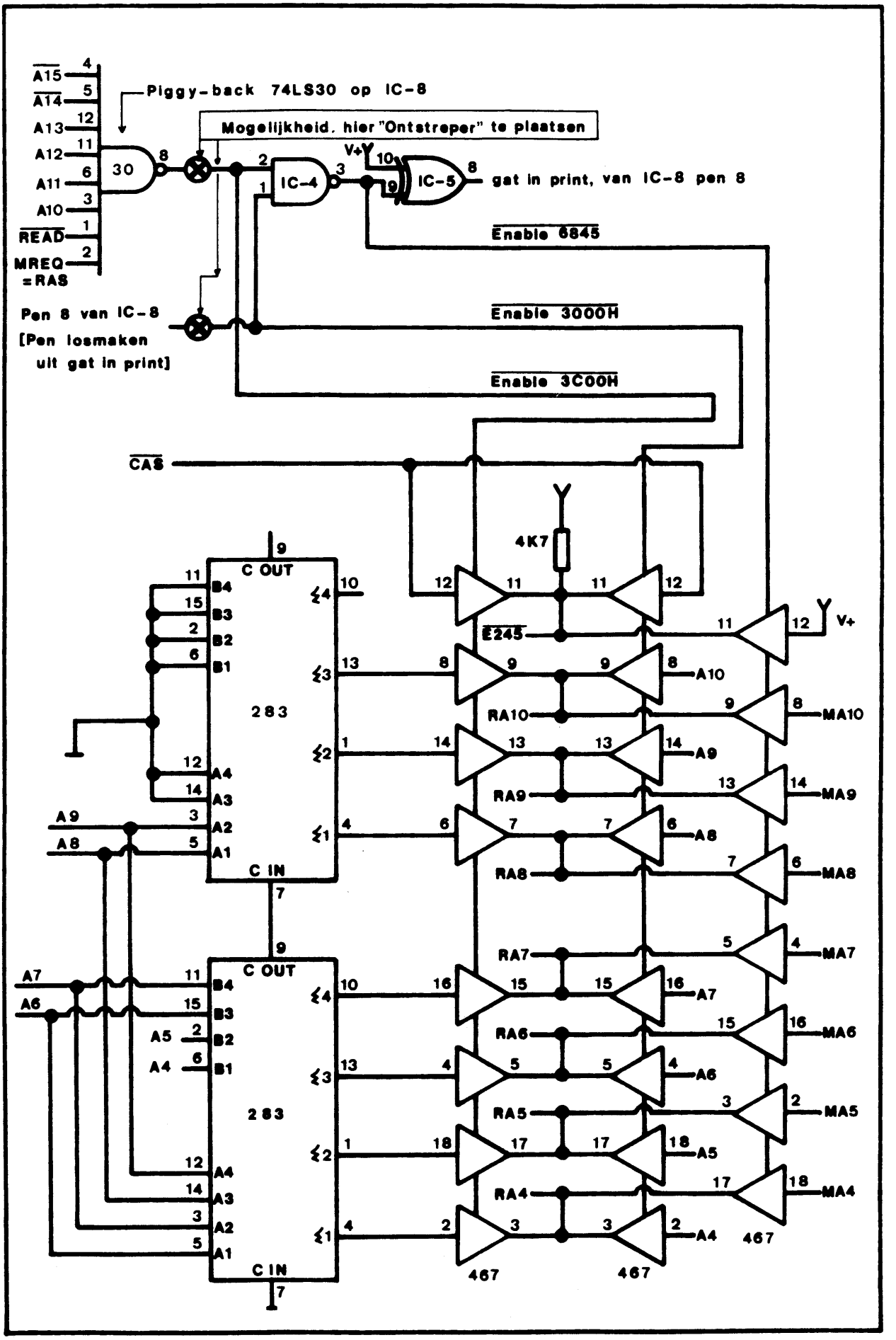
Figuur 5. De komponentenopstelling op de print voor de VDU-kaart. De koper-layouts van de dubbelzijdige print zijn afgedrukt op de Printlayout-pagina's achter in deze Elektuur.

VDU schema (origineel van Elektuur). 40

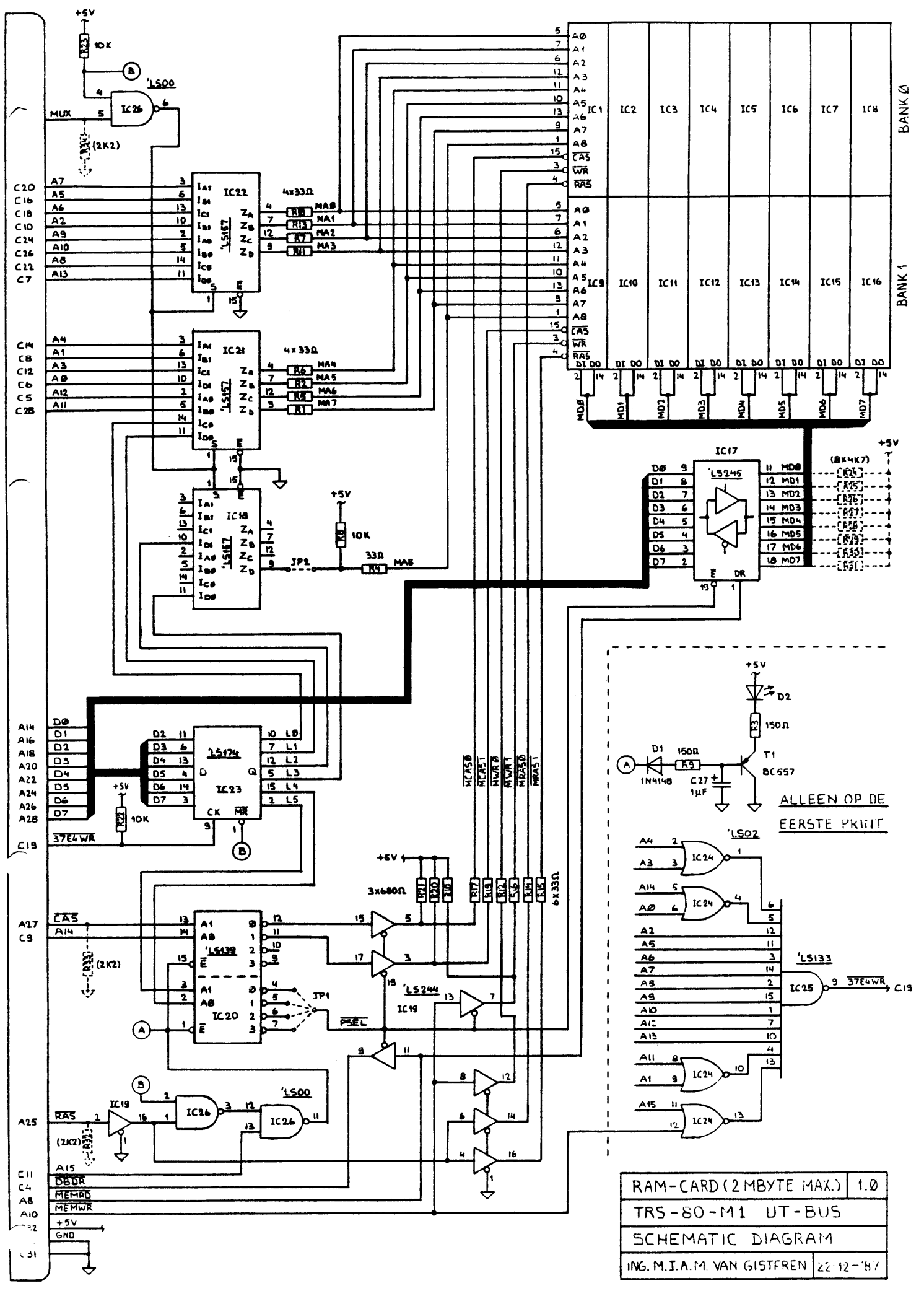




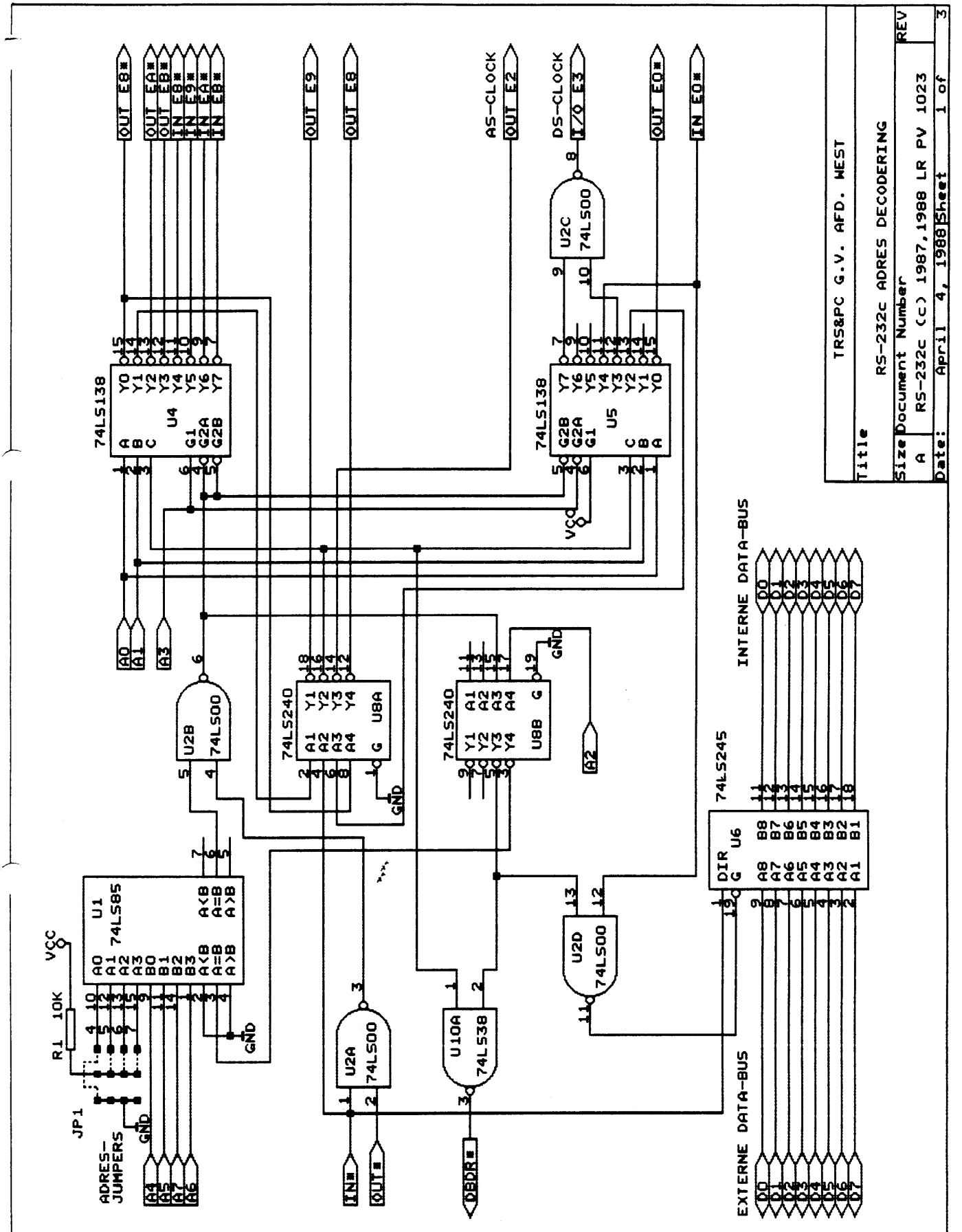
VDU schema (aangepast voor TRS-80).



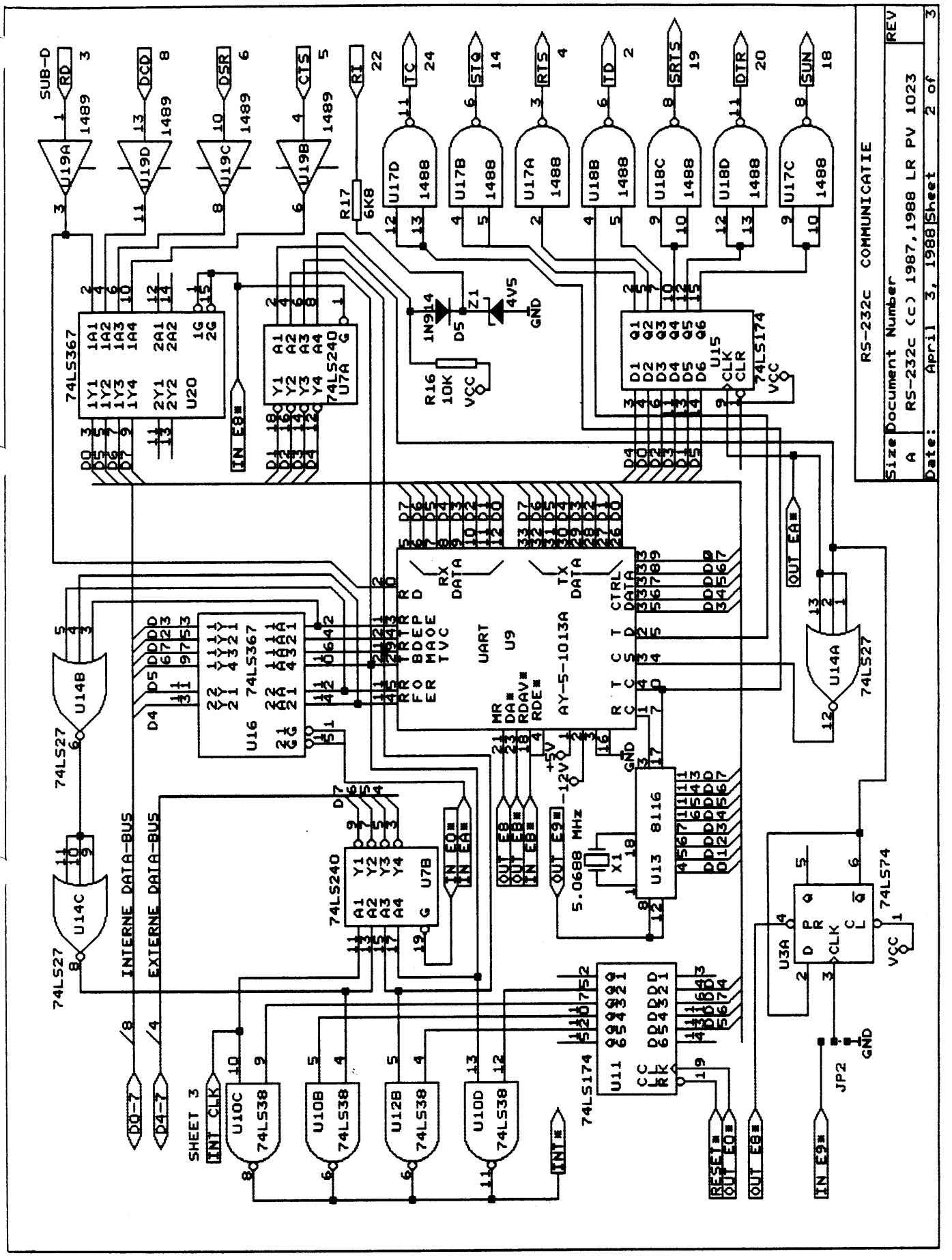
VDU opsteek printje (write-through) (schema). 42



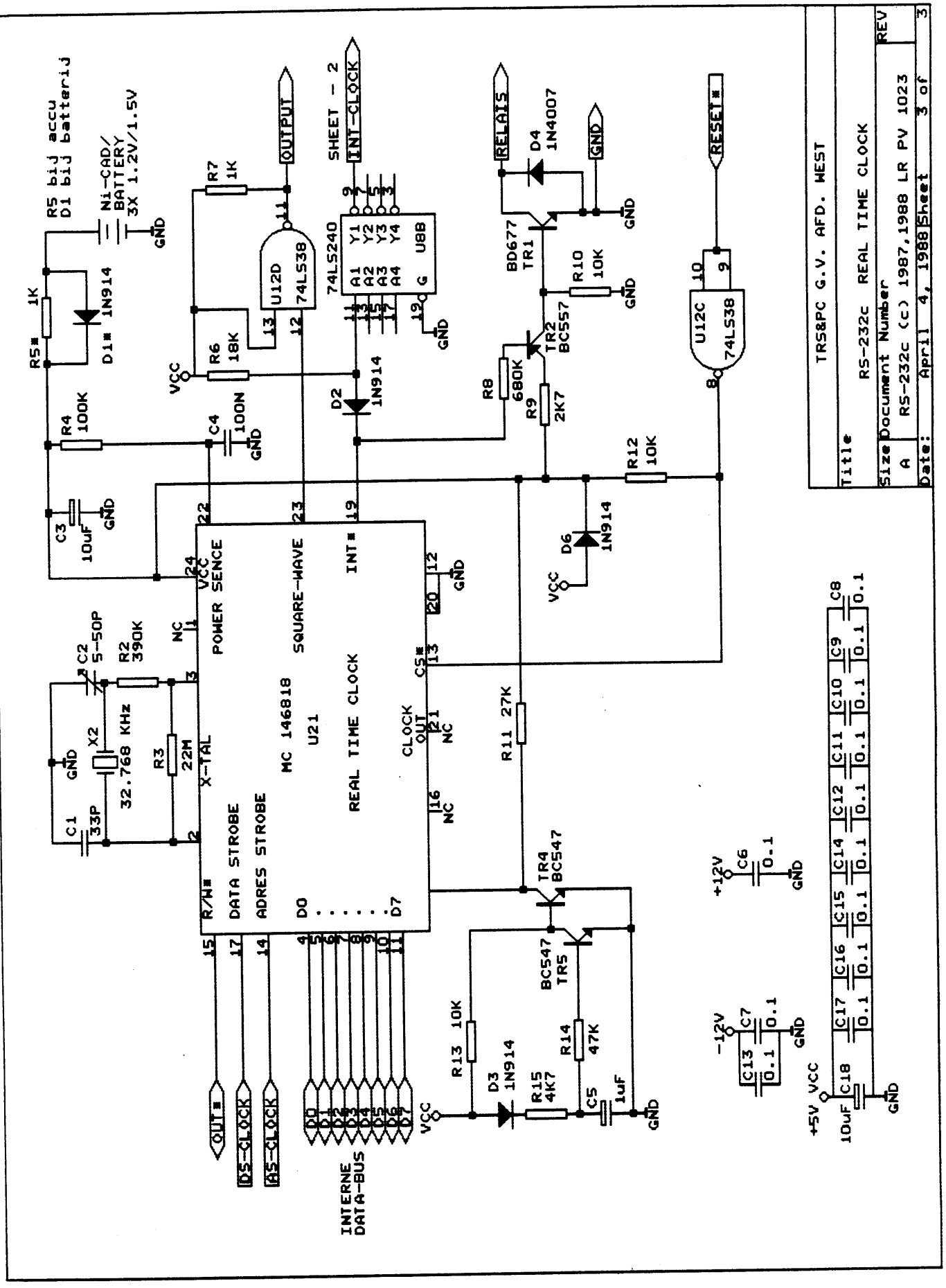
RAM uitbreidings print (schema).



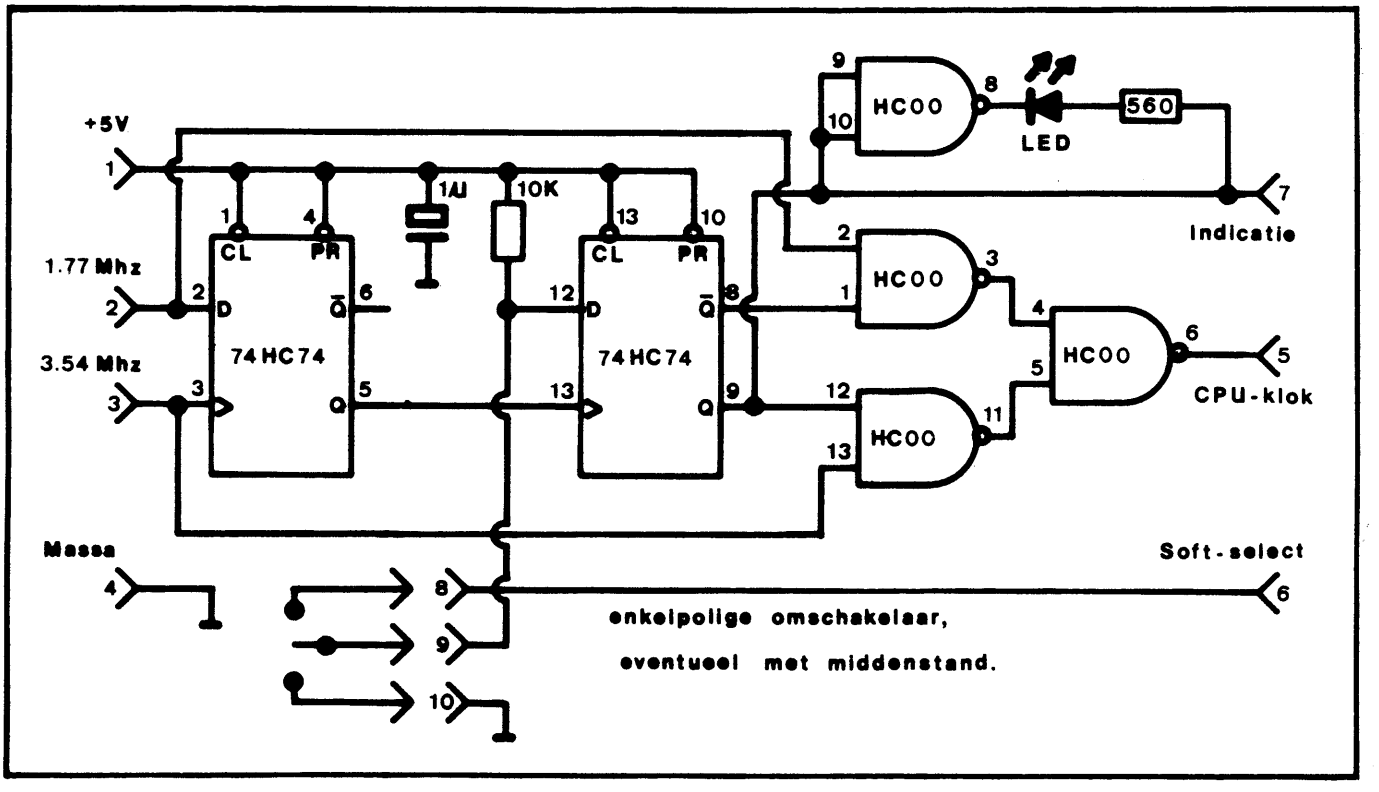
RS-232 print. Schema adres decodering.



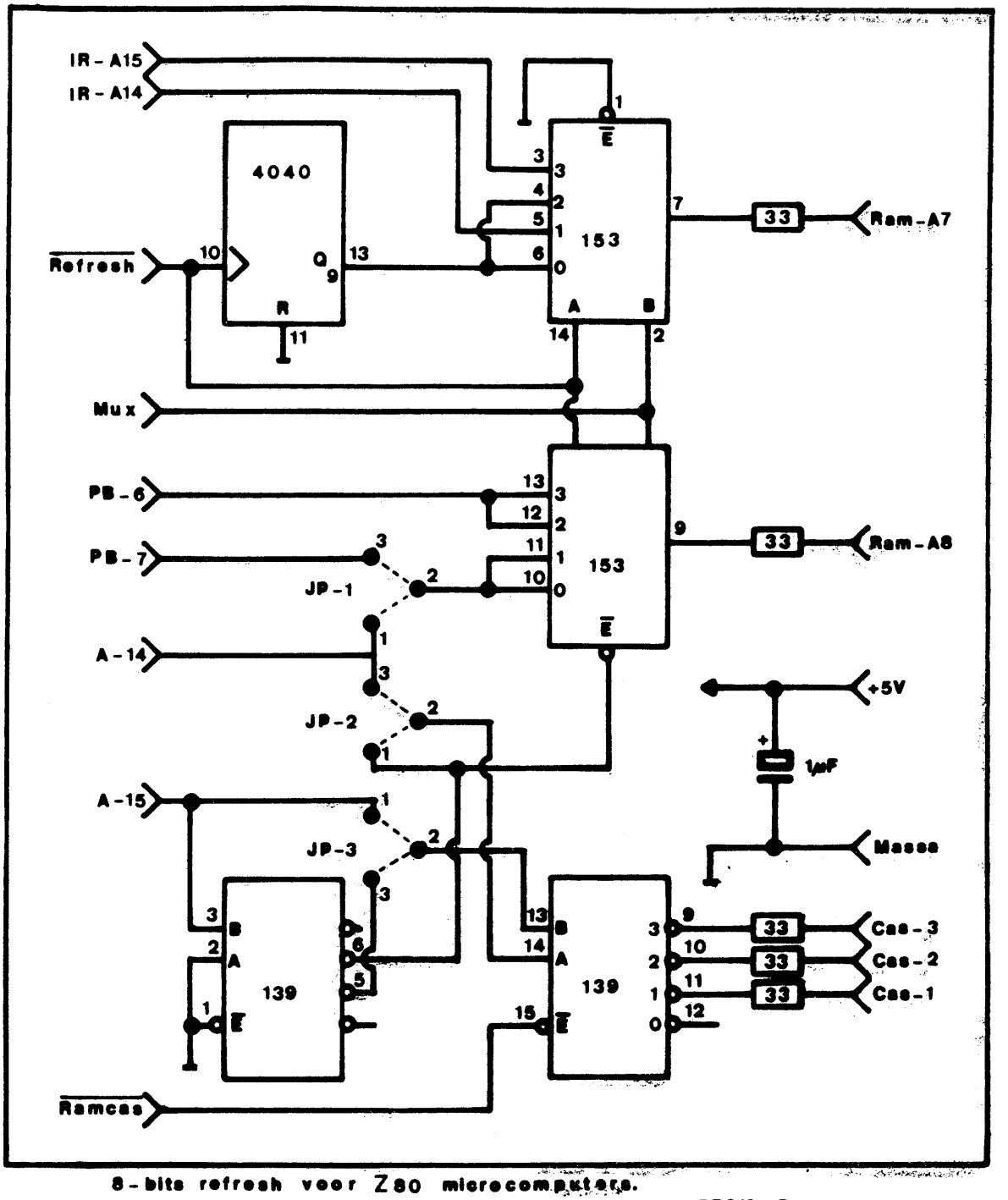
RS-232 print. Schema communicatie.



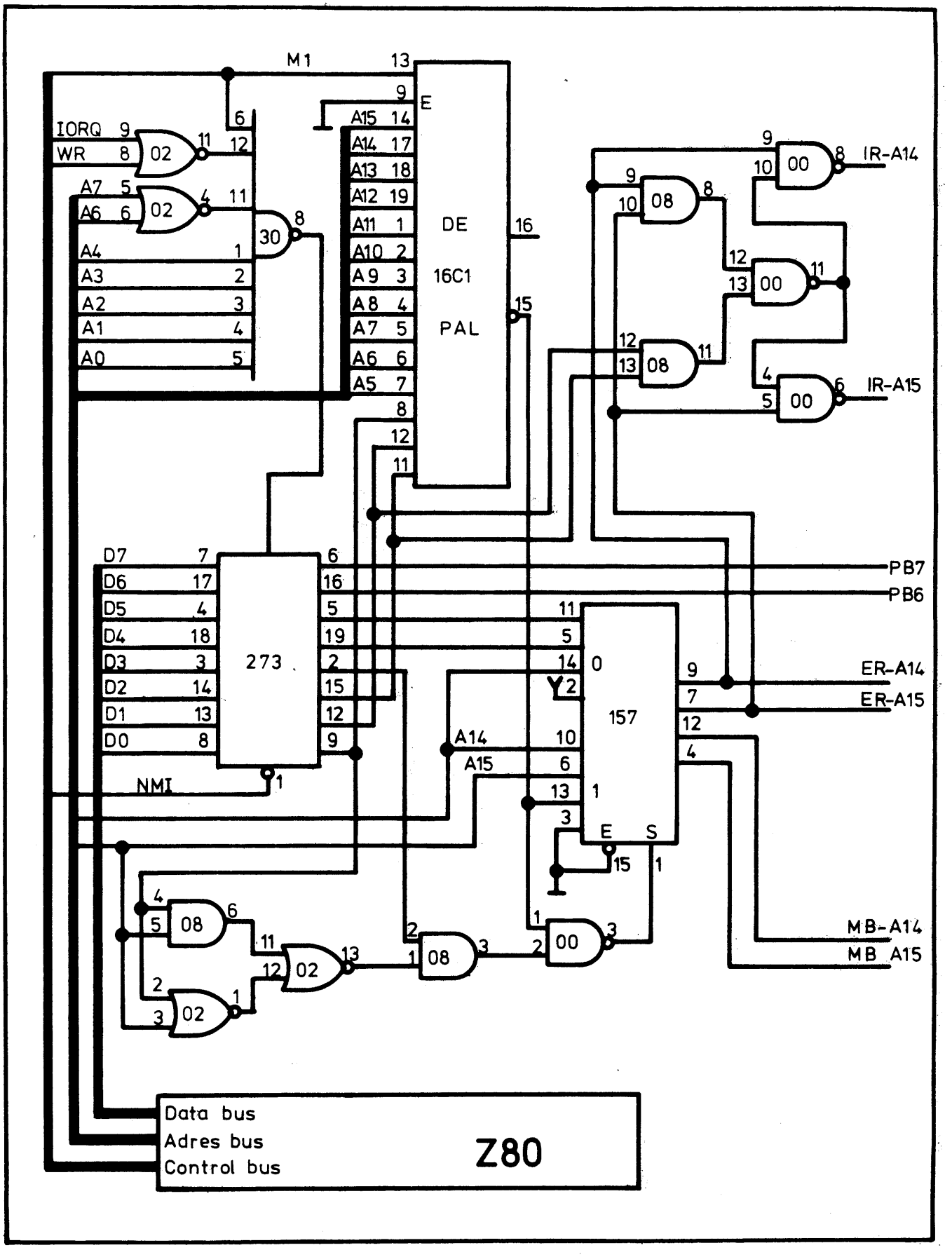
RS-232 print. Schema real time clock.

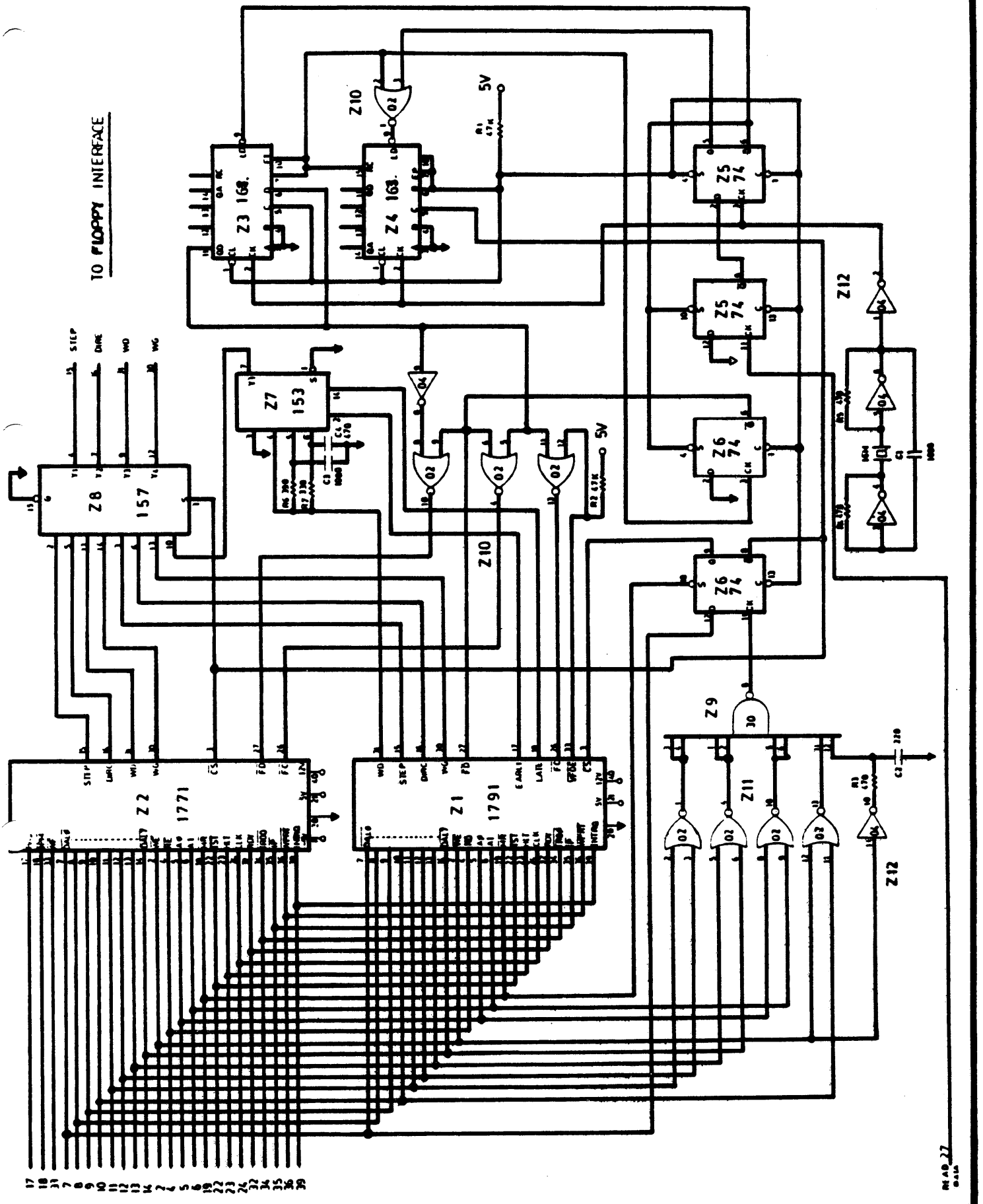


Speedup schema.



8-bits refresh voor Z80 microcomputers.
Samen met Selekter 256K, 320K, 512K of 576K Ram
in TRS-80 model I of compatible computer aansluitbaar.


M1
IORQ
WR
A7
A6
A4
A3
A2
A1
A0
02
30
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
E
DE
16C1
PAL
08
00
IR-A14
IR-A15
D7
D6
D5
D4
D3
D2
D1
D0
273
NMI
PB7
PB6
157
A14
A15
ER-A14
ER-A15
MB-A14
MB A15
Data bus
Adres bus
Control bus
Z80


TO FLOPPY INTERFACE
Z10
Z3 163
Z4 163
5V
Z5 74
Z6 74
Z12
Z7 153
Z8 157
Z10
Z9
Z11
Z2 1771
Z1 1791
STEP
DIRC
WD
WG
READ 22