4.11 Speaker Circuit (Sound Generator)

The QX-10 is designed to permit free programming of the scale and length of the sound from the speaker by changing the frequency using the timer counter μPD8253.
This function is enabled by I/O selection of the timer counter μPD8253 (14E/16E) or memory bank register LS273 (18F) and setting appropriate data.
Connection of these signals is shown in Fig. 4-21.
The signal supply line to the speaker and sound setting items bythat signal are shown in Table 4-3.

Connection		Setting item
IC' 23H' pin 13	Timer counter 8253-5 (16E) OUT 0 output	Setting of speaker frequency. Usually, the speaker frequency is set to about 1 kHz by IPL.
IC' 23H' pin 5	Time counter 8253-5 (14E) OUT 0 output	Approx. speaker timer setting. Usually, the speaker timer is set to about 100 ms by IPL.
IC' 23H'pin 4	Memory bank register LS273 (18F) Q2 output	Setting of continued or discontinued speaker sound. Continued sound is obtained by setting 1 in the bit 2 of the memory bank register.

Table4-3 Setting of speaker sound

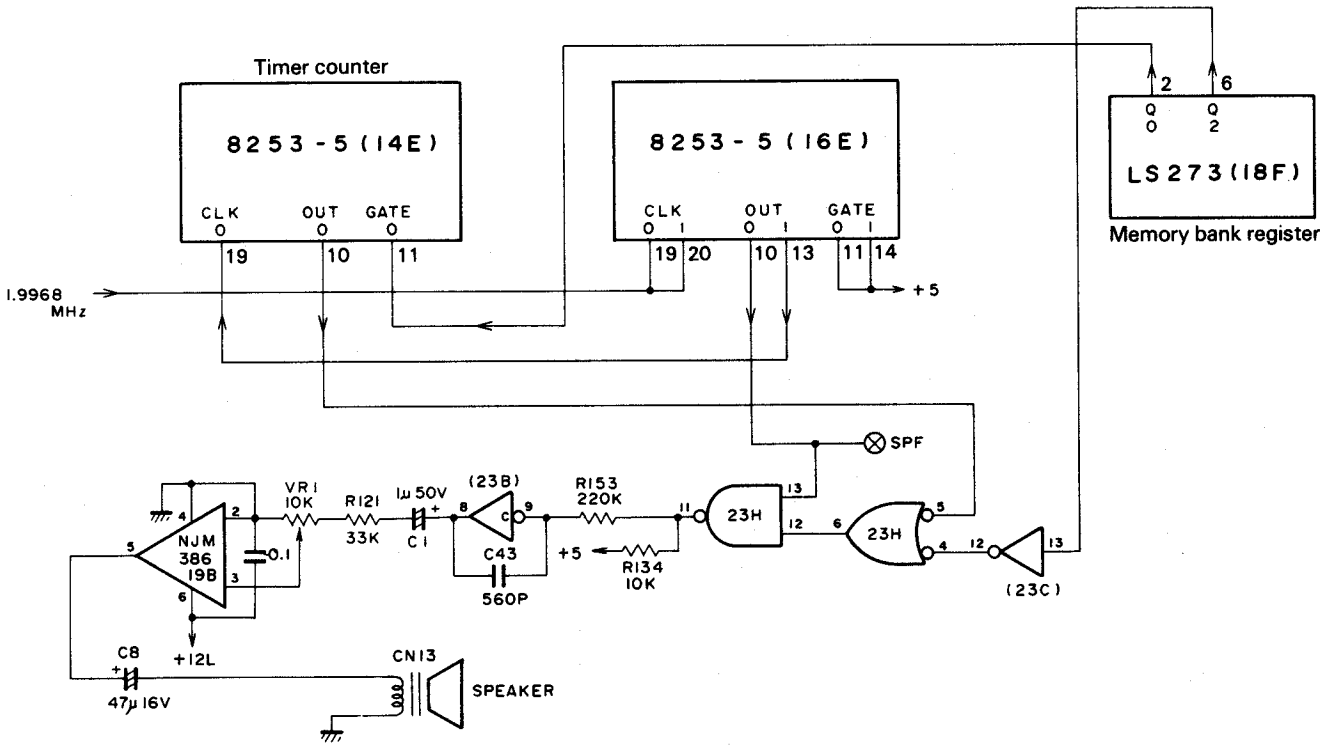


Fig. 4-21 Sound generator

4.12 Programmable Interval Timer μPD8253-5

Two programmable interval timers μPD8253-5 (14E/16E) compatible with Z80 are provided to set the speaker frequency, keyboard clock or RS-232C baud rate.
The μPD8253-5 (14E/16E) has three counters with the same function, enabling setting of operation mode at a program level.

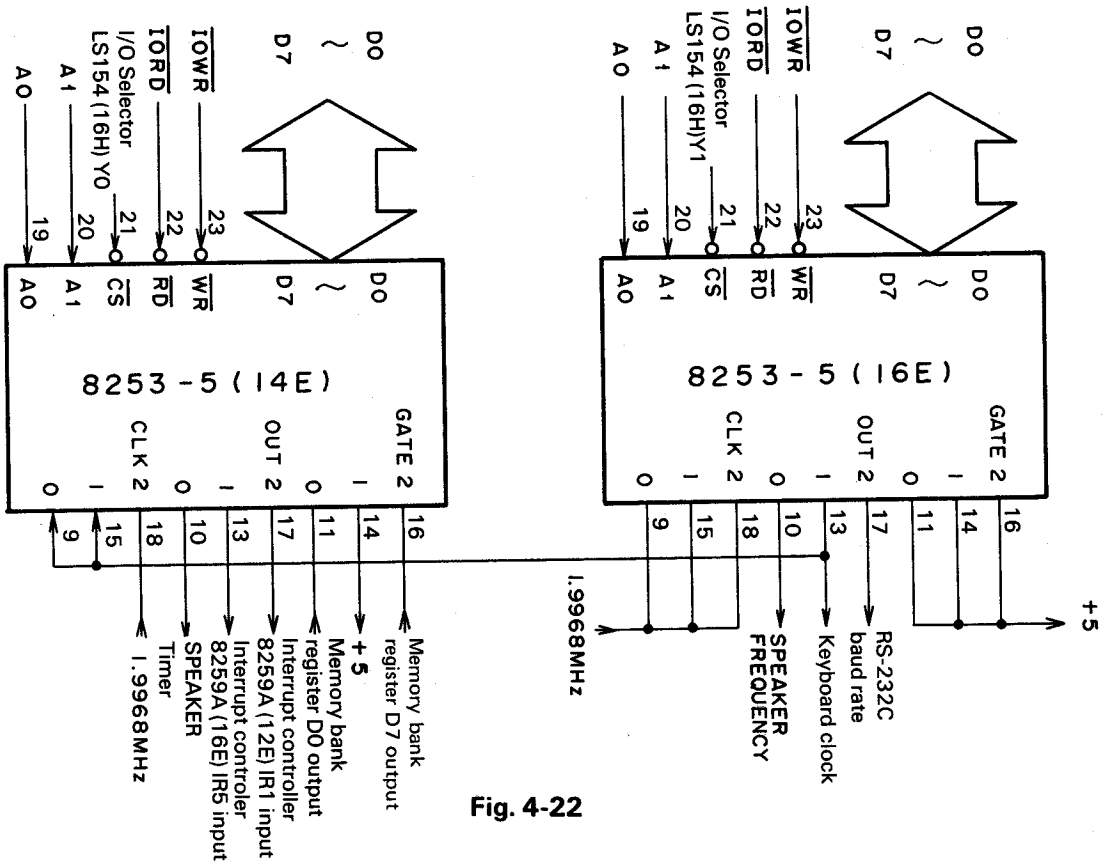


Fig. 4-22

Setting of this timer counter operation is as shown in 4.10 I/O command. The operation mode is set by the binary data of low-order 1 to 3 bits of the I/O command.

The relationship between the operation mode and gate signal is as shown in Table 4-4.

Mode	Operation	Gate signal		
		"L" or trailing edge	Leading edge	"H"
0	OUT becomes 1 when the specified count ends.	Count stop	–	Count
1	One shot pulse (active low) of the specified length is output.	–	Count start OUT becomes L by the next CLK.	–
2	An n-dividing counter of input clock. However, since OUT becomes 0 only for one clock cycle, the duty becomes 1/n.	Count stop OUT = H	Count start	Count
3	An n-dividing counter of input clock. The duty is 1/2 when the count is even, and n-1/2n when it is odd.	Count stop OUT = H	Count start	Count
4	When the specified count ends, a strobe pulse of one clock cycle (active low) is output.	Count stop	–	Count
5	Count is started by a trigger input, and when the specified count ends, a strobe pulse of one clock cycle (active low) is output.	–	Count start	–

Table 4-4

Connection and operation of the μPD8253-5 in QX-10 are shown in Table 4-5. For detailed functions of each terminal, see the attached μPD8253-5.

	Counter No.	CLK	Gate	OUT	Operation
#1	0	Keyboard clock 1200 bps	Memory bank register D0 output	Speaker timer	Approx. speaker timer setting. Set to about 100 ms in IPL.
	1	↑	+5V	Interrupt controller 8259A (10E) IR5: input	Software timer
	2	clock 1,9968 MHz	Memory bank register D7 output	Interrupt controller 8259 (12E) IR1 input	Software timer
#2 (16E)	0	↑	+5V	Speaker frequency	Setting of the speaker frequency. Set to about 1kHz in IPL.
	1	↑	↑	Keyboard clock	Setting the keyboard clock. Set to 1200 bps in IPL. (1,9968 MHz ÷1664)
	2	↑	↑	RS-232C baud rate	Setting RS-232C clock. Set to 9600 bps in IPL. (1,9968 MHz ÷ 208)

Table 4-5

4.13 Serial Interface μPD7201

The μPD7201 MPSC (Multi-protocol Serial Controller) controls serial-parallel and parallel-serial conversions for data processing between the CPU and MODEM or other serial data processors.
The MPSC has two channels, and uses channel A as an interface for QX-10 and B for RS-232C.

Channel	Interface
A	Keyboard
B	RS-232C

(1) Channel A: Keyboard interface

Data transfer between the CPU and keyboard is made through channel A of μPD7201. Data transfer with the keyboard is made at the speed of 1200 bps in the start-stop tuning format (8 bits/chr, 1 stop bit odd parity).

The meanings of each signal line are shown in Table 4-6.

Keyboard	Direction	QX-10	Function
RTS	→	$\overline{\text{DCDA}}$	Indicates transmission permission from an external device. Operates in the same way as CTS.
CTS	←	$\overline{\text{DTRA}}$	Informs the receiving device that the transmitting communication channel is ready.
DTR	→	$\overline{\text{CTSA}}$	Indicates transmission permission from an external device and controls data transmission.
RXD	←	TXDA	Serial data line for transmission.
TXD	→	RXDA	Serial data line for reception.

Table 4-6

(2) Channel B: RS-232C interface

USART IC (11B: 75188 line driver, 13B, 13C: 75189 line receiver) conformable to the specifications of RS-232C is used as an interface between RS-232C and μPD7201.

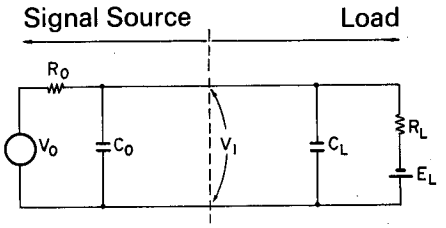
When a positive voltage is supplied, these operate on the specifications of RS-232C. The meanings of each signal line are shown in Table 4-7. The jumper wires of the interface are shown in Table 4-8.

External device	Direction	QX-10	Function
TXD	←	TXDB	Serial data line for transmission
RTS	←	RTSB	Signal to indicate that the transmitting side is making a transmission request.
TXC	←	–	Output as a clock to TXD.
CTS	→	$\overline{\text{CTSB}}$	Indicates transmission permission from an external device and controls data transmission.
DCD	→	$\overline{\text{DCDB}}$	Indicates transmission permission from an external device. Function is the same as $\overline{\text{CTSB}}$.
DSR	→	8255A(18B) PBO	This signal shows whether machine is ready or not.
RXD	→	RXDB	Receiving data input terminal
REV	←	DTRB	Informs the receiving device that the transmitting communication channel is ready.
DTR	←	DTRB	Informs the receiving device that the transmitting communication channel is ready.
RXC	→	$\overline{\text{RXCB}}$	Samples the receiving data at the leading edge of this signal.
DB	→	$\overline{\text{TXCB}}$	Transmitting data is output at the trailing edge of this signal.

Table 4-7

▶ Specifications of RS-232C

(1) Interconnection equivalent circuit (JIS C 6361)



V_O: Open circuit voltage of signal source.
R_O: Total effective DC resistance of signal source measured at interconnection point.
C_O: Total effective capacity of signal source measured at interconnection point.
V_I: Voltage for signal grounding line or common return line at interconnection point.
C_L: Total effective load capacity measured at interconnection point.
R_L: Total effective load resistance measured at interconnection point.
E_L: Open circuit voltage of load.

Signal Source		Load	
Open circuit voltage V0	: 25V (absolute value) or less	Load resistance RL	: 3 ~ 7 kΩ
Signal voltage V1 (for load 3 ~ 3 kΩ)	: 5 ~ 15V (absolute value)	Input threshold	: 3V (absolute value)
Minimum output resistance at power off	: 300Ω	Input voltage	: Max. 25V (absolute value)
Maximum output current at short	: 500 mA (absolute value)	Total effective load capacity CL	: 2500 pF or less
Through rate: Max	: 30V/μs	Open circuit voltage EL	: 2V or less

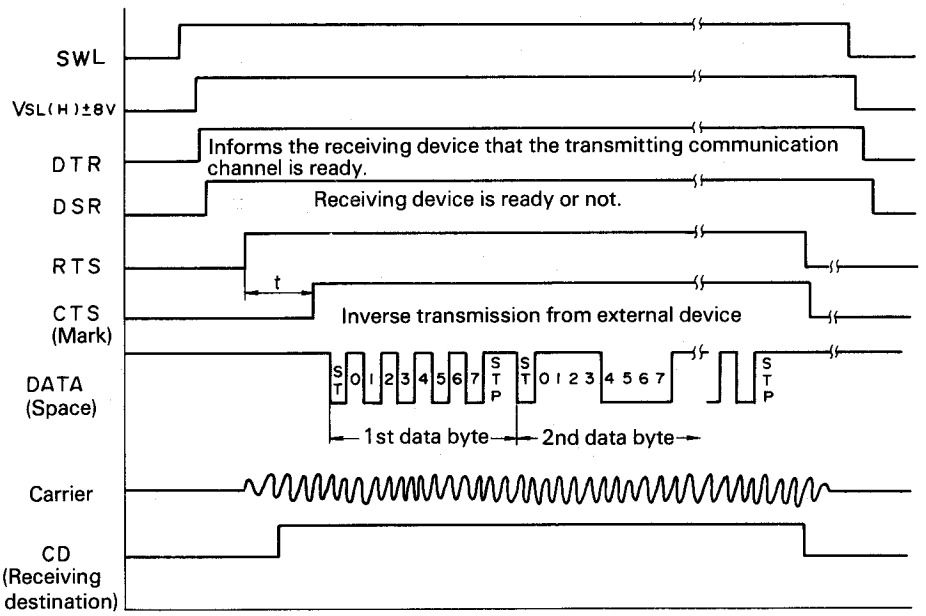
Fig. 4-23

(2) Signal polarity
Mark = Logic "1" (–3 ~ –25V): Stop bit
Space = Logic "0" (+3 ~ +25V): Start bit

(3) Word length
Start bit: 1 bit
Data bit: 7 or 8 bits
Stop bit: 1-bit length or longer

(4) Bit rate
110 BPS ~ 4800 BPS

▶ Operation timing of RS-232C (Using MODEM)



*t: Delay time registered by MODEM to be ready for transmission.

Fig. 4-24

► **Jumper Wires of RS-232C Interface**

Jumper			Direction	μPD7201	Function
J1	A	DTR	←	$\overline{DTRB}$	Normal use
	B	REV	←		Reverse channel
J2	A1	Input of RXCK signal from CTC	→	$\overline{TXCB}$	Operated by the internal clock.
	A2			$\overline{RXCB}$	
	B1	RXC	→	$\overline{TXCB}$	Operated by an external clock.
	B2	DB	→	$\overline{RXCB}$	
J3	A	Pull-up of +5V power line		PBO(8255)	Pull-up of the control line. Space status is set with the pull-up on.
	B			$\overline{DCDB}$	
	C			$\overline{CTSB}$	

Table 4-8

(3) MPSC μPD7201 ⇄ CPU or memory

Data, command and status are transferred in parallel between MPSC μPD7201 and the CPU or memory. The meanings of each signal line are shown in the Table 4-10. Modes set by combination of signals are shown in Table 4-9.

B/$\overline{A}$	C/$\overline{D}$	$\overline{WR}$	$\overline{RD}$	$\overline{CS}$	Function
0	0	0	1	0	Channel A — Writing transmission data
1					Channel B
0	0	1	0	0	Channel A — Reading received data
1					Channel B
0	1	0	1	0	Channel A — Writing the command/parameter register.
1					Channel B
0	1	1	0	0	Channel A — Reading from the status/vector register.
1					Channel B

Table 4-9

MPSC μPD7201	Direction	CPU/MEM	Function
D0 ~ D7	→	D0 ~ D7	An 8-bit two-way data bus used for transmission of data, command and status between MPSC and CPU.
$\overline{INTR}$	→	Interrupt controller 8259A (12E) IR4 input	An interrupt request signal output terminal.
B/$\overline{A}$	←	A0	Specifies the channel to write data onto the data bus or read the data from the data bus in the write/read operation. H: Channel B L: Channel A
C/$\overline{D}$	←	A1	Indicates that the information on the data bus is data, command or status, in the write/read operation.
$\overline{CS}$	←	I/O decoder LS154 (16H) Y4 output	Enables data/command transfer from CPU to MPSC (write cycle) or data/status transfer from MPSC to CPU (read cycle). This SIO is assigned to the I/O addresses 10H ~ 13H.
$\overline{RESET}$	←	$\overline{RESET}$	The same signal as the reset signal for the CPU is connected. Namely, the MPSC μPD7201 is reset in the following cases. 1 Reset by power on 2 Reset by the RESET switch (manual reset) 3 Reset from an external option
$\overline{RD}$	←	$\overline{IORD}$	Controls reading data/status from MPSC μPD7201 to CPU or memory.
$\overline{WR}$	←	$\overline{IOWR}$	Controls writing data/command from CPU or memory to MPSC.
$\overline{RXCA}$	←	CTC 8253-5 (16E) OUT1 output	Samples the data received from the keyboard at the leading edge of this signal.
$\overline{TXCA}$	←	CTC 8253-5 (16E) OUT1 output	Data is transmitted to the keyboard at the trailing edge of this signal.
ϕ	←	3.9936 MHz	A signal of 3.9936 MHz is supplied like the clock of CPU. The system clock rate needs to be increased to 4.5 times the data rate.

Table 4-10

▶ Keyboard Power Supply Circuit

The keyboard is powered by +12V of Q10SYM board through pin 3 of connector 1. To prevent a malfunction caused by unstable voltage at power on, supply of +12V is stopped by the circuit shown in Fig. 4-26 by making the reset signal to the CPU active for the duration while a low pulse is output from the Q-terminal which follows the time constant of the externally mounted CR of the single shot LS123 (24K). That is, when the reset signal to the CPU is active, the B-terminal input of LS123 is set to low level. On the other hand, since the A-terminal input is connected to the ground, when the B-terminal input rises to high level, a low level signal of 100 ~ 200msec which follows the time constant of the externally mounted RC is generated at the Q-terminal as an output.

By the gate of IC23K, these signals make the output of pin 11 of IC23K high level for about 100 ~ 200msec. from power on to leading edge of the Q-terminal output signal.

Since this signal makes the base of transistor Q2 high level via the two-stage inverter, it cuts off Q2. Therefore, during this reset period, +12V is not supplied to the keyboard.

When the reset signal is released, the base of Q2 is set to low level, and Q2 is turned on and +12V is supplied to the keyboard. The voltage waveform of this circuit is shown in Fig. 4-25.

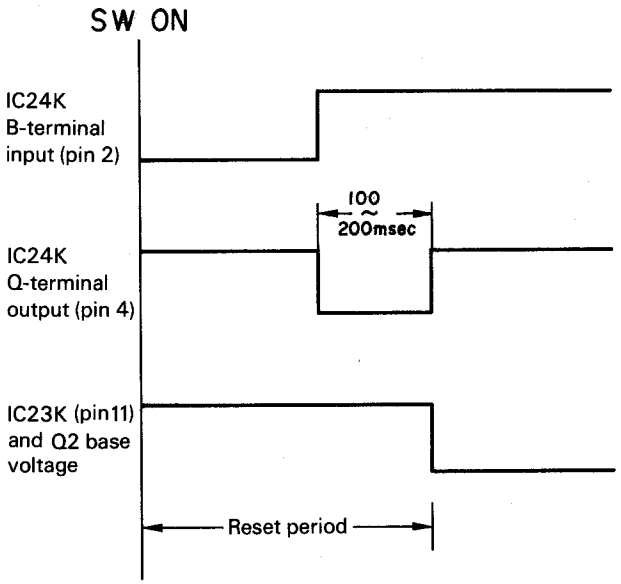


Fig. 4-25 Timing chart of keyboard power supply circuit

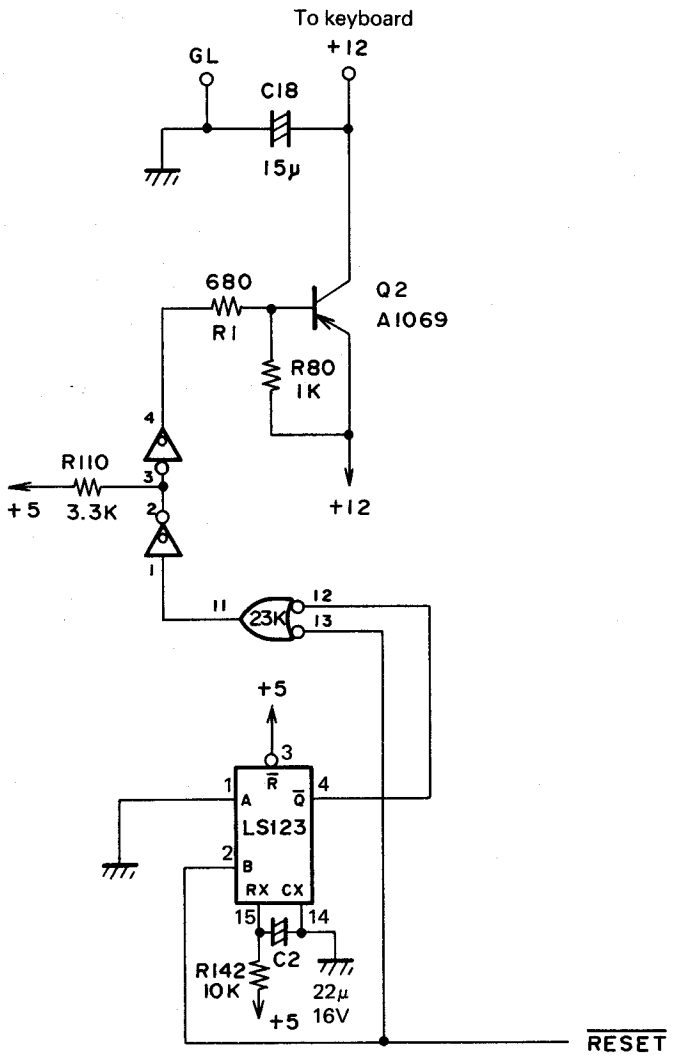


Fig. 4-26 Keyborad power supply circuit

4.14 Interrupt Controller μPD8259

This system uses two programmable interrupt controllers μPD8259 to give priority to 15 levels of interrupt requests made from an external device for controlling the interrupt to the CPU. In this case, as shown in Fig. 4-27, the SP (Slave Program) terminal of IC 12E is connected to +5V and SP terminal of IC 10E to GND, thereby allocating the μPD8259 to the master and slave programs.
The master program is preferentially interrupted. Regarding IR (Interrupt Request) terminals, IR0 has priority over IR7.
Interrupt addresses are shown in Table 4-11.
The actual address table after completion of IPL will be the value obtained by adding 780H to the relative addresses of the left side.

▶ Interrupt Sequence

When an interrupt routine address is generated, the μPD8259 is capable of jumping directly or indirectly to the requested specific interrupt routine without polling the interrupt requesting device.

(1) When one or more interrupt request inputs (IR0 ~ 7) become high level, all the corresponding bits of IRR (Interrupt Request Register) are set.
(2) The μPD8259 evaluates these requests and sends the INT signal to the CPU when they are recognized as appropriate.
(3) Recognizing the INT signal, the CPU returns one $\overline{\text{INTA}}$ pulse to the μPD8259.
(4) Receiving the first $\overline{\text{INTA}}$ pulse sent from the CPU, the μPD8259 outputs the CALL instruction code (11001101) to the data bus.
(5) Receiving the CALL instruction, the CPU sends two $\overline{\text{INTA}}$ pulses back to the μPD8259.
(6) Synchronizing with these two $\overline{\text{INTA}}$ pulses, the μPD8259 outputs the programmed subroutine address to the data bus: the low-order 8 bit addresses for the first pulse and the high-order 8 bit addresses for the second pulse.
At the trailing edge of the second pulse, the μPD8259 sets the ISR (In-Service Register) bit with the highest priority and resets the corresponding IRR bit.
(7) Generation of a 3-byte call instruction by the μPD8259 has now been completed.

Connection		Relative address	Interrupt cause	
Master	IR0	0000	Power down detection interrupt	High-order
	IR1	0004	Software timer # 1 interrupt	
	IR2	0008	External (option) interrupt INTF 1	
	IR3	000C	External (option) interrupt INTF 2	
	IR4	0010	Keyboard/RS-232C interrupt	
	IR5	0014	CRT/light pen interrupt	
	IR6	0018	Floppy controller interrupt	
				Priority
Slave	IR0	0020	Printer interrupt	
	IR1	0024	External (option) interrupt # 1	
	IR2	0028	Calendar clock interrupt	
	IR3	002C	External (option) interrupt # 2	
	IR4	0030	External (option) interrupt # 3	
	IR5	0034	Software timer # 2 interrupt	
	IR6	0038	External (option) interrupt # 4	
	IR7	003C	External (option) interrupt # 5	Low-order

Table 4-11 Interrupt addresses

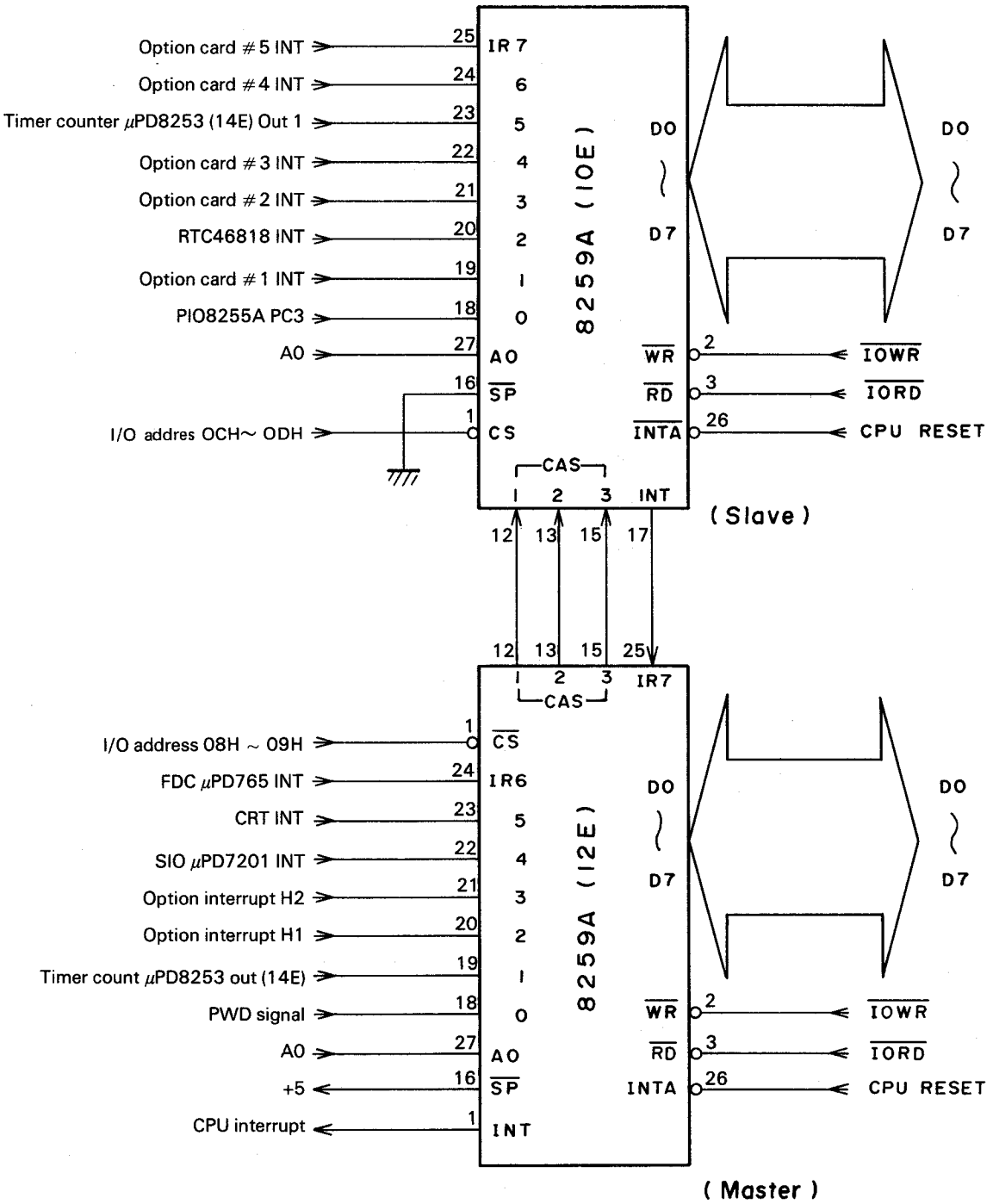


Fig. 4-27

4.15 Printer Interface Circuit

The QX-10 uses PIO (Parallel Input/Output Controller) 8255 to realize the interface of Centronics parallel specifications.

The interface circuit is shown in Fig. 4-29. The functions of terminals are shown in Table 4-13.

► PIO Operation Mode

The PIO 8255 (18B) is originally set to mode 1.

In this mode, port A is assigned as a data bus output to the printer and port B as a data line input of status information from the printer.

Port C is, as shown in Fig. 4-28, designed to supply $\overline{INT}$ and $\overline{ACK}$ signals accompanying transfer of input/output data of ports A and B.

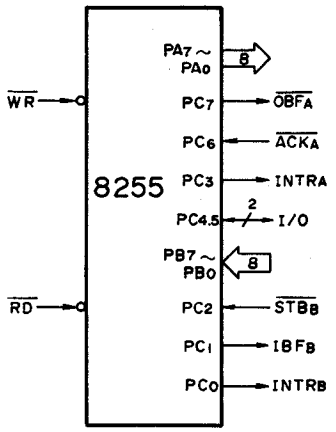


Fig. 4-28

► Data Transfer Sequence

Data transfer with the printer is made in the following sequence. The timing is shown in Fig. 4-30.

(1) Data is output from the QX-10 to the printer via data buses DB0 ~ DB7, and at the same time a data strobe pulse is output from PC0.
The printer reads the data at the trailing edge of the data strobe pulse.

(2) After reading the data, the printer goes into data processing for printing. During this period, the printer cannot accept data, and sets the $\overline{RDY}$ signal for data input inhibition to the high level.

(3) After completing the data processing, the printer sets the $\overline{RDY}$ signal to low level and then sends the $\overline{ACK}$ signal for data transfer request to the QX-10 and goes into the next data accept operation.

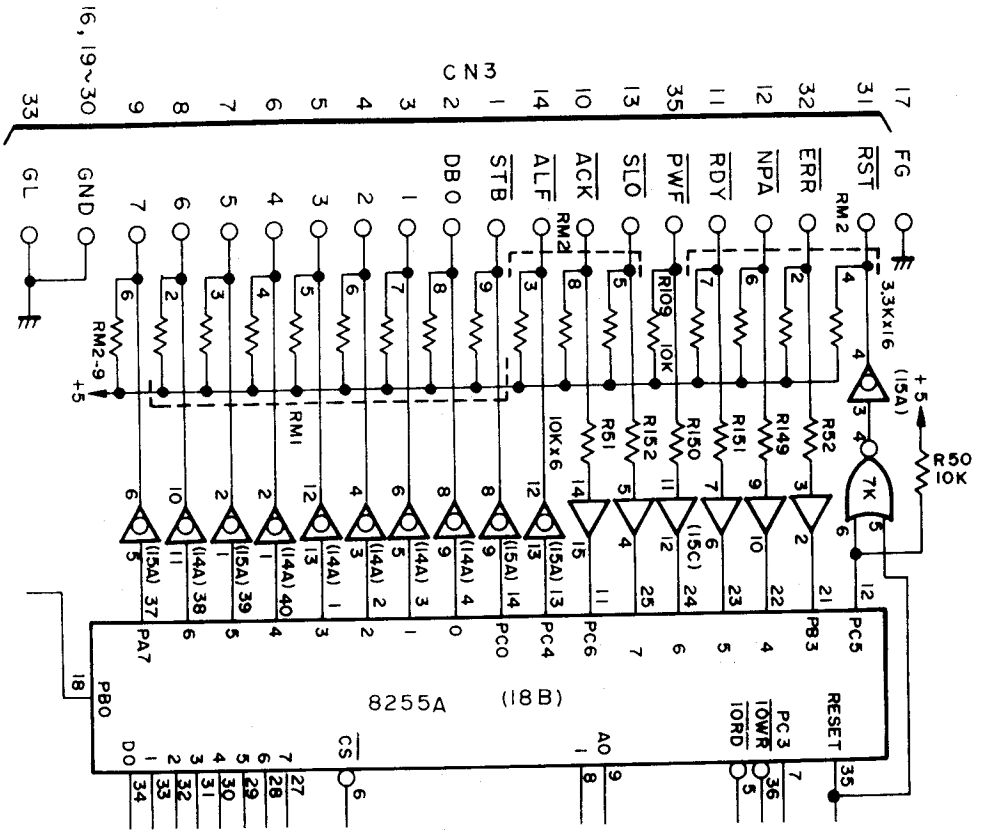


Fig. 4-29

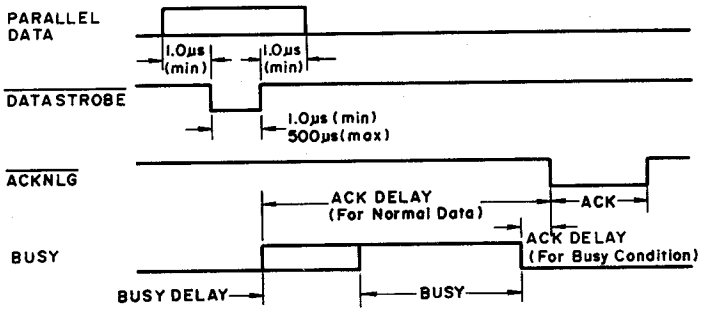
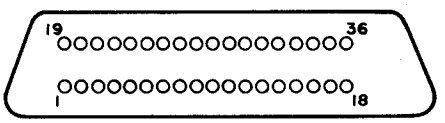


Fig. 4-30 Centronics timing chart

Terminal	Signal	Terminal	Signal
1	DATA STROBE	19	TWISTED PAIR GND
2	DATA 1	20	TWISTED PAIR GND
3	DATA 2	21	TWISTED PAIR GND
4	DATA 3	22	TWISTED PAIR GND
5	DATA 4	23	TWISTED PAIR GND
6	DATA 5	24	TWISTED PAIR GND
7	DATA 6	25	TWISTED PAIR GND
8	DATA 7	26	TWISTED PAIR GND
9	DATA 8	27	TWISTED PAIR GND
10	ACKNLG	28	TWISTED PAIR GND
11	BUSY	29	TWISTED PAIR GND
12	PE	30	INPUT PRIME RETURN
13	SLCT	31	INPUT PRIME
14	±0V	32	FAULT
15	OSCXT	33	LD
16	±0V	34	EX PRIME
17	CHASSIS GND	35	
18	+5V	36	

Table 4-12 Centronics connectors specifications



Connector part No. 552742-1 (AMP)

Terminal name	Signal	I/O	Function
D0 ~ D7	Data bus input	I/O	Connected to the CPU data bus and used for data transfer with the CPU.
$\overline{CS}$	Chip select	I	A signal obtained by decoding the CPU address bus (A0 ~ A7) by the I/O selector LS154 (16H) is supplied. This PIO μPD8255A is allocated to the I/O addresses 14H ~ 17H.
PA0 ~ PA7	Data bus output	O	Used as a data output bus to the printer.
PB0	DSR	I	This signal shows whether machine is ready or not. (RS-232C signal)
PB3	$\overline{ERR}$	I	Accepts the error signal from the printer. A low active signal.
PB4	$\overline{NPA}$	I	Accepts the no paper detect signal from the printer.
PB5	$\overline{RDY}$	I	Low level: Indicates that the printer is ready to receive data. High level: Indicates that the printer is busy for data processing.
PB6	$\overline{PEF}$	I	A signal to detect printer power down. Low active.
PB7	$\overline{SLO}$	I	A signal to indicate that the printer is not in the error state, but in the select (effective operation) state.
PC0	$\overline{STB}$	O	A strobe pulse generated when data is sent to the printer. Low active signal.
PC3	IR0	O	An interrupt input to the interrupt controller 8259A (10E).
PC4	$\overline{ALF}$	O	By setting this signal to low level, the printer automatically feeds line after printing the input data.
PC5	RST	O	Valid at reset by power on, reset switch or an external I/O. At this time, all the internal registers (including the control register) are cleared. An active low signal.
A0, A1	A0, A1 (CPU) Port Address	I	Connected to the CPU addresses A0 and A1 and used for mode setting of 8255A in cooperation with $\overline{IORD}$ and $\overline{IOWR}$ signals.
$\overline{IORD}$	$\overline{IORD}$ (From CPU)	O	Supplied from the CPU and used to set the mode of 8255A.
$\overline{IOWR}$	$\overline{IOWR}$ (From CPU)	O	A write signal to 8255A. By applying a low level signal to this terminal, data or control words can be written.

Table 4-13

4.16 Floppy Disk Controller μPD765

4.16.1 FDC Clock Supply Circuit

The FDC clock supply circuit has its own clock different from the clock of the main CPU.

The clock is 4 MHz, which is obtained by dividing the original oscillation of 8 MHz into two by the 4-bit binary counter LS393 (19H).

The $\overline{WCLK}$ signal which gives the timing signal of data writing into a drive is obtained by taking the logic of Q_B, Q_C and Q_D outputs of the counter LS393 (19H) and dividing the original oscillation to make a timing signal of 500 kHz.

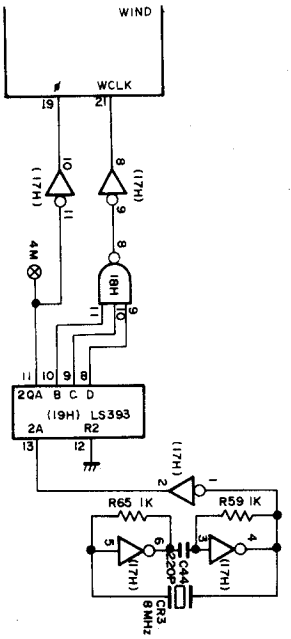


Fig. 4-31

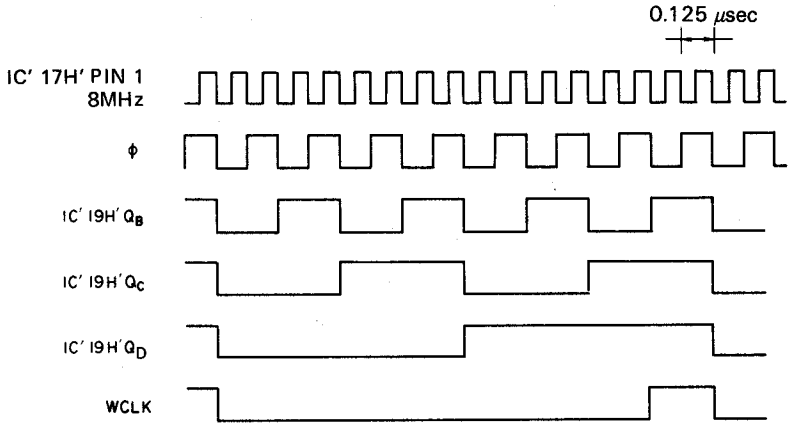


Fig. 4-32

4.16.2 Reading the Memory Bank Resister and the Status of FDC

As shown in Fig. 4-33, the memory bank register and FDC status information are read into the CPU or other I/O device through the 3-state buffer LS541 (20E).

$\overline{E1}$ and $\overline{E2}$ signals which permit data output of LS541 are supplied by the $\overline{IORD}$ signal from the CPU and Y12 output ($\overline{CSFDM}$) signal of the I/O selector LS154 (16H), respectively.

Therefore, the status information is read by reading the I/O address 30 H.

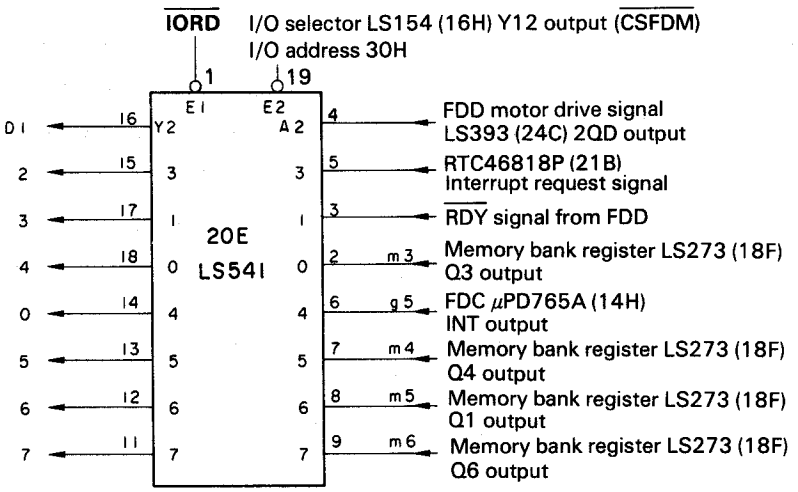
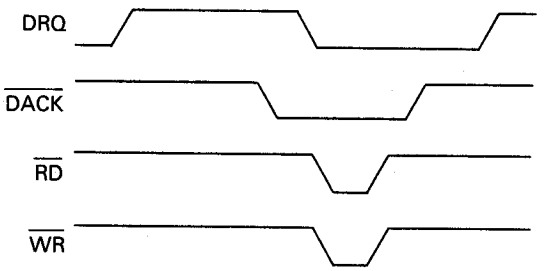
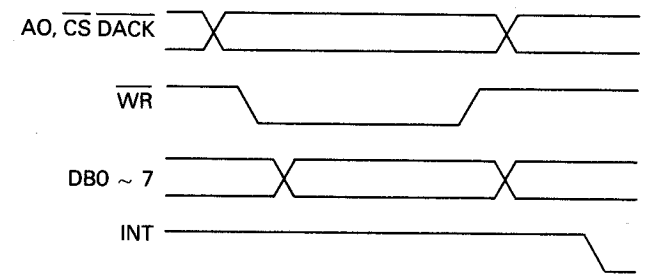
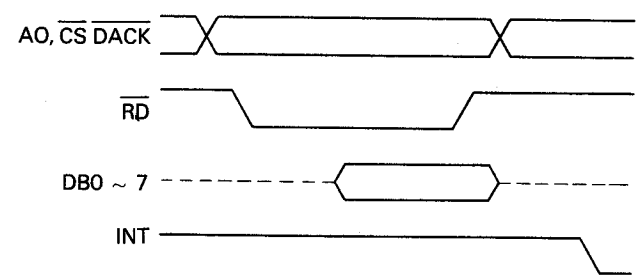


Fig. 4-33

4.16.3 CPU ⇆ FDC μPD765

The FDC μPD765 and system data and control signals are connected as shown in Table 4-14.

Signal name	I/O	Function
D7 ~ D0	I/O	Bidirectional 3-state data bus connected to the system data bus.
INT	O	A signal to indicate that the FDC is requesting service. This signal is output at every one byte in the NON DMA mode, and at the end of command operation in the DMA mode. This signal is connected to the IR6 terminal of the interrupt controller μPD8259 (12E).
RESET	I	The drive interface output which sets the FDC to the idle state and eliminates the WDATA output (indifinite). It also sets INT and DREQ outputs to low level. D7 ~ D0 are set to the input state. The same as the reset signal to the CPU is connected to this signal. The reset signal must be 1.68 μsec. minimum.
DREQ	O	A signal to request data transfer between FDC and memory in the DMA mode. This signal is connected to the DREQ1 terminal of the DMA controller μPD8237AC (21J).
$\overline{DACK}$	I	A signal to indicate that the DMA cycle is given. The function is the same as that of the $\overline{CS}$ signal in the DMA cycle. This signal is connected to the DACK1 terminal of the DMA controller μPD8237AC (21J). Receiving the above DREQ signal, the $\overline{DACK}$ signal is made active. DMA operation 
$\overline{WR}$ $\overline{RD}$	I	Write operation  Read operation 

Signal name	I/O	Function
A0	I	A signal to select the status register and data register in FDC to be accessed via the data bus. The status register is selected when this signal is "0", and the data register when it is "1". This signal is connected to the CPU address A0.
TC	I	A signal to indicate the end of read or write operation from the main system. This signal is supplied by the Q output of FFs LS73 (20H). The FFs is reset at the leading edge of the $\overline{DACK}$ signal. This TC pulse must be 120 ns minimum.

Table 4-14

► FDD Motor Contrl Circuit

The FDD motor control signal is supplied by the circuit shown in Fig. 4-34. The motor is started by specifying the I/O address 30H and making the $\overline{IOWR}$ signal active low.

The motor driving time depends upon the SQW signal supplied by RTC46818 (21B).

The FDD motor timer length is set in the low-order 4 bits of port OAH of RTC46818 assigned to the I/O address 3DH, and the motor driving time is set by turning on/off the square wave (SQW wave) output from bit 3 of port OBH. Namely, assuming that the data set in the low-order 4 bits of port OAH is n in decimal notation, the motor on time of $1/16 \times 2^n$ is set by two LS393 as shown in Fig. 4-34.

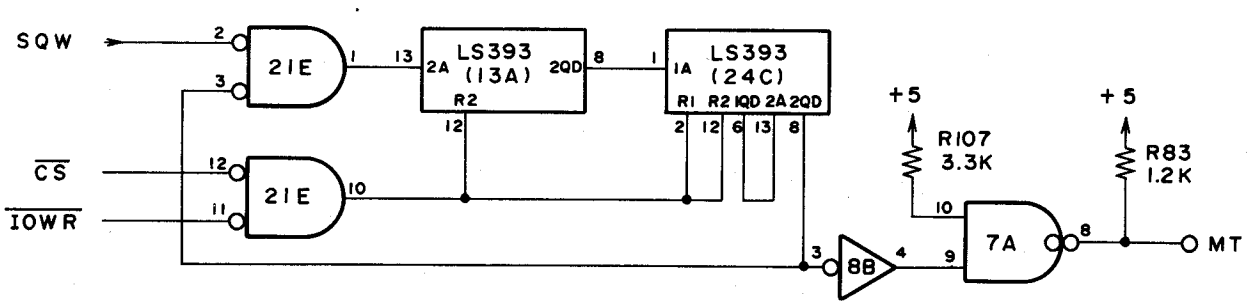


Fig. 4-34

4.16.5 Interface between Drive and FDC μPD765

The FDC μPD765 and FDD SD-321 are connected by the control signals shown in Table 4-15.

SD-321		Direction	μPD765	Function
4	HLD (Head Load)	←	HOLD	A signal to set the drive read/write head to the load state.
34	RDY(Ready)	→	RDY	A signal to indicate that the drive is in the ready state.
28	WPT (Write Protect)	→	WPRT	A signal to indicate when the write protect is set and the drive or media is inhibited from being written when the RW/SEEK signal specifies RW, and the two-side is set and the two-side media is inserted when the RW/SEEK signal specifies SEEK.
26	T0 (Track 00)	→	FLT/TRK0	A signal to indicate the FAULT state when the RW/SEEK signal specifies RW.
32	HDS (Side Select)	←	SIDE	A signal to select the head 0 (low level) and 1 (high level) of the two-side drive.
24	WG (Write gate)	←	WE	A signal to specify writing to the drive.
22	WD (Write data)	←	WD	Data to be written into the drive.
20	STP (Step)	←	FLTR/STEP	This signal works as a reset signal of the fault state held by the drive when the RW/SEEK signal specifies RW, and as a step signal of seek when the RW/SEEK signal specifies SEEK.
	↑↓	←	RW/SEEK	0: RW (Read/Write mode) 1: SEEK (Seek mode)
18	DIR	←	LCT/DIR	This signal indicates that the drive read/write head selects more than 43 cyclinders, when the RW/SEEK signal specifies RW. It specifies the seek direction when the RW/SEEK signal specifies SEEK. 0: Centrifugal direction 1: Centripetal direction
8	INDX (Index)	→	INDX	A signal to indicate the physical start point of the track on the media.
10	US0	←	US0 0	A signal to select FDD NO. to be drived.
			US1 0	
12	US1		US0 1	
			US1 0	
14	US2		US0 0	
			US1 1	
6	US3		US0 1	
			US1 1	

Table 4-15

The timing of these control signals for the FDD SD-321 is shown in Fig. 4-35.

(a) Seek operation

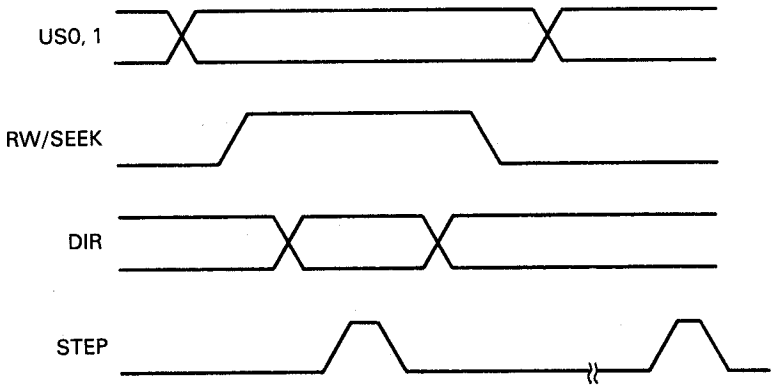


Fig. 4-35

4.16.6 VFO

► Circuitry of the VFO

The VFO is the "data window" generator which provides read data with sufficient margins. (See Fig. 4-36.)

The VFO is synchronized with the pulse train of the sync field where data "00" of the disk format is written, to obtain an accurate data window. (See Fig. 4-37.)

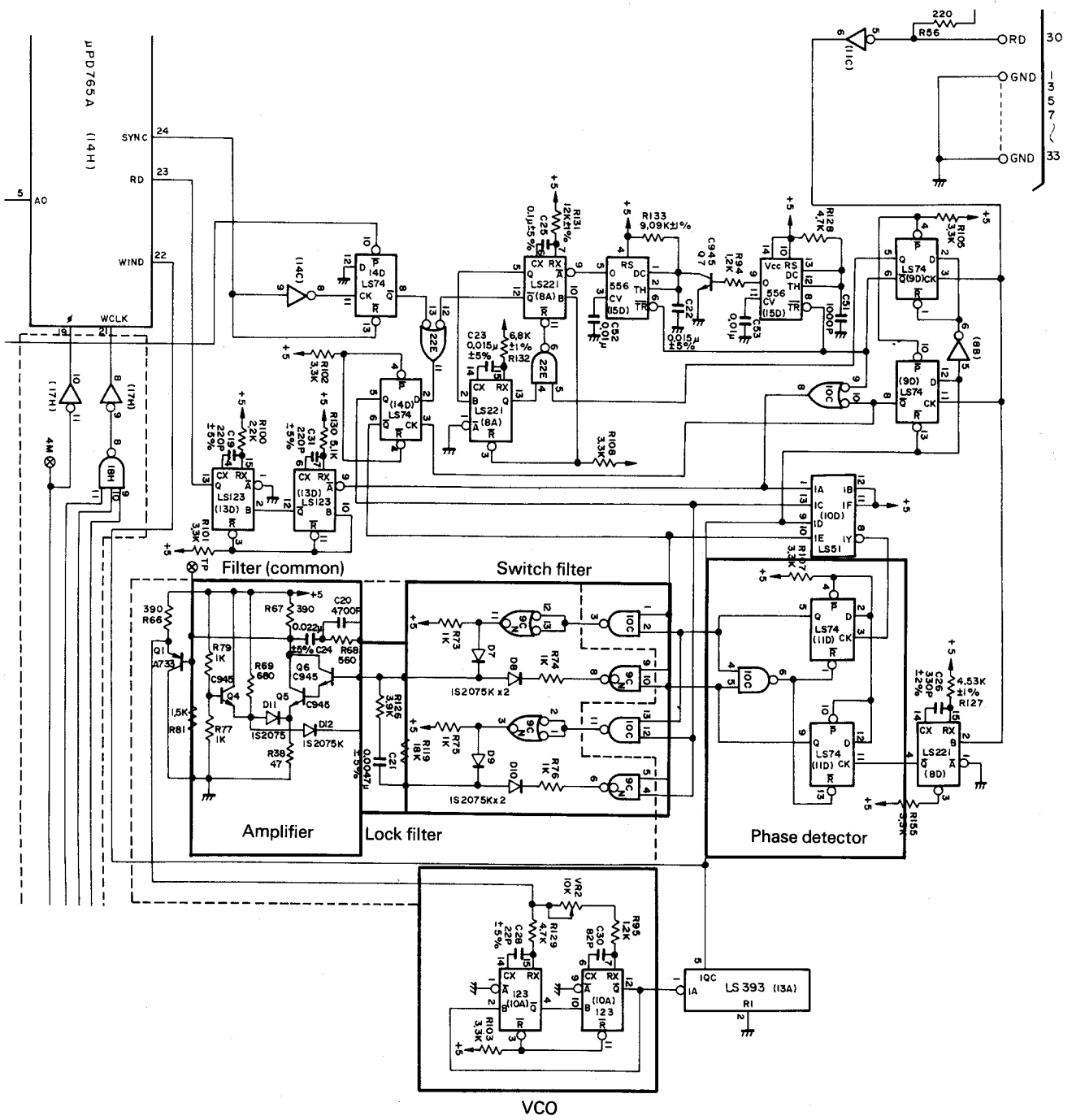


Fig. 4-36

Once synchronization is established, the VFO operates only to follow variation of bit phase resulting from variation of disk rotation speed but ignores bit phase variation due to shift of individual peaks. The operating principles of the VFO are explained below.

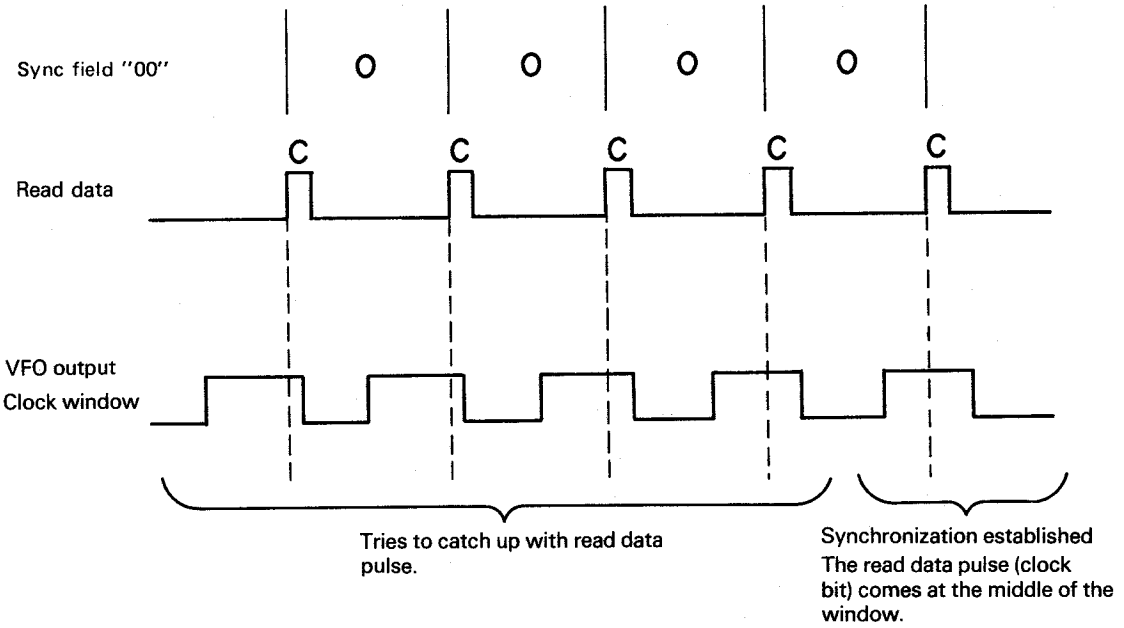


Fig. 4-37 Synchronization of the VFO

► Operation of the VFO

(1) Before establishment of synchronization

D flip-flop LS74(11D) detects phase difference of read data which is applied via one-shot LS221(8D) to pin 11 (clock input) and Clock window applied to pin 3 (clock input).

The output of flip-flop (11D) is the sync field, which is as shown in Fig. 4-40 depending on phase difference of clock inputs.

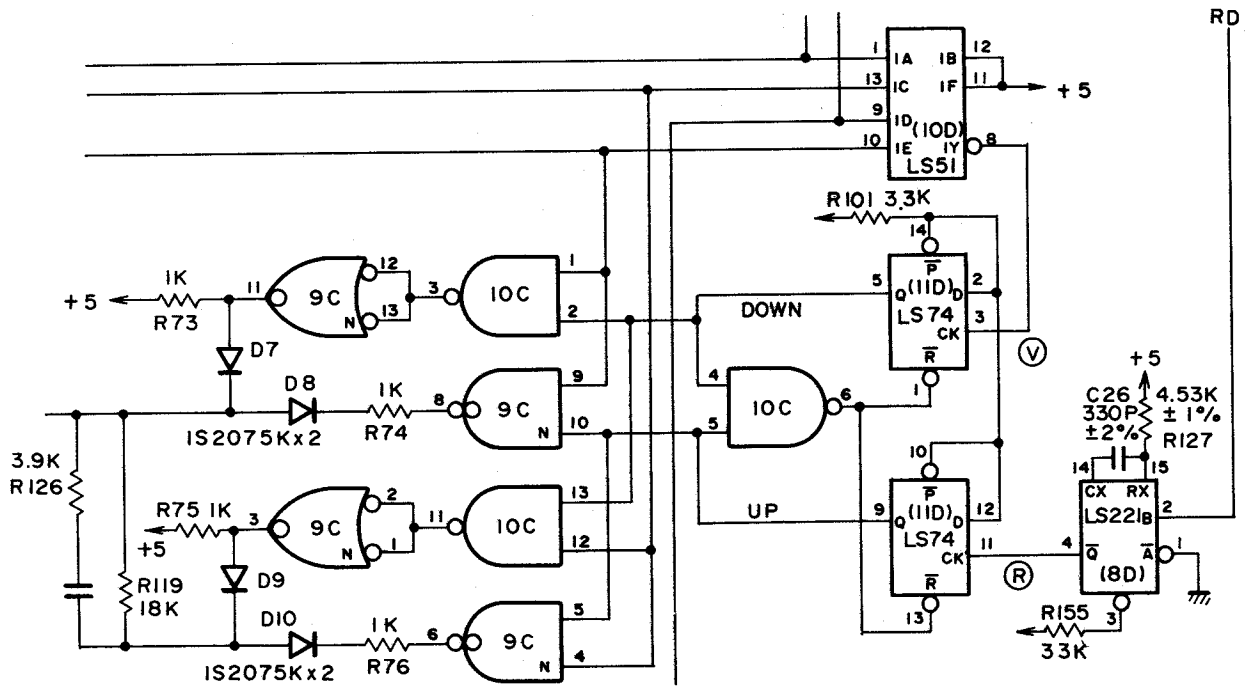


Fig. 4-38 Phase difference detector

Fig. 4-40 (a) shows the case when Clock Windows come later than clock bits of the sync field. Signal UP is High level at this time and the amplifier input is as shown in Fig. 4-40 (a) so that the frequency of the VCO becomes higher.
Fig. 4-40 (a) shows the case when Clock Windows come earlier than the clock bits of the sync field. Signal DOWN is H level in this case and the amplifier input is as shown in Fig. 4-40 (b) so that the frequency of the VCO becomes lower.
Fig. 4-40 (c) shows the case when Clock Windows are synchronized with the clock bits of the sync field. At this time, each bit of read data rises at the middle of Clock Window.

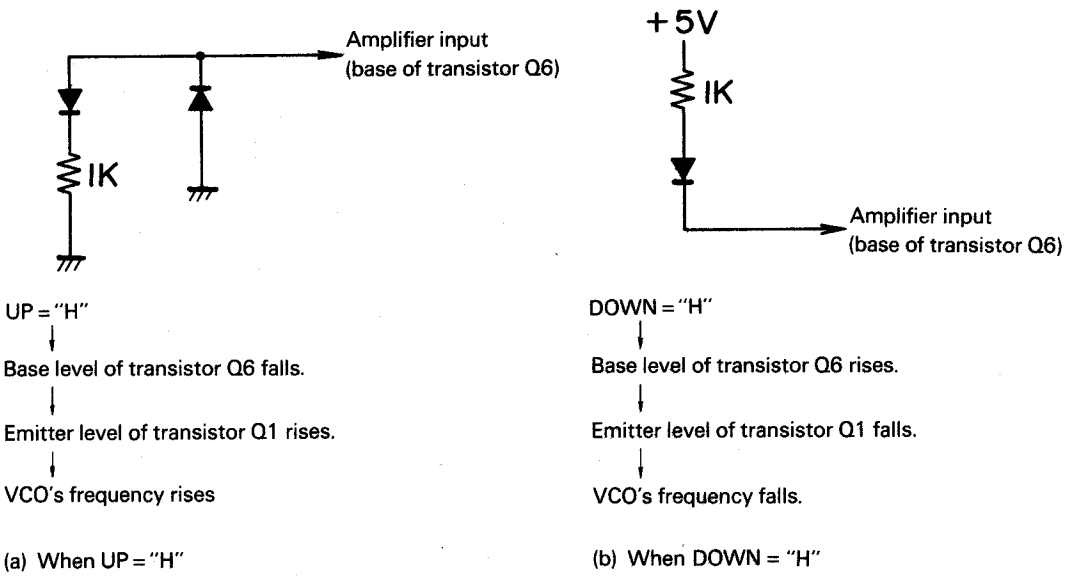


Fig. 4-39 Variations of amplifier input

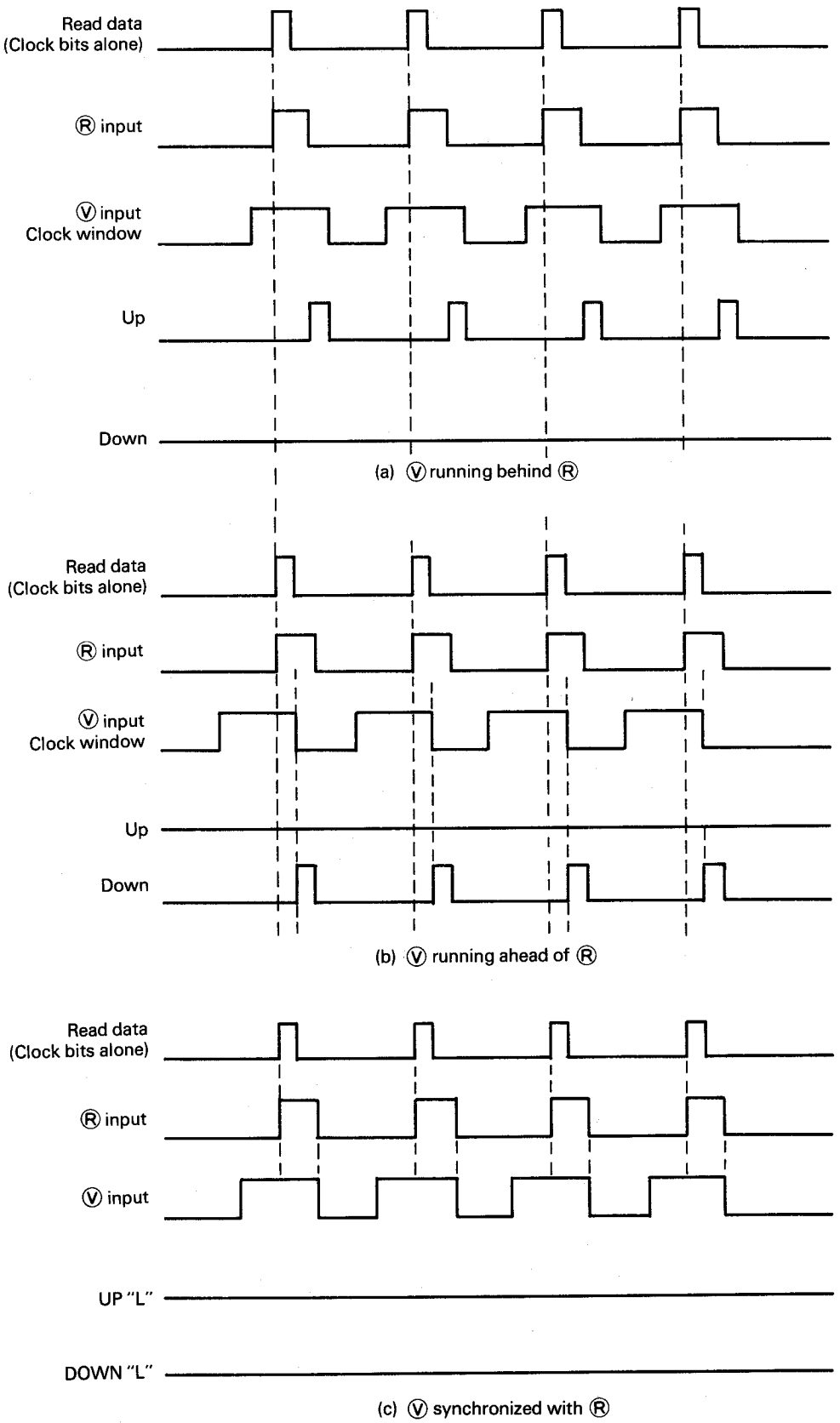


Fig. 4-40 Operation of the VFO in the sync field

(1) After establishment of synchronization

Fig.4-41 shows how the VFO operates after establishment of synchronization. Input (V) is a pulse train each bit of which rises at the rise of read data and decays at the rise or decay of Clock Window.

Since peaks of read data shift in the direction shown by the arrow, signals UP and DOWN remain at high level for the durations corresponding to the peak shifts even when Clock Window is properly timed. These signals, however, scarcely affect Clock Window because they are fed back to the oscillator via the lock filter composed of R119, R126, and C21 (see Fig. 4-36).

Thus, once synchronization has been established, the VFO operates to follow only slow phase changes due to changes of disk rotation speed, etc. but does not respond to rapid phase changes due to peak shift.

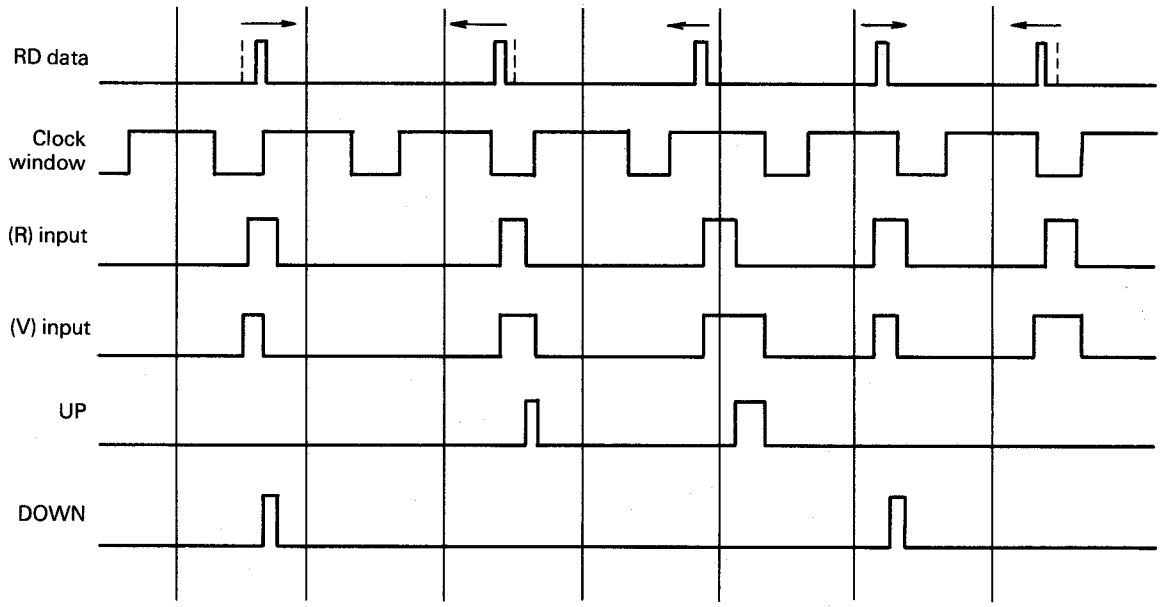


Fig. 4-41 Operation of the synchronized VFO in the data field

4.17 HD146818P (Real Time Clock Plus RAM)

► Functions

The QX-10 uses RTC (Real Time Clock Plus RAM) HD146818P to provide the following functions.

1) Clock function

The RTC updates the time and calendar RAM at the rate of once per second, and displays the time.

2) Static C-MOS RAM

A 50-byte general purpose RAM is provided. Since the RTC is backed up by the battery, the data needed to be held in the system can be stored in this RAM.

3) Generating square wave

The RTC is provided with an internal frequency divider, which generates a square wave at the SQW terminal. The wave frequency can be selected by the program.

4) Three independent interrupts

(a) Periodic interrupt

An interrupt request can be generated at the rate of once per 30μs ~ 500ms.

(b) Alarm interrupt

An interrupt request can be generated when the time set for alarm (second, minute and hour) coincides with the timing.

(c) Update ended interrupt

An interrupt request can be generated each time the time is updated.

Terminal name	I/O	Function
OSC1	I	Supplies an external pulse of 32.768 kHz. The OSC2 terminal should be set to the open state when the clock is supplied.
CKFS (Clock Out Frequency Select)	I	This terminal is an input signal to specify the CKOUT output signal dividing rate, but connected to GND as the CKOUT terminal is used.
AD0 ~ AD7	I/O	Bidirectional bus used for address information transfer or data input/output as the processor accesses the RTC. It is used for address information transfer in the first half of the cycle, and for data transfer in the latter half. The address information must be defined at the trailing edge of the M-signal. The RTC uses AD0 ~ AD5 for the address information. The data must be defined in the latter half of the cycle. The data bus driver is a three-state output buffer, which is set at the high impedance state except when the RTC outputs data.
M (Multiplexed Address Strobe)	I	A strobe signal to take in the address information from the address bus. It is composed of the write signal ($\overline{\text{IOWR}}$) to 46818 and RTC system chip select signal ($\overline{\text{CSCLK}}$). The address information is taken into the RTC at the trailing edge of this signal.
$\overline{\text{G}}$ (Data Strobe)	I	The logical products of $\overline{\text{IORD}}$ signal and chip select signal ($\overline{\text{CSCLK}}$) is input. When the CPU writes the data, the data is input at trailing edge.
$\overline{\text{W}}$ (Read/Write)	I	When CPU reads the RTC, this signal holds high. When CPU writes the RTC data, this signal becomes low.
$\overline{\text{CS}}$ (Chip Select)	I	This signal is the reverse logic of reset signal. It is low level except under reset.
$\overline{\text{IRQ}}$ (Interrupt Request)	O	A signal to request the CPU to make an interrupt. Pulled up to +5V and active low level.
$\overline{\text{RES}}$ (Reset)	I	Supplied by the power on reset signal. The RTC is reset by this signal, but the functions of the clock calendar RAM are not influenced.
PS (Power Sense)	I	Supplied from the address line A7. After initializing the RTC contents, the CPU sets this bit to "1" to prepare for power down or other power failure.

Table 4-16

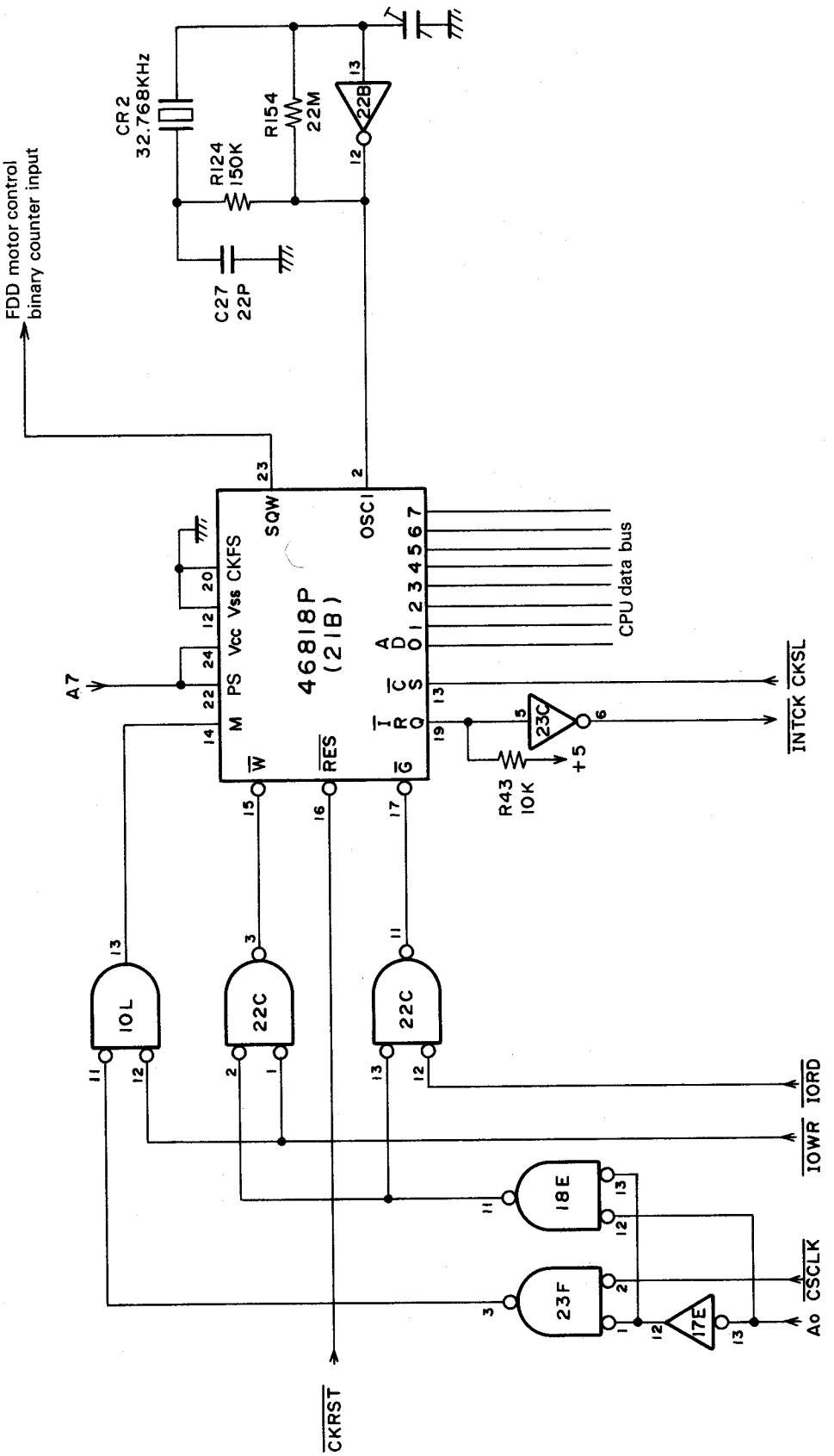


Fig. 4-42 Real time clock plus RAM 46818

4.18 DMA Controller μPD8237AC

The programmable DMA controller μPD8237 with four independent channels as shown in Fig. 4-43 is used.

Two DMA controllers are connected in two-stage cascade to provide seven channels. In this case, the μPD8237 (21J) works as a master and the μPD8237 (19J) as a slave.

HRQ and HLA signals of the slave DMA controller are connected to the 4th channel of the master controller.

Channel 0 is given the highest priority. The priority in this circuit is as shown in Table 4-17.

When the service of one channel is accepted, the service of the other channels can not be accepted until the service of that channel is completed.

Channel		Connection	
Master	1	Floppy disk	High
	2	Monitor	
	3	Option slots (One of OP # 1 through OP # 5)	
			Priority
Slave	1	Option slots (OP # 1)	
	2	Option slots (OP # 2)	
	3	Option slots (OP # 3)	
	4	Option slots (OP # 4)	Low

Table 4-17

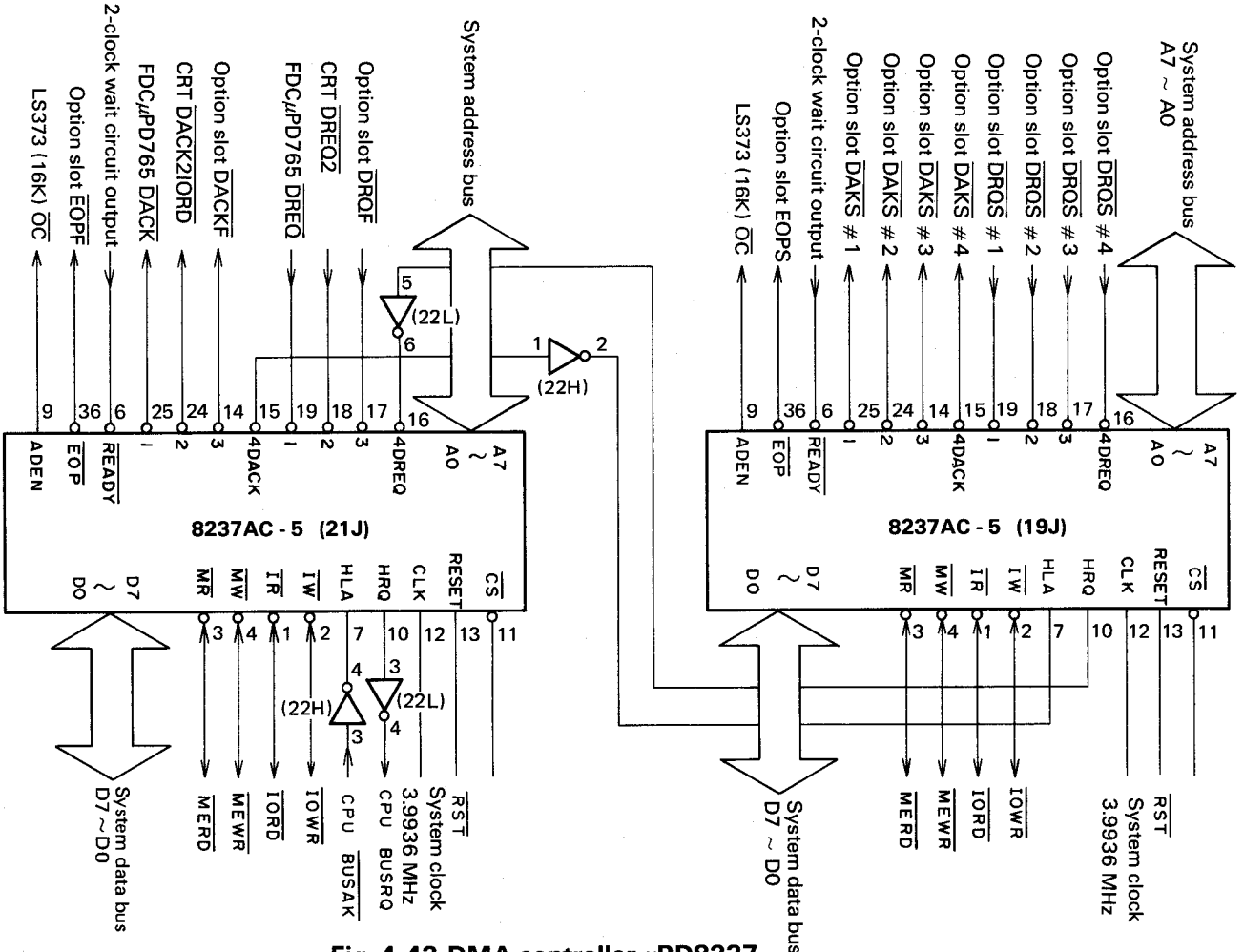


Fig. 4-43 DMA controller μPD8237