TECHNICAL MANUAL
QX-10
ALL BUSINESS COMPUTER SYSTEM

This Technical Manual provides technical information on the structure, principles of operation of the QX-10. Major techincal modifications, if made in the future, will be notified through Service Bulletins, and the Technical Manual should be revised accordingly. The details of the Manual are subject to change without notice.

All the information given in the Manual concerns the QX-10, and we are not responsible for any troubles with the industrial copyright of a third party that might arise from your application of the Manual to other products or from the connection of the QX-10 to others.

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CHAPTER 1
GENERAL

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1.1 General

The QX-10 is an all business computer system. It consists of a Z80A-compatible CPU, a memory of 256 KB maximum, two floppy disk drives of double-sided, double-density, 5-1/4" disks, and a 12" full-graphic CRT display with a resolution of 640 by 400 dots.

The standard configuration includes a programmable timer, Centronics-compatible printer interface, RS-232C interface, C-MOS RAM backed up by battery, clock and calendar, and separate keyboard. It has five card slots which permit installation of optional cards as required.

Optional cards available include character generators of varying fonts, GP-IB interface, optical fiber interface, color CRT interface, and pulse transformer interface.

1.2 Hardware configuration

1.2.1 General

The QX-10 is composed of three units: the main system unit, the keyboard unit, and the monitor unit.

The main system unit, the heart of the QX-10 system, includes the main circuit board, sub circuit board, power supply, two 5-1/4" floppy disk drives developed by Epson, and five slots permitting installation of optional cards.

The keyboard unit is connected to the main system unit with a curled cord through which signals may be transmitted in any direction.

The standard monitor unit is a 12" high resolution green monitor capable of displaying bit images.

1.2.2 Hardware

Main system

CPU	μPD780AC-1 (Z80A compatible, 4 MHz)	
Memory	RAM	: 256 KB (maximum on main board)
	VIDEO RAM	: 128 KB (maximum on CRT board)
	C-MOS RAM	: 2 KB (standard, backed up by battery)
	EPROM	: 2/4/8 KB (for IPL)
Clock	C-MOS real-time clock (backed up by battery)	
Speaker	Permanent magnet speaker	
Interfaces	Printer interface (Centronics-compatible)	
	RS-232C communications interface	
DMA	7 channels	
Interrupt levels	15	
Counter/timer	6 channels	
FDD	5-1/4" FDD x 2	
	320 KB x 2 drives	
	48 TPI, double sided & double density	
Card slots	5	
Monitor	12" green monitor	
	640 x 400 dots	
Keyboard	ASCII, HASCI	

1.3 Specifications

1.3.1 External Dimensions and Weight

(1) External dimensions

		(W)		(D)	(H)
Main system unit	ca.	508	×	340	× 103 (mm)
Green monitor unit	ca.	312	×	340	× 270 (mm)
Keyboard unit	ca.	508 (510)	×	224	× 48 (mm)
Optional card		280	×	80	(mm)

(2) Weight: approx. 18kg

1.3.2 Environmental Conditions

(1) Temperature	during operation	:	5°C to 40°C
	storage	:	–30°C to 70°C
(2) Humidity.....	during operation	:	10 – 80% (no condensation)
	storage	:	10 – 90% (no condensation)
(3) Resistance to shock	during operation	:	max. 1 G, 1 msec
	storage	:	max. 5 G, 1 msec
(4) Resistance to vibration....	during operation	:	max. 0.25 G, 5-50 Hz
	storage	:	max. 3 G, 5-50Hz

CHAPTER 2
HARDWARE CONFIGURATION

CONTENTS

2.1 Hardware Configuration

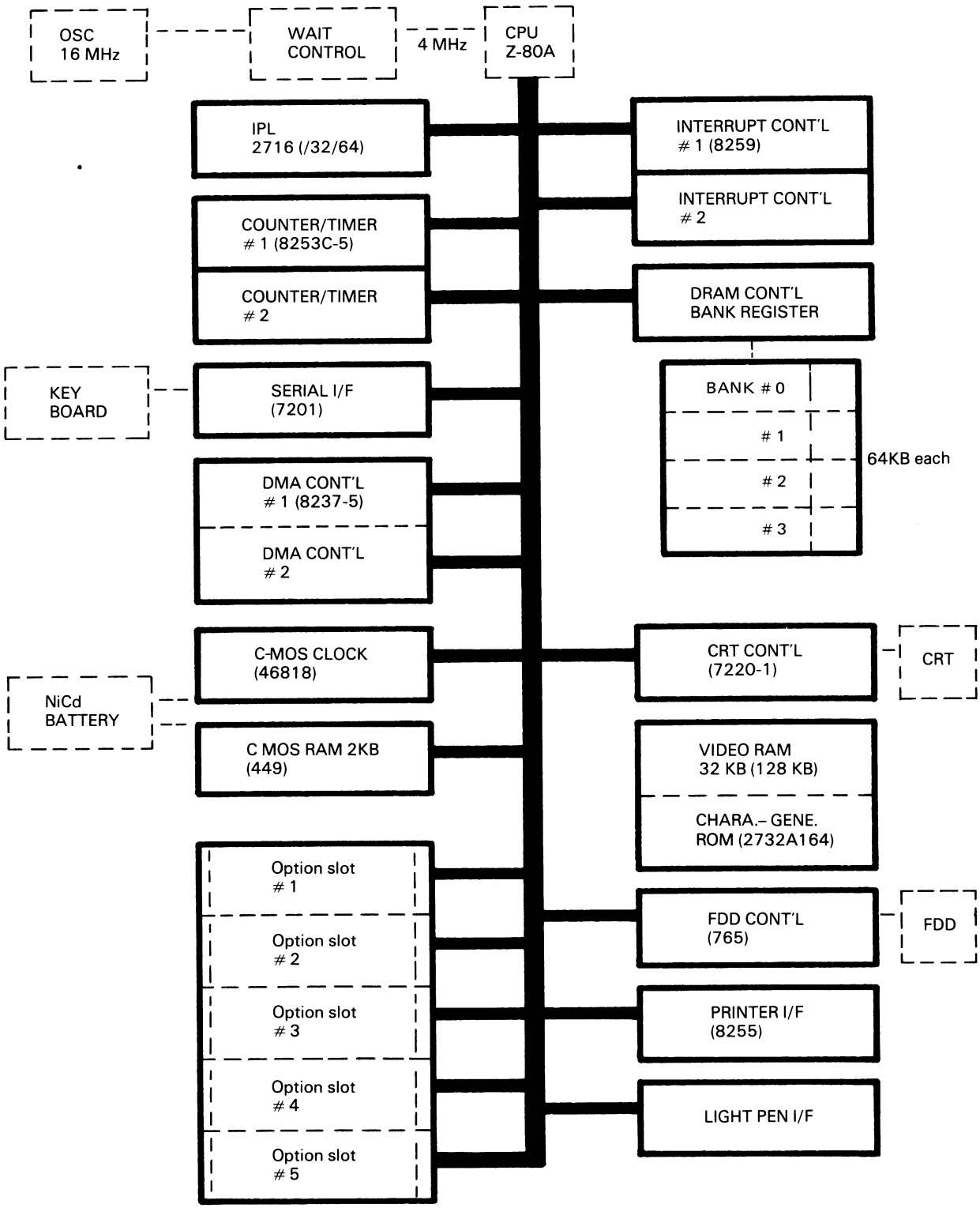


Fig. 2-1

2.2 Interfaces

2.2.1 Connector Locations

The QX-10's main circuit board (Q10SYM board) is provided with 19 connectors (including five connectors for option card slots) which connect to other circuit boards or peripheral devices through cables as shown in QX-10 system layout.

The connectors of the Q10SYM board are summarized below. (Table 2-1)

Connector	Pins	Connected to:
CN1	8	Keyboard
CN2	25	RS-232C
CN3	36	Printer (Centronics type)
CN4	8	CRT unit
CN5	5	Light pen
CN6	34	FDD control signals
CN7	10	FDD power
CN8	13	Power (from Q10PS board)
CN9	22	Control signals (to Q10GMS board)
CN10	22	Control signals (to Q10GMS board)
CN11	6	Power check terminals
CN12	3	NiCd battery
CN13	2	Fan motor power
CN14	2	PWD signal for option cards
Option slots #1 – #5	60	Option card control signals and power

Table 2-1

2.2.2 connector CN1 (connector to the keyboard)

(a) Use : connection to keyboard control signal lines

(b) Type: DIN 8-pin, TCS4490

Pin No.	Signal Symbol	Signal Direction	Description of Signal
1	RXD	OUT	Received data
2	CLK	OUT	Clock
3	+12	OUT	+12V
4	TXD	IN	Transmitted data
5	GL	–	Ground
6	GL	–	Ground
7	GL	–	Ground
8	GL	–	Ground

Note: The direction of signal is as viewed from the Q10SYM board.

Table 2-2

2.2.3 Connector CN2 (RS-232C interface)

(a) Use : for interface to a coupler or development unit

(b) Type: 25-pin, cannon, female, GMM-25HUFDA

Pin No.	Signal Symbol	Signal Direction	Description of Signal
1	FG	–	Frame ground
2	TXD	OUT	Transmitted data
3	RXD	IN	Received data
4	RTS	OUT	Request to send
5	CTS	IN	Clear to send
6	DSR	IN	Data set ready
7	GL	–	Signal ground
8	DCD	IN	Carrier detect
9-10	–	–	NC (unused)
11	REV	OUT	Reverse channel
12-14	–	–	NC (unused)
15	DB	IN	Transmitter signal element timing
16	–	–	NC (unused)
17	RXC	IN	Receiver clock
18-23	–	–	NC (unused)
24	TXC	OUT	Transmitter clock

Note: The direction of signal is as viewed from the Q10SYM board.

Table 2-3

2.2.4 Connector CN3 (printer interface)

(a) Use : for interface to a Centronics-type printer

(b) Type: 36 pins, HONDA ADS-36BLFD

Pin No.	Signal Symbol	Signal Direction	Description of Signal
1	$\overline{STB}$	OUT	Strobe
2	DB0	OUT	Data line 0
3	DB1	OUT	Data line 1
4	DB2	OUT	Data line 2
5	DB3	OUT	Data line 3
6	DB4	OUT	Data line 4
7	DB5	OUT	Data line 5
8	DB6	OUT	Data line 6
9	DB7	OUT	Data line 7
10	$\overline{ACK}$	IN	Acknowledge
11	$\overline{RDY}$	IN	Ready
12	$\overline{NPA}$	IN	No paper
13	$\overline{SLO}$	IN	Select out
14	$\overline{ALF}$	OUT	Auto line feed
15	–	–	NC (unused)
16	GL	–	Signal ground
17	FG	–	Frame ground
18	–	–	NC (unused)
19-30	GL	–	Signal ground
31	$\overline{RST}$	OUT	Reset
32	$\overline{ERR}$	IN	Error
33	GL	–	Signal ground
34	–	–	NC (unused)
35	$\overline{PWF}$	IN	Power failure
36	–	–	NC (unused)

Note: The direction of signal is as viewed from the Q10SYM board.

Table 2-4

2.2.5 Connector CN4 (CRT drive unit interface)

(a) Use : for interface between the Q10GMS board and the CRT drive unit

(b) Type: DIN, 8 pins, TCS4480

Pin No.	Signal Symbol	Signal Direction	Description of Signal
1	+12C	–	+12V
2	GP	–	Ground
3	–	–	NC (unused)
4	H. SYNC	OUT	Horizontal sync
5	V. SYNC	OUT	Vertical sync
6	GL1	–	Ground
7	GL2	–	Ground
8	VIDEO	OUT	Video signal
E	FG	–	Frame ground

Note: The direction of signal is as viewed from the Q10SYM board.

Table 2-5

2.2.6 Connector CN5 (light pen interface)

(a) Use : for interface to a light pen

(b) Type: DIN, 5 pins TCS4420.

Pin No.	Signal Symbol	Signal Direction	Description of Signal
1	+5V	–	+5V
2	SIG	IN	Light pen signal
3	+12C	–	+12V
4	SW	IN	Light pen switch
5	GP	–	Ground
E	FG	–	Frame ground

Note: The direction of signal is as viewed from the Q10SYM board.

Table 2-6

2.2.7 Connector CN6 (FDD interface)

(a) Use : connection to FDD control signal lines

(b) Type: 34 pins, male, 3M P/N 3463-0001 or equivalent

Pin No.	Signal Symbol	Signal Direction	Description of Signal
2	–	–	NC (unused)
4	HLD	OUT	Head load
6	US3	OUT	Drive select 3
8	INDX	IN	Index
10	US0	OUT	Drive select 0
12	US1	OUT	Drive select 1
14	US2	OUT	Drive select 2
16	MT	OUT	Motor on
18	DIR	OUT	Direction
20	STP	OUT	Step
22	WD	OUT	Write data
24	WG	OUT	Write gate
26	T0	IN	Track 00
28	WRT	IN	Write protect
30	RD	IN	Read data
32	HDS	OUT	Side select
34	RDY	IN	Ready

Note: 1. All odd number pins (1-33) are "ground".

2. The direction of signal is as viewed from the Q10SYM board.

Table 2-7

2.2.8 Connector CN7 (connector to the FDD power supply)

(a) Use : connection to the FDD power supply

(b) Type: 10 pins, male, AMP P/N 1-480424-0 or equivalent

Pin No.	Signal Symbol	Signal Direction	Description of Signal
1	LED	–	Power (+5V) of power indicator LED
2	GL	–	Signal ground
3	GP	–	Signal ground
4	GP	–	Signal ground
5	+12F	–	+12V
6	+12F	–	+12V
7	GL	–	Signal ground
8	GL	–	Signal ground
9	+5	–	+5V
10	+5	–	+5V

Table 2-8

2.2.9 Connector CN8 (power lines connector)

(a) Use : connection of power lines from the Q10PS board

(b) Type: 13 pins, male, 5271-6A

Pin No.	Signal Symbol	Signal Direction	Description of Signal
1	PWD	–	For power failure detection
2	GND	–	Ground of +5V
3	GND	–	Ground of –12V
4	GND	–	Ground of +12L
5	GP	–	Ground of +12V
6	GP	–	Ground of +12V
7	+5V	–	+5V for logics
8	+5V	–	+5V for logics
9	+5V	–	+5V for logics
10	–12V	–	–12V
11	+12L	–	+12V for logics
12	+12F	–	+12V for FDD
13	+12D	–	+12V for CRT

Table 2-9

2.2.10 Connector CN9 (Q10GMS interface)

(a) Use : connection of the data bus and power lines to the Q10GMS board

(b) Type: 22 pins, male, HKP-22FD2-2 (HONDA)

Pin No.	Signal Symbol	Signal Direction	Description of Signal
1	−12V	–	−12V
2	−12V	–	−12V
3 – 4	–	–	NC (unused)
5	+12L	–	+12V
6	+12L	–	+12V
7	+5V	–	+5V
8	+12L	–	+12V
9	+5	–	+5V
10	+5V	–	+5V
11	D0	IN/OUT	Data line 0
12	D1	IN/OUT	Data line 1
13	D2	IN/OUT	Data line 2
14	D3	IN/OUT	Data line 3
15	D4	IN/OUT	Data line 4
16	D5	IN/OUT	Data line 5
17	D6	IN/OUT	Data line 6
18	D7	IN/OUT	Data line 7
19	GL	–	GND
20	GL	–	GND
21	GL	–	GND
22	GL	–	GND

Table 2-10

2.2.11 Connector CN10 (Q10GMS interface)

(a) Use : connection of the control signal lines to the Q10GMS board

(b) Type: 22 pins, male, HKP-22FD 2-2 (HONDA)

Pin No.	Signal Symbol	Signal Direction	Description of Signal
1	GL	–	Ground
2	GL1	–	Ground
3	$\overline{\text{DACK2}}$	IN	DMA acknowledge
4	GL2	–	Ground
5	–	–	–
6	VIDEO	IN	Video signal
7	V. SYNC	IN	Vertical sync
8	–	–	–
9	$\overline{\text{IORD}}$	OUT	Read data
10	A0	OUT	Address line 0
11	SIG	OUT	Light pen signal
12	$\overline{\text{IOWR}}$	OUT	Write data strobe
13	$\overline{\text{CSCCR}}$	OUT	CRT drive board select
14	$\overline{\text{DREQ2}}$	OUT	DMA transfer request
15	$\overline{\text{RESET}}$	OUT	Reset
16	$\overline{\text{INTCR}}$	IN	Light pen interrupt request
17	SW	OUT	Light pen switch
18	H. SYNC	IN	Horizontal sync
19	–	–	NC (unused)
20	–	–	NC (unused)
21	A1	OUT	Address line 1
22	$\overline{\text{CSCRT}}$	OUT	CRT drive board select

Note: The direction of signal is as viewed from the Q10SYM board.

Table 2-11

2.2.12 Connector CN11 (supply voltage checkpoint terminals)

(a) Use : for checking supply voltages

(b) Type: 6 pins, 3022-7A

Pin No.	Signal Symbol	Signal Direction	Description of Signal
–	5V GL	–	Ground of +5V
–	GP	–	Ground of +12V
–	12C	–	+12V for CRT
–	12L	–	+12V for logics
–	12F	–	+12V for FDD
–	–12V	–	–12V

Table 2-12

2.2.13 Connector CN12 (connector to NiCd battery)

(a) Use : for supplying C-MOS ICs with backup power

(b) Type: 3 pins, ADS-36 BLFDR1

Pin No.	Signal Symbol	Signal Direction	Description of Signal
A	–	–	Ground
B	–	–	Voltage for charging NiCd battery
C	–	–	+3.6V

Table 2-13

2.2.14 Connector CN13 (fan motor power lines connector)

(a) Use : connection of the cooling fan motor power lines

(b) Type: 2 pins, 5045-3A

Pin No.	Signal Symbol	Signal Direction	Description of Signal
–	+12	–	+12V
–	G	–	Ground

Table 2-14

2.2.15 Connector CN14 (PWD signal for option card)

(a) Use: : for supplying PWD signal to external device

(b) Type: 2 pins, 5045-2A

Pin No.	Signal Symbol	Signal Direction	Description of Signal
1	PWD	OUT	Power Down signal
2	–	–	–

Table 2-15

2.2.16 Connector CN15 (option card slots #1 ~ #5)

(a) Use : option cards connector

(b) Type: 60 pins, female, DDK 225D-10030C2-23

Pin No.	Signal Symbol	Signal Direction	Description of Signal
1 – 2	GND	–	Ground
3 – 10	DTB0 – 7	IN/OUT	Data bus
11 – 12	–12V	–	–12V
13 – 28	ADR0 – 15	OUT	Address bus
29 – 30	GND	–	Ground
31	CLK	OUT	system clock
32	GND	–	Ground
33	$\overline{\text{BSAK}}$	OUT	Bus acknowledge
34	$\overline{\text{MEMX}}$	OUT	External memory select
35	$\overline{\text{IRD}}$	OUT	I/O read
36	$\overline{\text{IWR}}$	OUT	I/O write
37	$\overline{\text{MRD}}$	OUT	Memory read
38	$\overline{\text{MWR}}$	OUT	Memory write
39	$\overline{\text{RSIN}}$	IN	Reset input
40	INT(H)1	IN	High-priority external interrupt
41	INT(H)2	IN	High-priority external interrupt
42	INT(L)	IN	Low-priority external interrupt
43	+5V	–	+5V
44	$\overline{\text{RSET}}$	OUT	Reset output
45 – 46	+5V	–	+5V
47	$\overline{\text{DRQ(F)}}$	IN	DMA request
48	$\overline{\text{DRQ(S)}}$	IN	DMA request
49	$\overline{\text{RDY(F)}}$	IN	DMA ready
50	$\overline{\text{RDY(S)}}$	IN	DMA ready
51	$\overline{\text{WAIT}}$	IN	Wait
52	$\overline{\text{IWS}}$	OUT	I/O write short
53	$\overline{\text{DAK(F)}}$	OUT	DMA acknowledge
54	$\overline{\text{DAK(S)}}$	OUT	DMA acknowledge
55	$\overline{\text{EOP(F)}}$	OUT	End of process
56	$\overline{\text{EOP(S)}}$	OUT	End of process
57 – 58	+12V	–	+12V
59 – 60	GND	–	Ground

Table 2-16

CHAPTER 3
POWER SUPPLY UNIT

CONTENTS

3.1 General

The power supply is mounted in Q10PS board. It supplies power to the logic keyboard, FDD and CRT. The block diagram is shown in Fig. 3-1. It shows the voltage multiplying rectifier which can be switched to input voltage range 100/115V AC and 220/240V AC. The internal jump wire is used for voltage switching.

The primary control circuits are simplified using hybrid ICs, and amplify oscillation pulses of about 30 kHz to drive the primary side of the transformer (T1).

The voltage taken from the secondary side of the transformer is rectified, smoothed and regulated to provide necessary DC power. Voltage stabilization is achieved by monitoring +5V by IC and controlled by varying the duty of the oscillation frequency. Excess voltage/current inhibitor protects the load side elements from destruction.

Another feature is the PWD signal circuit, which detects sudden AC voltage drop and causes an interruption in the main circuit CPU.

3.2 Specifications of Q10 PS board (Power Supply Unit)

(1) Input voltage: 100V channel 100V − 10% ~ 120V + 10%
200V channel 220V − 10% ~ 240V + 10%

(2) Frequency: 50/60 Hz

(3) Power consumption: Approx. 75W

(4) Input serge current: 30A for 20ms maximum

(5) Leak current: 1 mA maximum

(6) Insulation strength: 100V channel Can withstand 1 kV applied between AC power supply and case for 1 minute.
200V channel Can withstand 1.25 kV applied between AC power supply and case for 1 minute.

(7) Output Voltage:

output voltage	limits of output voltage	standard current	ripple voltage (mV p-p)
+5	5.0 ~ 5.1V	3.6A	100 mA
+12(C)	11.6 ~ 12.4V	0.9A	50 mA
+12(F)	11.4 ~ 12.6V	1.2A	200 mA
+12(L)	11 ~ 13V	0.45A	200 mA
−12	−11 ~ −13V	0.02A	200 mA

(8) Insulation resistance: 10 MΩ for 500V DC minimum.

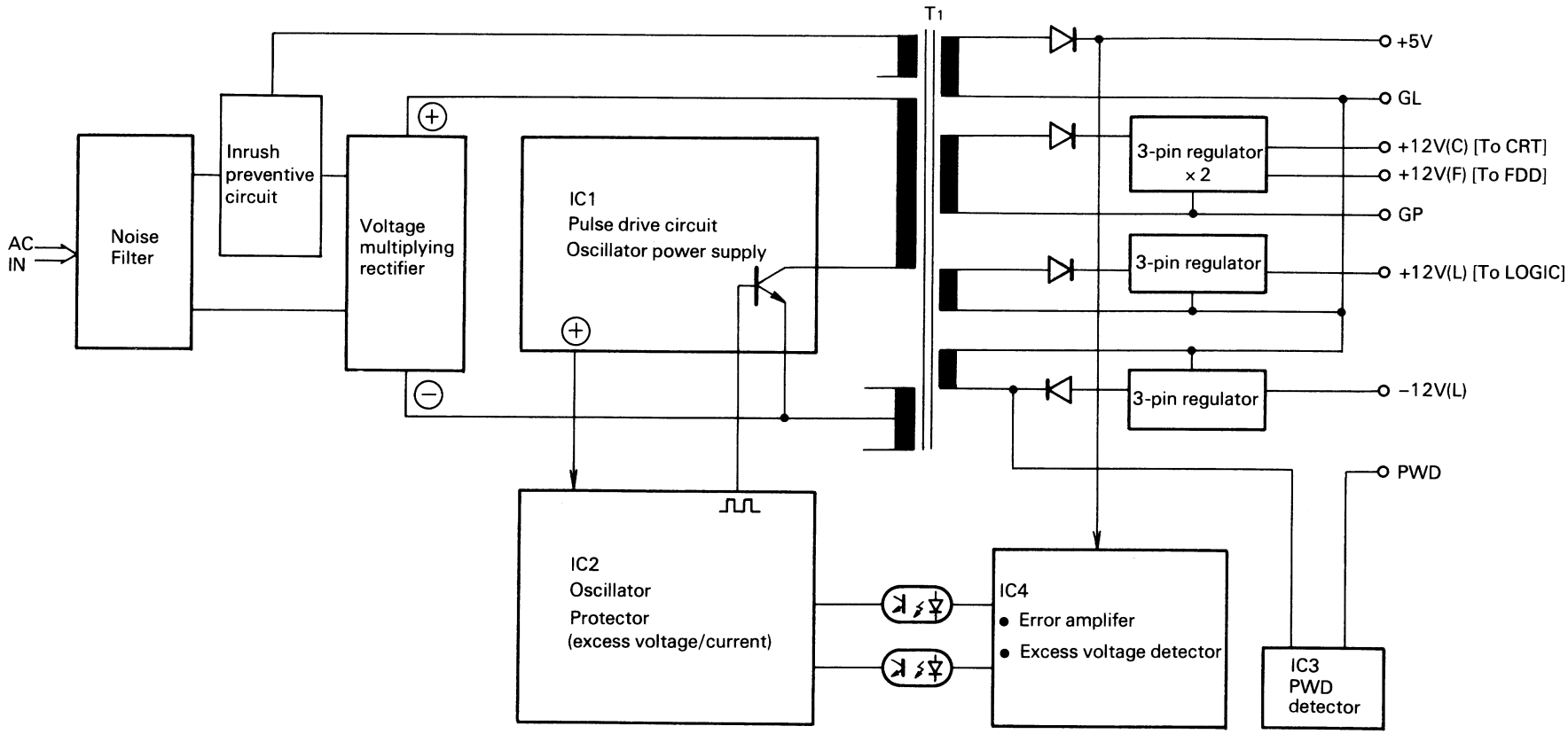


Fig. 3-1 Power Supply Block Diagram (Q10PS)

3.3 Noise Filter

(C17, M1, C18, L4, L5, C20, C21, M2, C19, C22 and C23)

- The noise filter prevents a malfunction due to input surge voltage and input feedback noise (noise generated inside is not transferred to the AC line).

3.4 Inrush Preventive Circuit

(TY1, R2, R9, D5 and R7)

- This circuit prevents parts such as DB1 from being damaged by the large current which flows in C1 and C2 when the power is turned on.

(1) Functions

- R2 limits the current flow when the power is turned on.
- When the oscillator operates normally, the voltage of T1 turns on TY1 (triode AC switch) to allow the current to flow.
  If R2 is abnormally heated, the inrush protective circuit is not operating normally.

3.5 Voltage Multiplying Rectifier

(DB1, C1, C2 and J1)

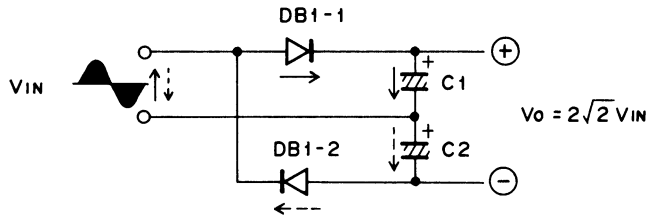


Fig. 3-2 Basic Circuit

In Fig. 3-2, DB1-1 conducts first, and C1 is charged with the maximum AC voltage Vm. In the next half cycle, DB1-2 conducts, the C1 charging voltage and supply voltage are applied in the same direction, and double voltage appears.

- When J1 is connected.....100V AC input channel
  The voltage of 100V AC input channel (Japan, U.S.A. and Canada) is multiplied and rectified to match the 200V channel (Europe).
- When J1 is not connected.....200V AC input channel
  The voltage of 200V AC channel is normally bridge rectified.

3.6 Oscillator Power Supply and Pulse Drive Circuit

(IC1 and peripheral parts)

a. Oscillator power supply

(R3, R5, C15, L1, (D1), (D2) and (Q1)) Parts in ( ) contained in IC1.

a-1 When not oscillating (at starting or through failure)

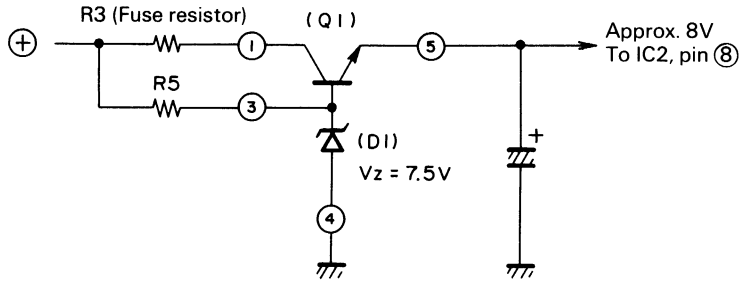


Fig. 3-4

About 8V is produced by the ordinary dropper and applied to pin 8 of IC2 (oscillator power supply) to make oscillation.

a-2 When oscillating

The pulse generated in IC2 is applied to IC1 to drive T1 inside. Then, the voltage generated by T1 is stabilized by L1 (D2), and about 9V is applied to pin 8 of IC2 (switched from the operation of Q1 in a-1) to continue oscillation.

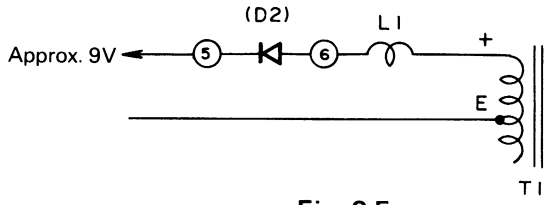


Fig. 3-5

a-3 Action for fault

When oscillation stops for any reason (not switched to the operation of a-2), R3 (fuse resistor) blows to stop power (for about 2 minutes or longer after stop of oscillation).

b. Pulse Drive Circuit

((Q2), (Q3), (Q4), (D3), L2 and C16) Parts in ( ) are contained in IC1.

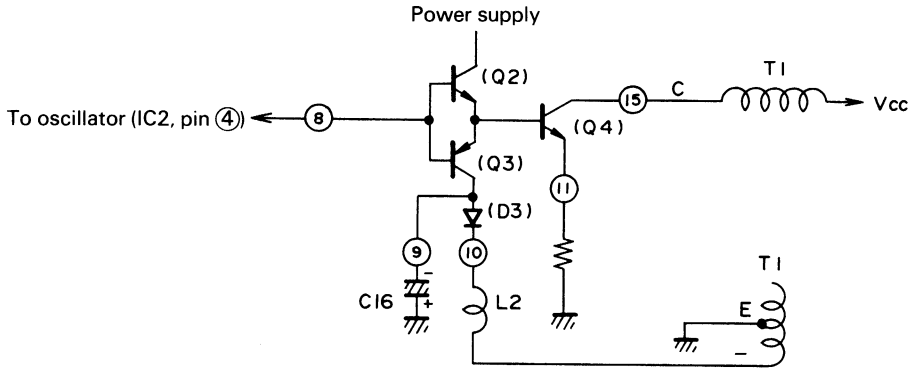


Fig. 3-6

The pulse from the generator is amplified by (Q2) and (Q3) to turn (Q4) on and off, thereby driving T1. Negative power supply (approx. 9V) is obtained by the voltage of T1 through L2, (D3) and C16. R4, C25, C24 and D1 near the D-terminal of T1 coil form a counter electromotive force preventive circuit.

3.7 Oscillator and Protector

(IC2 and peripheral parts)

a. Oscillator

((IC-1), (IC-2), (R1), (R2), (C1) and (C2)) Parts in ( ) are contained in IC2.

An oscillator of about 30 kHz.

b. Excess voltage protector

((Q2), (Q3), (R10), (R11), (IC-3) and PC1) Parts in ( ) are contained in IC2.

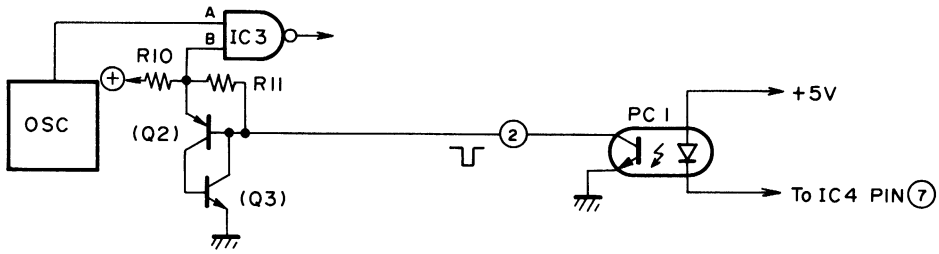


Fig. 3-7

The output voltage of +5V rises to something over 8V, IC4 controls to light up the light emitting diode of PC1, and the photo-transistor turns on. since (Q2) and (Q3) in IC2 are made in thyristor connection, when PC1 works even once, they turn off the gate (B) of (IC-3), preventing oscillation output until the power is turned on again.

c. Voltage stabilizer

(PC2, (R6) and (IC-3)) Parts in ( ) are contained in IC2.

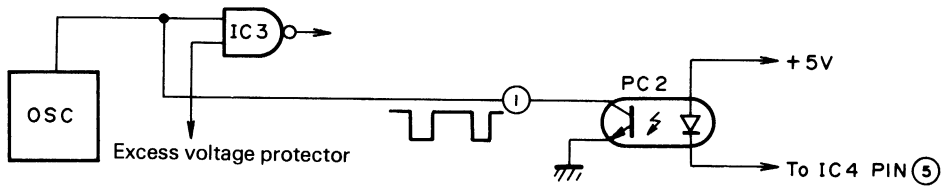


Fig. 3-8

The voltage of the +5V line is detected by the error amplifier in IC4. When the voltage rises, exceeding the reference value, PC2 works to lower the voltage at the pin ① of IC2. By setting the gate of (IC-3) to high and low, the oscillation duty is varied to keep the voltage at a constant level.

d. Excess current protector

(R1, R10, R16, (R3), (R4), (R5) and (Q1)) Parts in ( ) are contained in IC2.

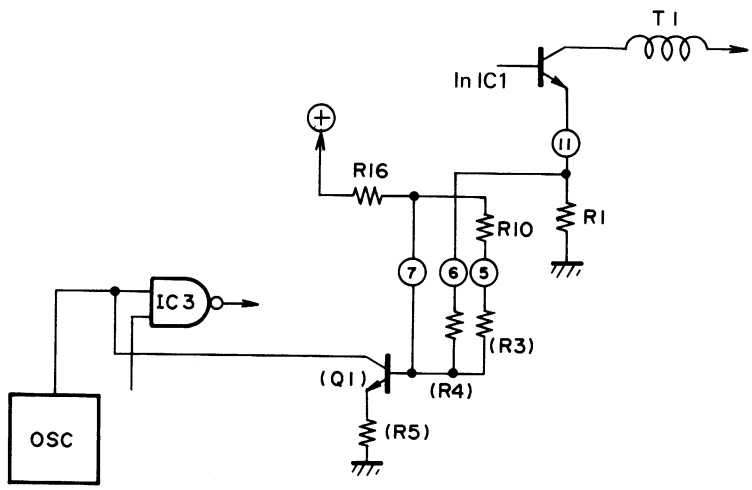


Fig. 3-9

The voltages at both ends of R1 are detected by (Q1) of IC2. When the output is overloaded, the gate of (IC-3) is set to low and the oscillation output is stopped.

* Operates when overloaded at full load.

+5V..... 7A
+12C 2A
+12F..... 2A
+12L..... 0.5A
−12..... 0.5A

} Operates at +α

Does not operate when overloaded only at +5V.

3.8 Error Amplifier and Excess Voltage Detector (IC-4)

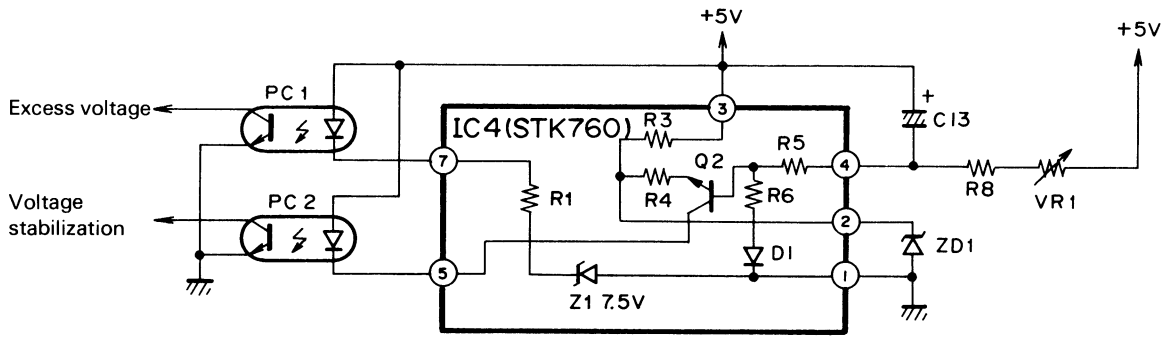


Fig. 3-10 IC Circuit

a. Error amplifier
(PC1, C13, R8, VR1, ZD1, (R3), (R4), (R5), (R6), (D1) and (Q2)) Parts in ( ) are contained in IC4.

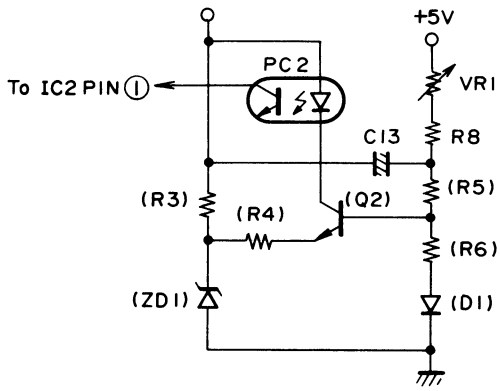


Fig. 3-11

The voltage on the +5V line is detected and when it is lower than the reference voltage, PC2 works to set the pin ① of IC2 to low, and the oscillation duty is changed to stabilize the voltage VR1 adjusts +5V when full load is connected.

b. Excess voltage detector
(PC1, (R1) and (Z1)) Parts in ( )are contained in IC4.
+5V is checked by Z1 (Vz = 7.5V) and when it is found to be over 8V, oscillation is stopped through PC1.

3.9 PWD (Power Down) Detector (IC-3)

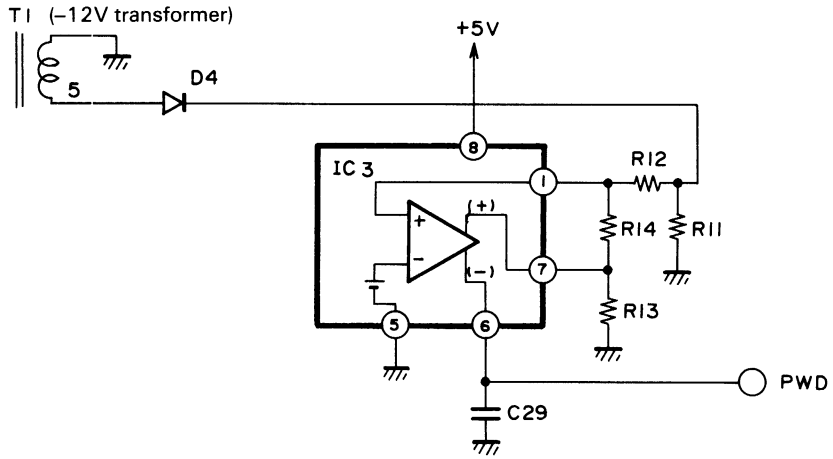


Fig. 3-12

The voltage rectifying the pin ⑤ of T1 indirectly monitors the input voltage by utilizing its characteristic proportional to the input voltage of the AC line. PWD signal is output immediately before the output voltage goes unstable due to power failure or momentary power loss, causing an interrupt of highest priority in CPU.

100V AC channel ..... The PWD signal goes high at about 80V AC.

200V AC channel ..... The PWD signal goes high at about 160V AC.

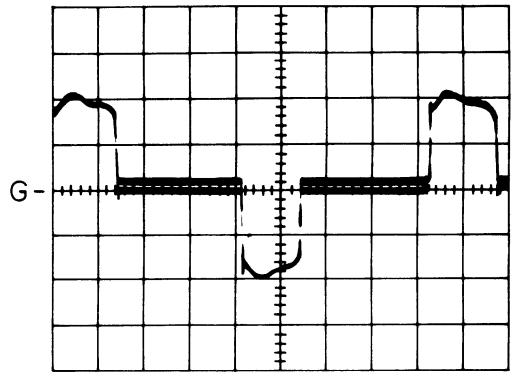
3.10 Voltage Output Circuit

a. +5V output circuit

The voltage output from T1 is rectified by diode DB2. L3 functions to take a spike.

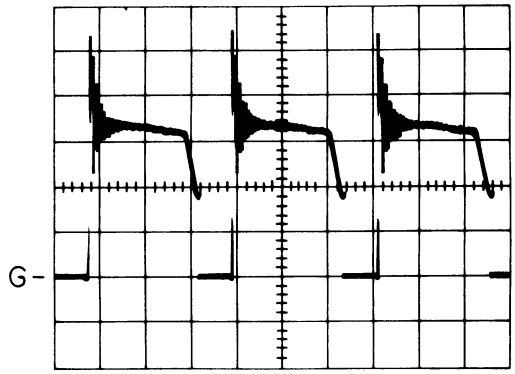
b. +12(C)/+12(F)/+12(L)/–12V output circuit

Each voltage output from T1 is rectified by the diode and regulated to desired voltage by the 3-pin regulator. The regulator has a protective function against excess current.



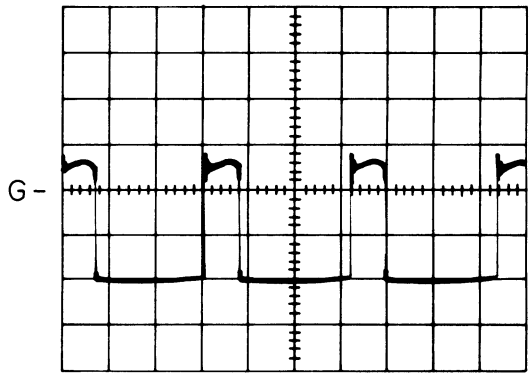
at either end of R2
0.5 V/DIV
2 ms/DIV

Fig. 3-13



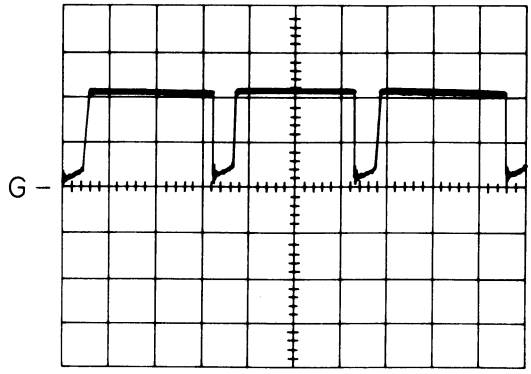
IC1 pin 15
(When being loaded)
100 V/DIV
10 μS/DIV

Fig. 3-14



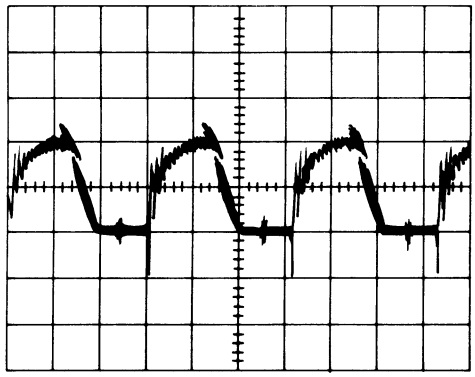
IC2 pin 4
5V/DIV
10 μs/DIV

Fig. 3-15



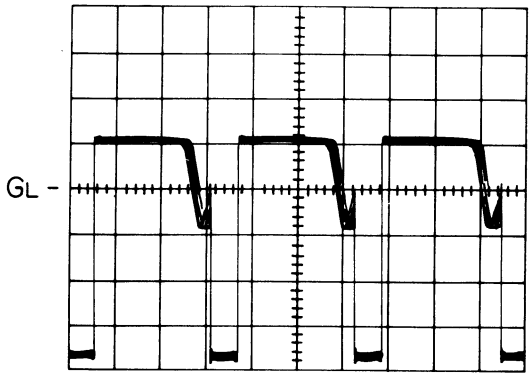
IC1 pin 7
5V/DIV
10 μS/DIV

Fig. 3-16



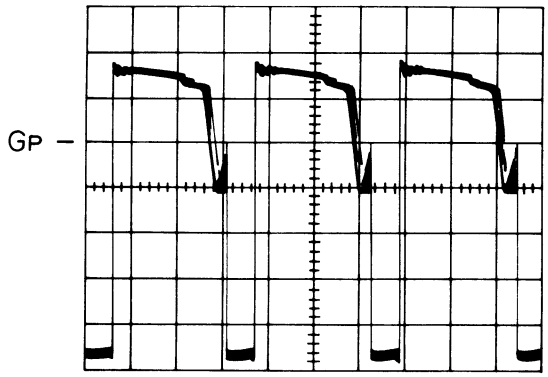
IC4 pin 5
AC 50 mV/DIV
10 μs/DIV

Fig. 3-17



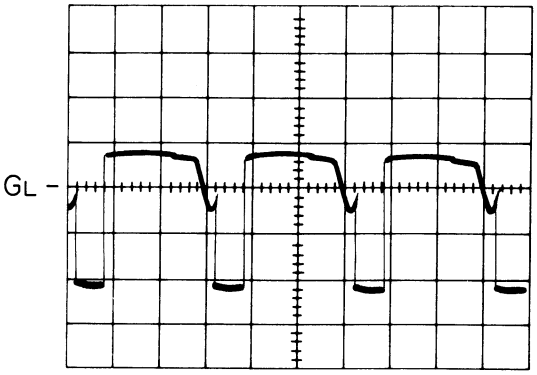
T1 (Transformer)
pin 2
5 V/DIV
10 μS/DIV

Fig. 3-18



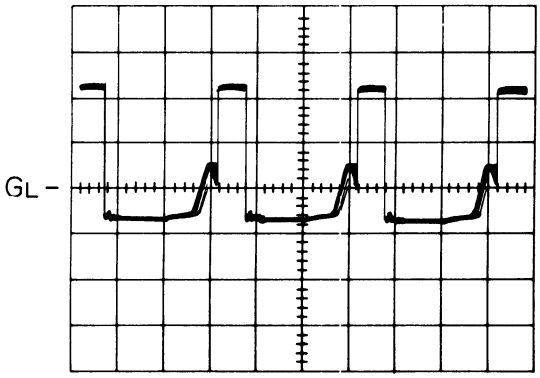
T1 (Transformer)
pin 4
10 V/DIV
10 μS/DIV

Fig. 3-19



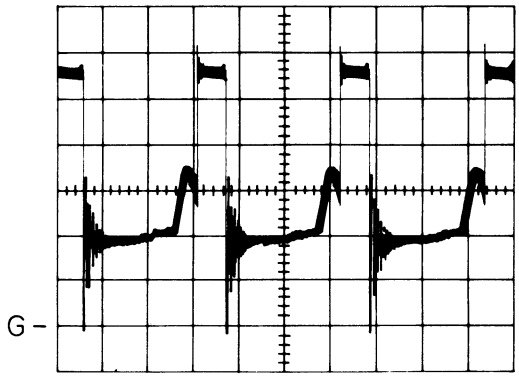
T1 (Transformer)
pin 6
20 V/DIV
10 μS/DIV

Fig. 3-20



T1 (Transformer)
pin 5
20 V/DIV
10 μS/DIV

Fig. 3-21



T1 (Transformer)
pin 9
100 V/DIV
10 μS/DIV

Fig. 3-22

CHAPTER 4
Q10SYM BOARD

CONTENTS

4.1 Reset Circuit

A reset signal is supplied to the main CPU μPD780 and peripheral ICs in the following four cases.

(1) Power on reset.
(2) Reset by RESET switch (Manual reset).
(3) Reset from external option I/O.
(4) Power down reset.

Receiving the reset signal, the CPU sets the program counter (PC) to 0 and holds the address bus and data bus at high impedance during reception of the reset signal.
Reset signal supply circuits are described below.

(1) Power on reset circuit
When the power is turned on, +5V is supplied to the emitter of transistor Q3. At the same time, this voltage is lowered by resistor R78 giving the potential difference between the emitter and base of transistor Q3 to turn it on.
This voltage is applied to the positive side of capacitor C3 to charge it, and then set the input of pin 9 of IC23E to high level.
The reset time by power on depends on the time constants of capacitor C3 and resistor R122, and in this system is 0.3 $\sim$ 0.5 seconds.
That is, since the input of pin 9 of IC23E is at low level after the power is turned on and at the beginning of capacitor charging, the gate input of IC21M is applied to pin 2 through the two-stage inverter IC23E.
Therefore, the output of pin 12 of IC21M or the reset signal to the CPU is set to low level, resetting the CPU and peripheral ICs.

(2) Reset by RESET switch (Manual reset)
When the RESET switch is turned on, the D-type FFs of IC24M are reset and the Q-output is set to Low level. By the next CK-input to IC24M, Q-output is set to high level. This signal is applied to the B-terminal of IC24K as its input. IC24K outputs a single shot signal according to the externally mounted CR. In this case, since the input to the A-terminal is GND, a signal of 5 $\sim$ 10μsec at low level is generated as a Q-output, which is applied to pin 13 as a gate input of IC21M, providing a signal to reset the CPU. This circuit is needed to hold contents of D-RAM.

(3) Reset by external I/O
A reset signal from the extended external I/O is accepted. The reset signal is applied to pin 1 of IC21M, providing a reset signal to the CPU or peripheral ICs.

(4) Power down reset
By the power down signal and the output from pin 10 of IC23E, a low level signal is output with a delay of about 10msec after detection of the PWD signal.
Power down reset is made by this signal.

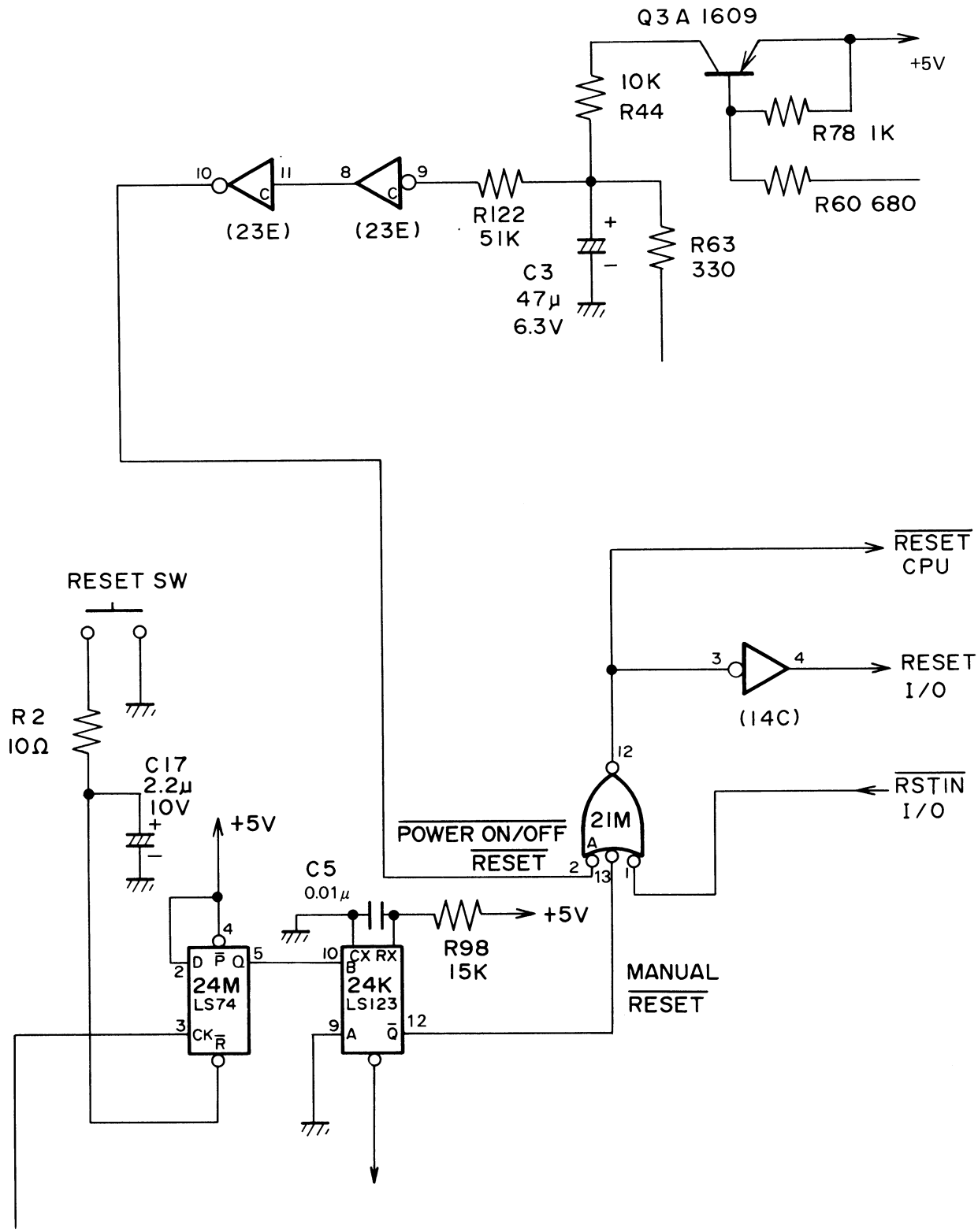


Fig. 4-1 Reset circuit

4.2 PWD Signal Supply Circuit

When the supply voltage drops to lower than about 80V AC in the 100V AC channel and 160V in the 200V channel, the PWD signal is detected by the signal of low to high level from the power supply circuit Q10PS board.

When the PWD signal is set to high level, the base voltage of the transistor Q3 rises to high level to cut it off. On the other hand, with the PWD signal, the inverter output at pin 6 of IC21C is set to low level, making an interrupt request to the interrupt input terminal IR0 of the interrupt controller μPD8259 (12E) through the inverter output at pin 10 of IC23C.

This interrupt made by power down is programmed in the interrupt controller as an interrupt with the highest priority, and supplies an interrupt signal for the CPU.

Receiving this interrupt signal, the CPU selects C-MOS RAM and activates the $\overline{CS1}$ terminal of C-MOS RAM μPD449.

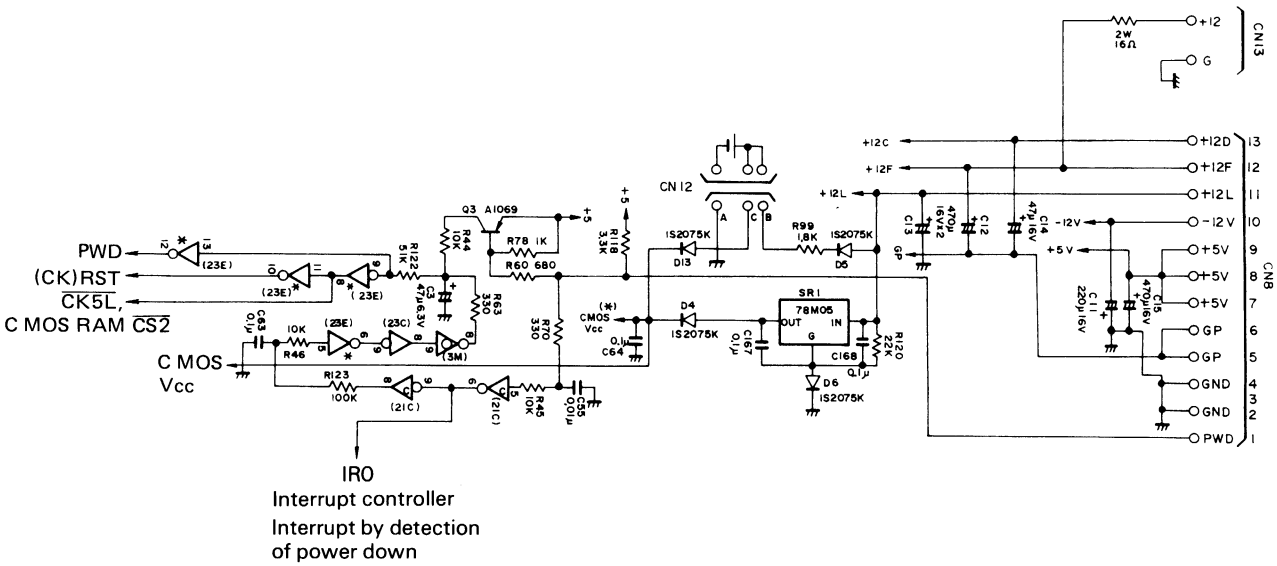


Fig. 4-2 PWD signal supply circuit

Further, the inverter output of IC21C supplies a low level signal to the output of pin 8 of IC3M after a delay of 10msec through the delay circuit comprising four inverters, R123 (100 kΩ) and C63 (0.1μF).

This delay circuit prevents the CPU from being reset due to momentary power down.

Receiving this low level signal, the output of pin 8 of the inverter IC23E is set to high level.

This output is connected to the $\overline{CS2}$ terminal of C-MOS RAM μPD449, and before it is set to high level by detection of the PWD signal, the signal of the $\overline{CS1}$ is set to low level. Thus, the C-MOS RAM is activated and the data of each register or stack pointer is written.

Thereafter, by detection of the PWD signal, the signal of $\overline{CS2}$ is set to high level by the battery backup of IC23E, and the C-MOS RAM is separated from the system to preserve the data.

Further, the PWD detection signal supplies a PWD signal to an external device from the inverter output of pin 12 of IC23E, and a $\overline{RESET}$ signal for the CPU and peripheral I/Os from the output of pin 10 of IC23E.

These signals are shown in Fig. 4-3.

The $\overline{CS2}$ signal is re-set to low level when the power is turned on. Thus, the contents of C-MOS RAM are read by setting the $\overline{CS1}$ signal to low level by selecting the C-MOS by the I/O select signal from the CPU.

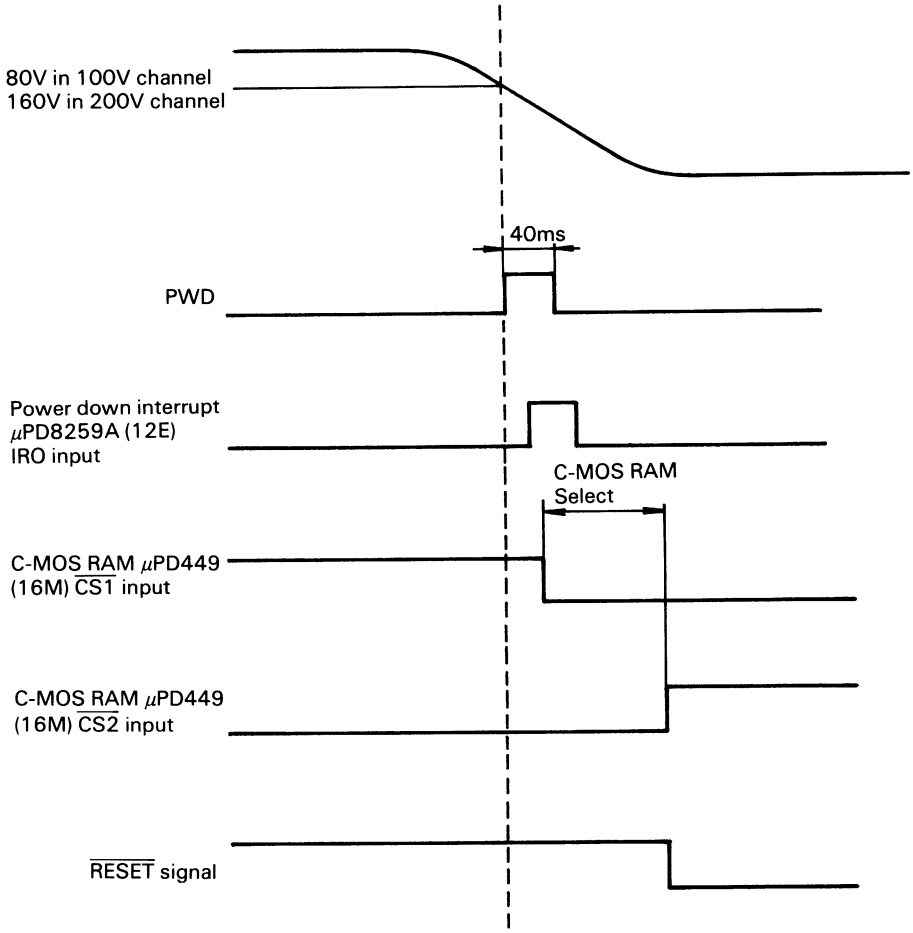


Fig. 4-3

4.3 C-MOS IC Power Supply Circuit

When the AC power is turned off, the C-MOS IC is backed up by the NiCd battery (3.6V, 90mAh). When the AC power is turned on, +5V is provided from the +12V supplied from the power supply Q10PS board through the series regulator 78M05 (SR1) and supplied to the C-MOS IC, because the C-MOS IC requires a very stable power supply.

At this time, the diode D4 functions to prevent reverse current from the NiCd battery at power down. Diode D6 is inserted between the regulator GND terminal and GND line to raise the regulator potential by about 0.6V for ensuring +5V in the output in order to compensate the voltage drop by diode D4.

The NiCd battery is charged by the +12V line through diode D5 (1S2075K) and resistor R99 (1.8kΩ).

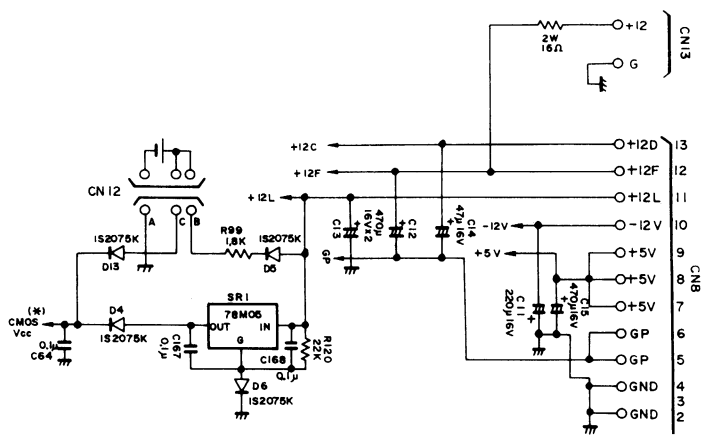


Fig. 4-4

4.4 System Clock Supply Circuit

The system clock supply circuit of Q10SYM board is shown in Fig. 4-5. The CPU μPD780 applies the original oscillation of 15.9744 MHz to the INPUT A terminal of the 4-bit binary counter LS93 and its output or Q_A output to the INPUT B terminal. Thereby it is operated by the 4-divided clock of 3.9936 MHz from the Q_B terminal.

This system clock is also supplied to the flip-flop which controls the pulse width and position.

The Q_C output which is 8-divided frequency of the original oscillation supplies a clock to the programmable interval timer 8253 (14E/16E).

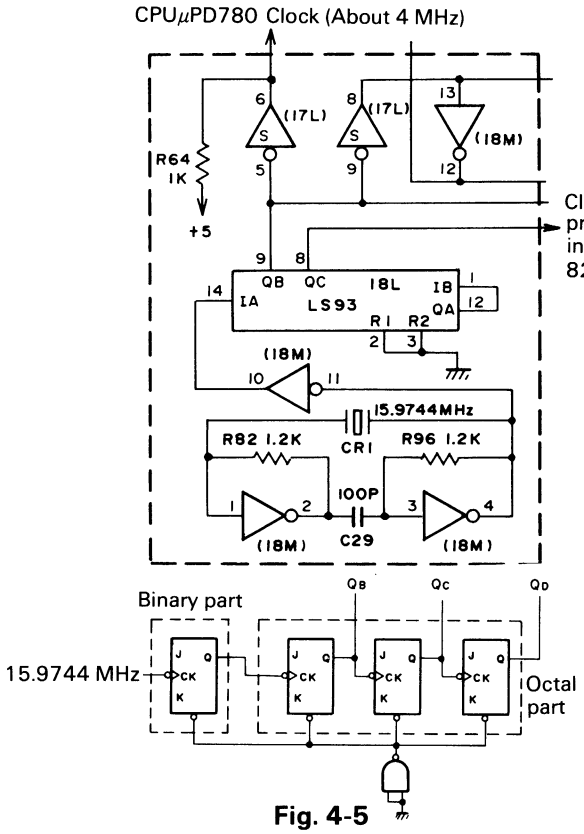


Fig. 4-5

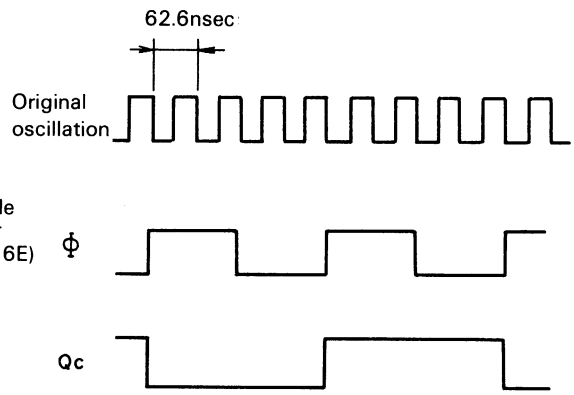


Fig. 4-6

4.5 I/O and Memory Read/Write Signal Supply Circuit

The CPU μPD780 has 64K bytes, 0000H ~ FFFFH as a memory address and 1K port, 00 ~ FFH as an I/O address.

Access to each address and port is available with the following four methods.

(1) Reading from I/O
(2) Writing into I/O
(3) Reading from memory
(4) Writing into memory

In the μPD780, the following four signal lines are combined by the gate of the circuit shown in Fig. 4-7, thereby supplying the signals of (1) ~ (4) above.

(a) $\overline{\text{IORQ}}$: Specifies I/O.
(b) $\overline{\text{MREQ}}$: Specifies memory.
(c) $\overline{\text{RD}}$: Read timing.
(d) $\overline{\text{WR}}$: Write timing.

Therefore, the above signal lines become as follows.

(1) $\overline{\text{IORQ}} \cdot \overline{\text{RD}} \rightarrow \overline{\text{IORD}}$
(2) $\overline{\text{IORQ}} \cdot \overline{\text{WR}} \rightarrow \overline{\text{IOWR}}$
(3) $\overline{\text{MREQ}} \cdot \overline{\text{RD}} \rightarrow \overline{\text{MERD}}$
(4) $\overline{\text{MERQ}} \cdot \overline{\text{WR}} \rightarrow \overline{\text{MEWR}}$

These signals are output through the 3-state line buffer S241 (23J). The S241 (23J) has the G-signal input terminal to determine the state of the output signal of the Y-terminal: the input signal of S241 (23J) is output when the G-signal level is high, and the output of S241 (23J) is in the high impedance state when the G-signal level is low.

The G-signal is supplied by the gate made by IC21E shown in Fig. 4-7.

To pin 9 of IC21E, the $\overline{\text{BUSAK}}$ signal from the CPU is connected via the inverter (IC22H). When the $\overline{\text{BUSAK}}$ signal is at high level, that is, the system address and data bus can be used by the CPU only, S241 (23J) is permitted to output a signal.

In other words, when the $\overline{\text{BUSAK}}$ signal is active during DMA transmission, output of signals (1) ~ (4) from the CPU is inhibited.

To pin 8, which is another input of gate IC21E, an interrupt acknowledge signal at active $\overline{\text{IORQ}}$ signal output in the M1 cycle is connected.

When the interrupt acknowledge signal applied to pin 8 of IC21E is active and at high level, the G-terminal of S241 (23J) becomes low level. Thus, the output of S241 is set to high impedance, inhibiting the CPU from outputting signals (1) ~ (4) to an external device.

To release this interrupt processing, an $\overline{\text{WR}}$ signal is supplied from the CPU. When the $\overline{\text{WR}}$ signal is made active, the input to pin 8 of IC21E is set to low level and a high level signal is supplied to the 2G terminal of S241 (23J). The timing chart is shown in Fig. 4-8.

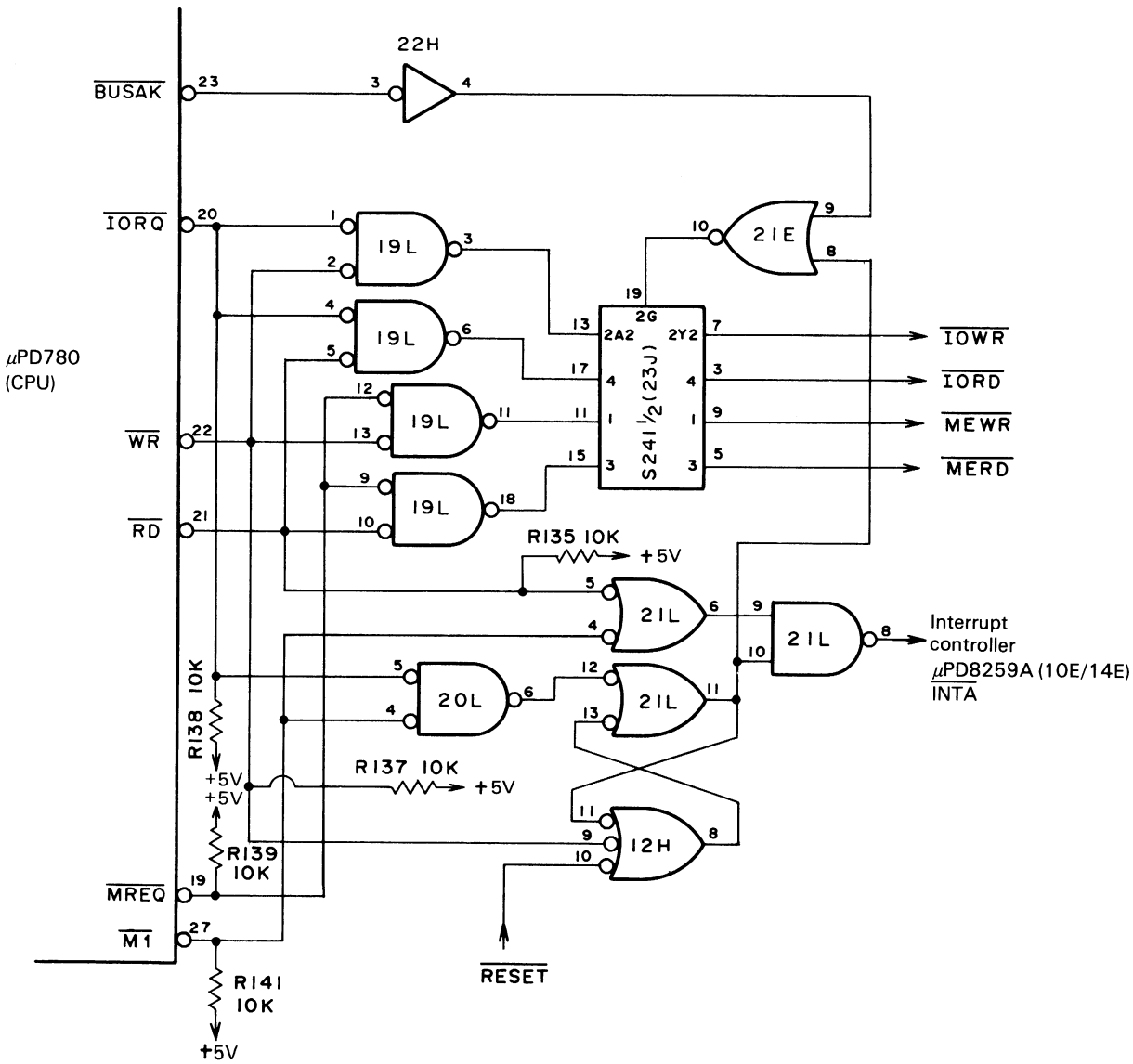


Fig. 4-7 Circuit to supply read/write signal to I/O and memory

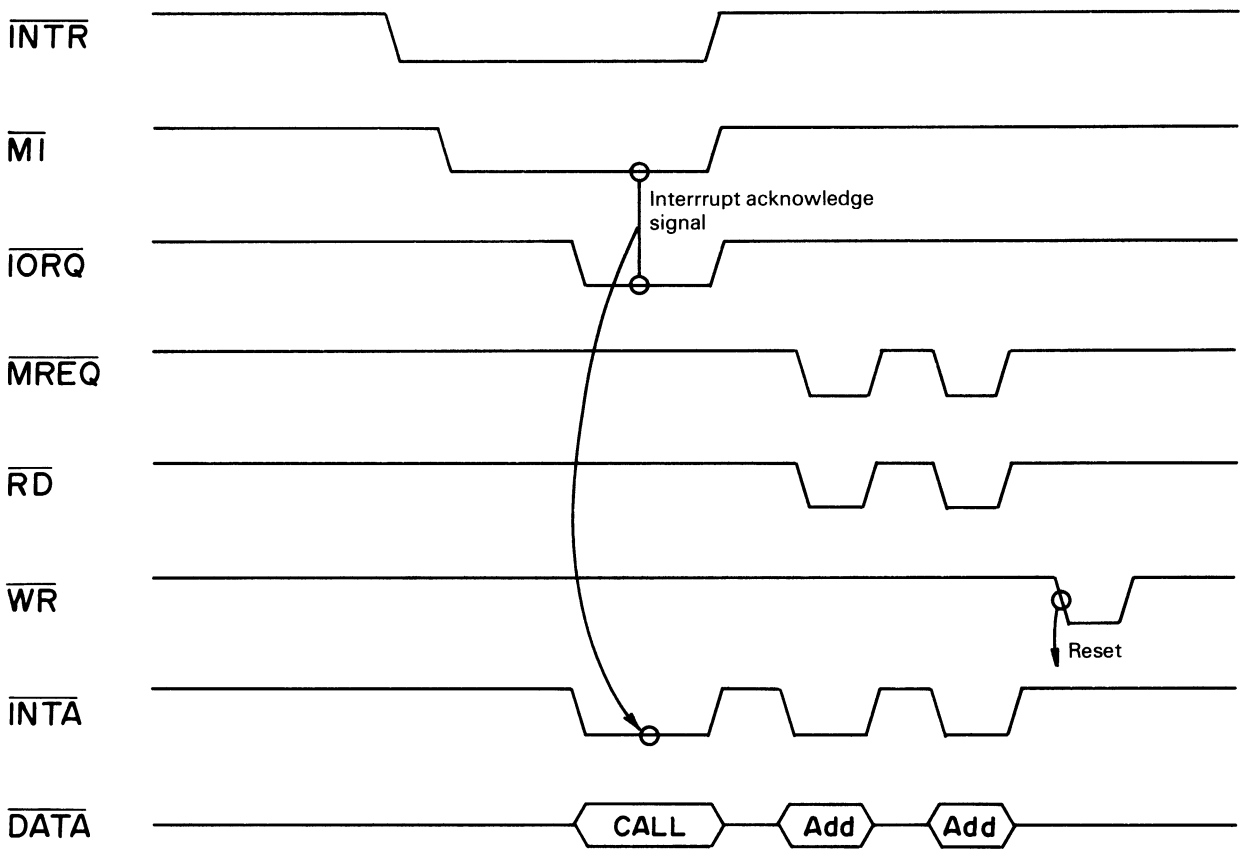


Fig. 4-8 Interrupt acknowledge signal timing

► IOWR Signal Supply Circuit

As described in the preceding paragraph, the write (WR) signal to the I/O device can be supplied by taking AND of IORQ signal of the CPU and WR signal.

The timing of the output data D0 ~ 7 from CPU and IOWR signal is shown in Fig. 4-10.

The output data is sampled at the leading edge of the IOWR signal.

However, when an I/O device is provided by an external option, the sampling timing for data writing needs to be set to the ensured time of data output in order to guarantee the writing data.

The circuit shown in Fig. 4-9 is used for this purpose, which reduces the IOWR signal by one clocks and makes its leading edge earlier and performs data writing.

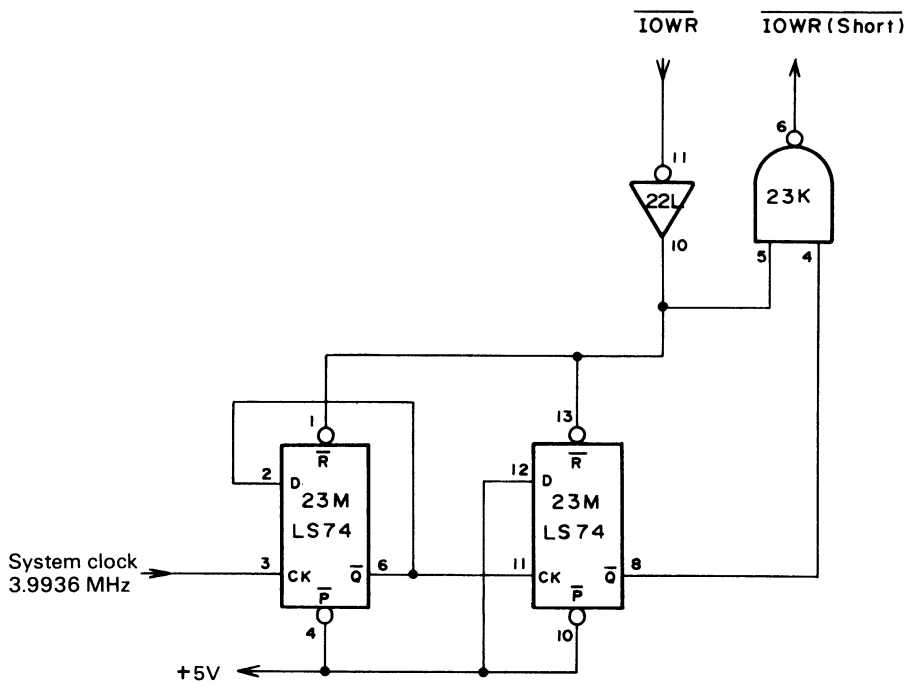


Fig. 4-9

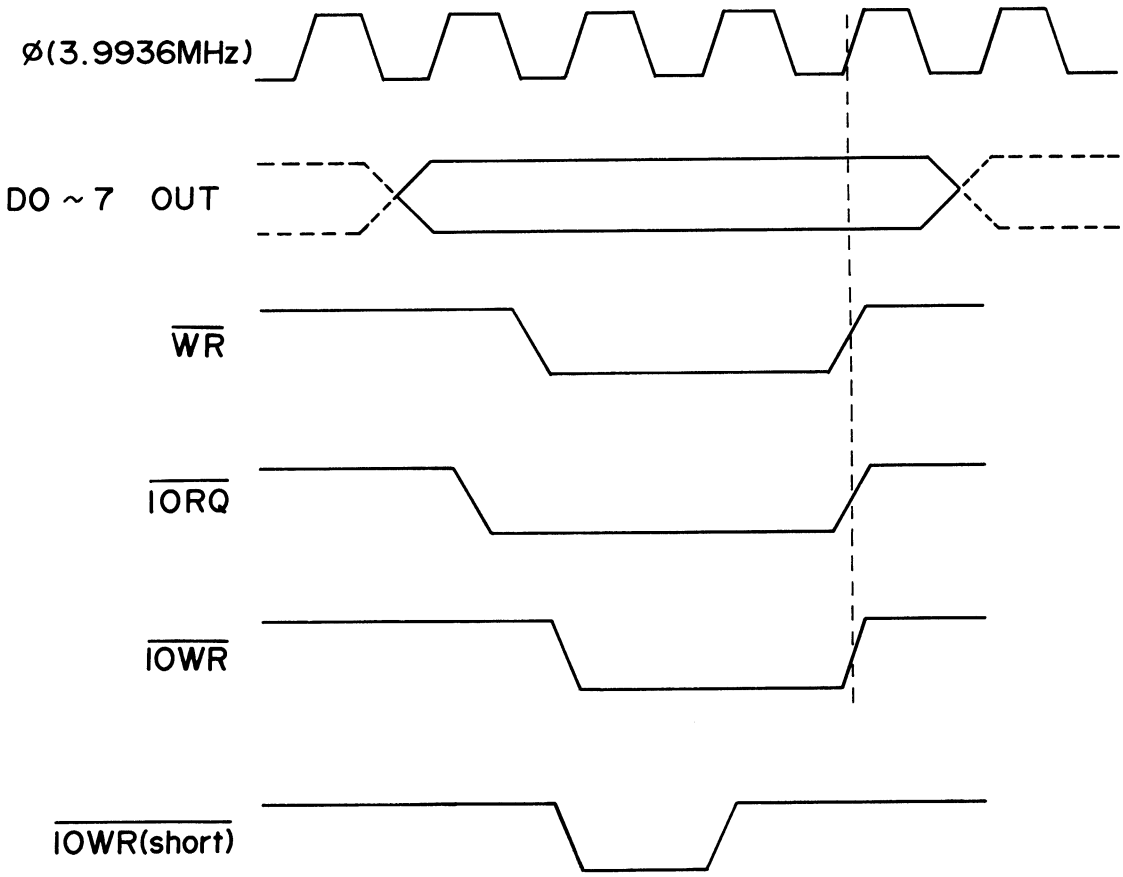


Fig. 4-10

4.6 Data Bus line Signal Direction Selector (LS245 (14K))

D-RAM, I/O device and external memory are connected through the data bus line for the CPU as shown in Fig. 4-11.

In normal operation, data is transferred from the CPU to the I/O device or external memory. However, in the DMA transfer mode, the data transfer direction needs to be changed to the CPU in the following cases (1) ~ (6).

(1) CPU ← I/O (Read)
(2) CPU ← External memory (Read)
(3) D-RAM ← I/O device (Read)
(4) I/O device (Write) ← External memory (Read) } DMA
(5) External memory ← I/O device (Read)
(6) CPU (Int) ← 8259 (Read)

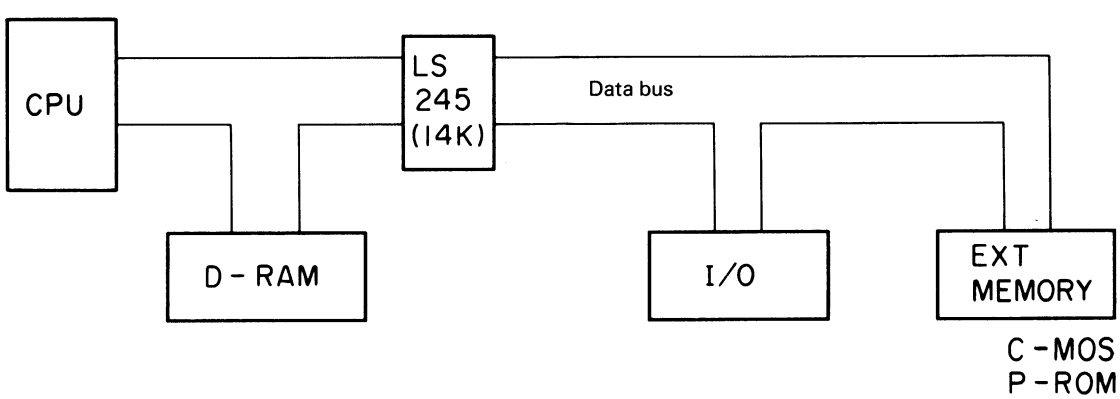


Fig. 4-11 Data bus line and peripheral devices

So, in this circuit, a 3-state bus transceiver (LS245) is inserted to change the data bus line signal direction according to the status of data transfer.

LS245 has DIR signal terminal to change the bus line direction. Data is transferred from the CPU to the I/O device or external memory when the DIR signal is low, and vice versa when the signal is high.

As shown in Fig. 4-12, in any one of the above states (1) to (6), AND is taken by IC20F in this circuit and a high level signal is sent to the DIR terminal of LS245.

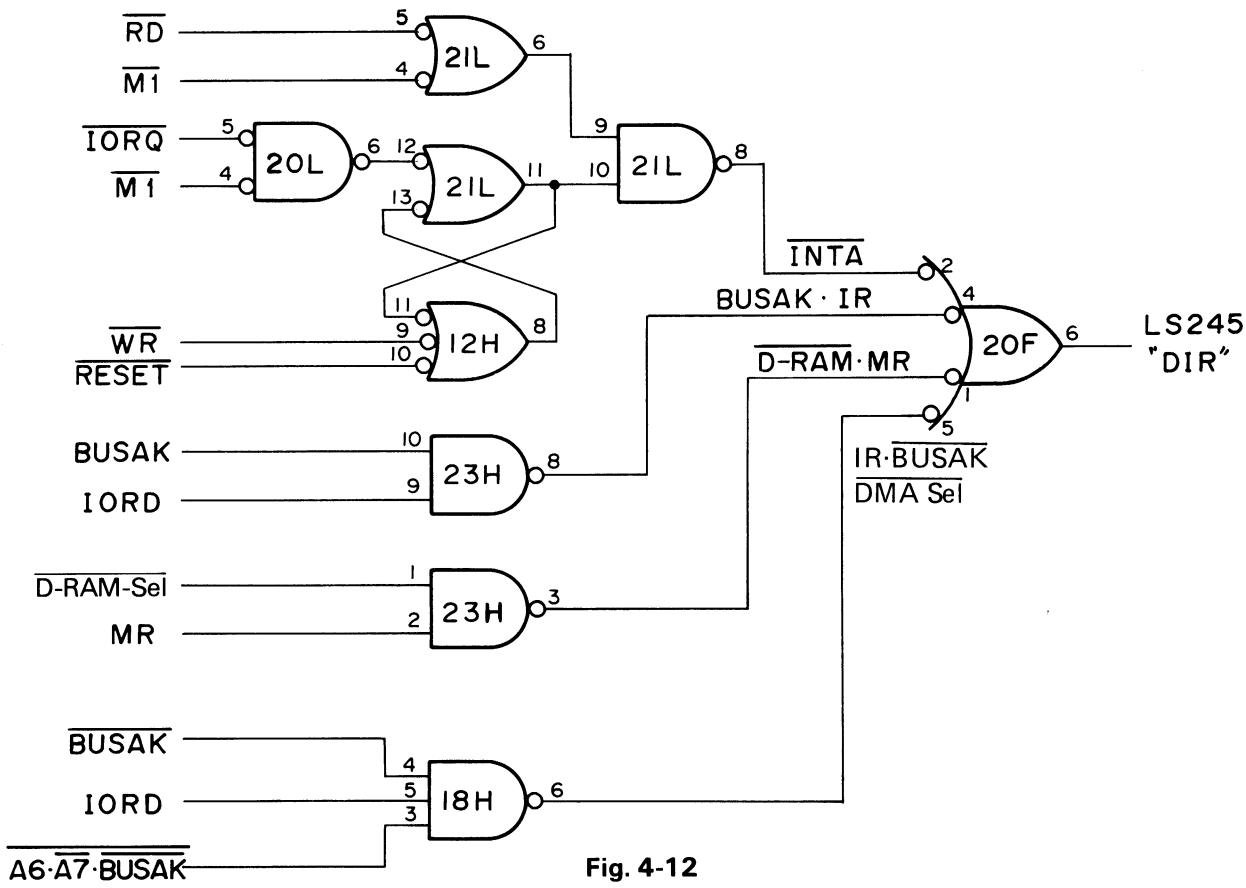


Fig. 4-12

(a) Input signal of pin 2 of IC20F

The same signal as the $\overline{\text{INTA}}$ signal of the interrupt controller 8259A is entered. This is an interrupt acknowledge signal of CPU against the interrupt request from the peripheral device, and made from the $\overline{\text{IORQ}}$ signal and $\overline{\text{RD}}$ signal output from the CPU accompanied by the M1 (machine cycle 1) signal. This signal is reset by the $\overline{\text{WR}}$ signal or $\overline{\text{RESET}}$ signal. Therefore, it gives a direction signal in case of (6).

(b) Input signal of pin 4 of IC20F

AND of $\overline{\text{BUSAK}}$ and $\overline{\text{IORD}}$ signals from the CPU is entered.

The $\overline{\text{BUSAK}}$ signal indicates that the CPU data bus, address bus and 3-state output control signal line are in the high impedance state and these buses can be used by the other device (I/O device).

The $\overline{\text{IORD}}$ signal indicates the read signal from the I/O device. Therefore, taking AND of these signals meets the data bus condition for D-RAM from the I/O device at DMA transfer or READ for an external memory.

Namely, this signal gives a direction signal in cases (3) and (5).

(c) Input signal of pin 1 of IC20F

This signal is composed of AND of the $\overline{\text{MR}}$ signal of the interrupt controller 8237 and the signal indicating selection of memory.

Therefore, pin 1 of IC20F is made active when the external memories including P-ROM and RAM of C-MOS are selected and the CPU and I/O devices read these memories.

This signal meets cases (2) and (4).

(d) Input signal of pin 5 of IC20F

$\overline{IORD}$, $\overline{BUSAK}$ and $\overline{DMASel}$ signals are applied to pin 5.

When the DMA is not selected and the CPU is read by the I/O device, this input signal is made active.

Therefore, this signal meets case (1).

4.7 External Option Bus Line Signal Direction Selector

The data bus direction in data transfer between the CPU or memory and external option is selected by the 3-state bus transceiver LS245 (8H). The DIR signal of LS245 (8H) releases the data bus from the external option toward CPU/memory when the signal level is high, and vice versa when it is low.

DIR signal	Data bus transfer direction
H	CPU/Memory → External option
L	External option → CPU/Memory

To meet these conditions, the DIR signal is supplied by the circuit shown in Fig. 4-13 at the hardware level.

Data transfer from the external option to CPU/memory is made in the following three cases.

(1) The memory is read by an external option memory.

(2) DMA transfer from an external option. (6 channels)

(3) Reading form external I/O.

The DIR signal provides the signal to meet these conditions through the gate composed of IC7K and IC9K.

Therefore, it is an output signal except when data is entered from an option card.

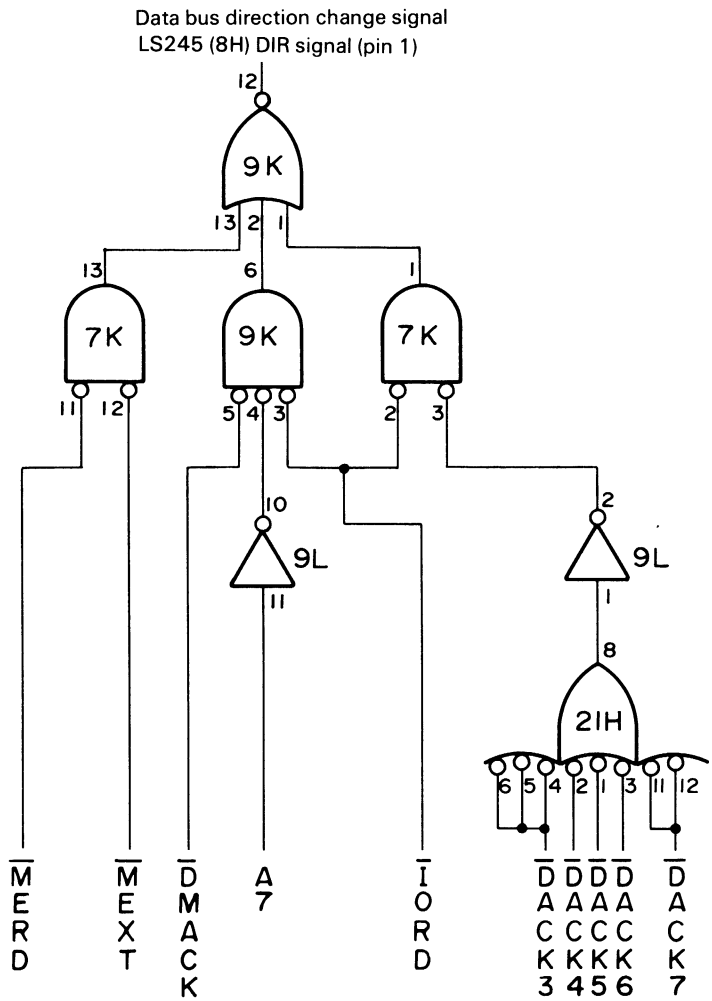


Fig. 4-13 Option card – data bus direction change signal supply circuit

4.8 $\overline{\text{WAIT}}$ Signal Supply Circuit

CPU μPD780 fetches the OP code when the $\overline{\text{M1}}$ signal is active. Usually, the machine cycle $\overline{\text{M1}}$ comprises 3 or 4 cycles T1 to T3 or T1 to T4 as shown in the timing chart (Fig. 4-14). During this cycle, an instruction is read and executed.

The CPU outputs the address value (program counter data) containing the instruction to be next executed in the T1 cycle to the address bus and reads the instruction from the data bus (D0 ~ D7) at the end of T2 cycle.

Namely, an external program memory must read the data within this time difference and give it to the CPU.

In this system, to ensure time for reading the data from D-RAM (access time 150ns) and C-MOS RAM (access time 450ns), the circuit shown in Fig. 4-16 is provided to generate the $\overline{\text{WAIT}}$ signal which is active low in the T2 cycle when the $\overline{\text{M1}}$ signal is active.

Thus, as shown in the timing chart (Fig. 4-15), the CPU takes in the $\overline{\text{WAIT}}$ signal in the leading signal in the T2 cycle, provides one extra T2 cycle in the next cycle and prolongs the time to ensure reading the data from the memory. This cycle is called a TW cycle. The $\overline{\text{WAIT}}$ signal is supplied through jumper J6, and J6 is usually set in the jumper state.

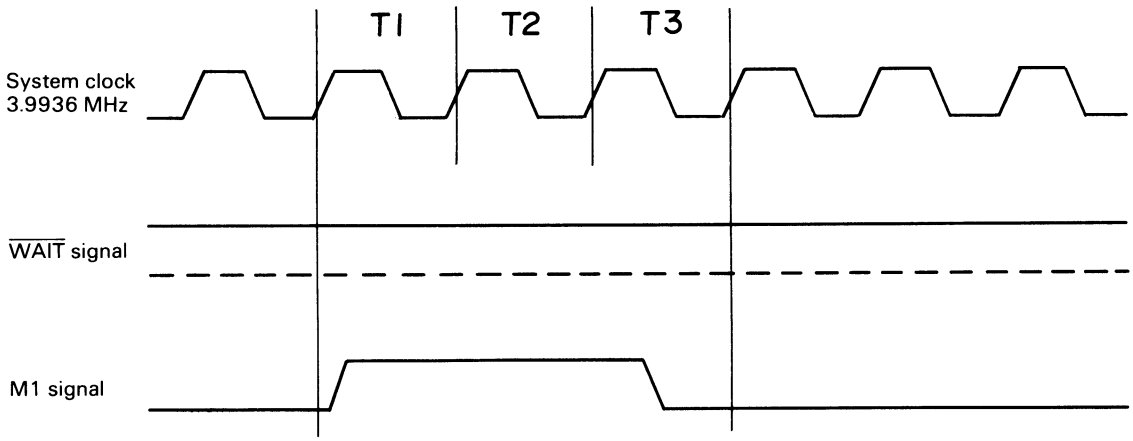


Fig. 4-14 M1 timing without Tw cycle (At 3 cycles)

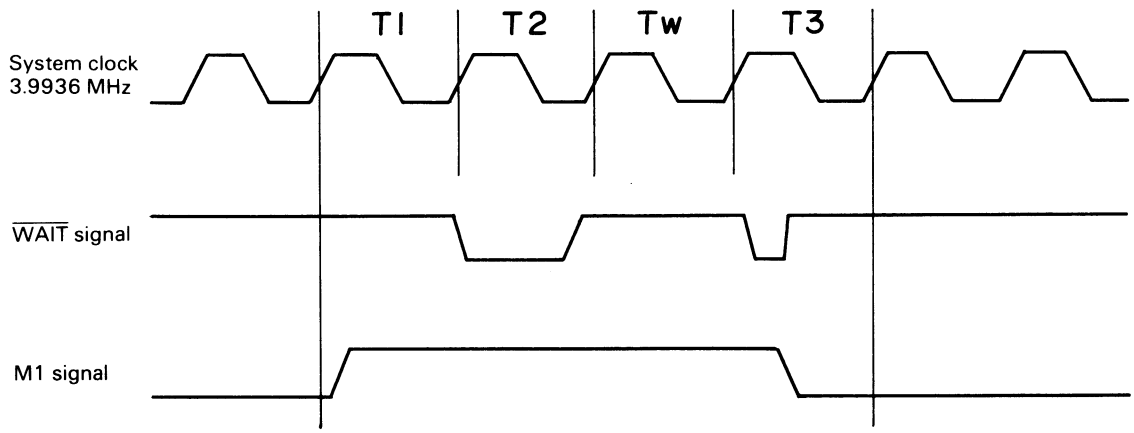


Fig. 4-15 M1 cycle with Tw cycle (At 4 cycles)

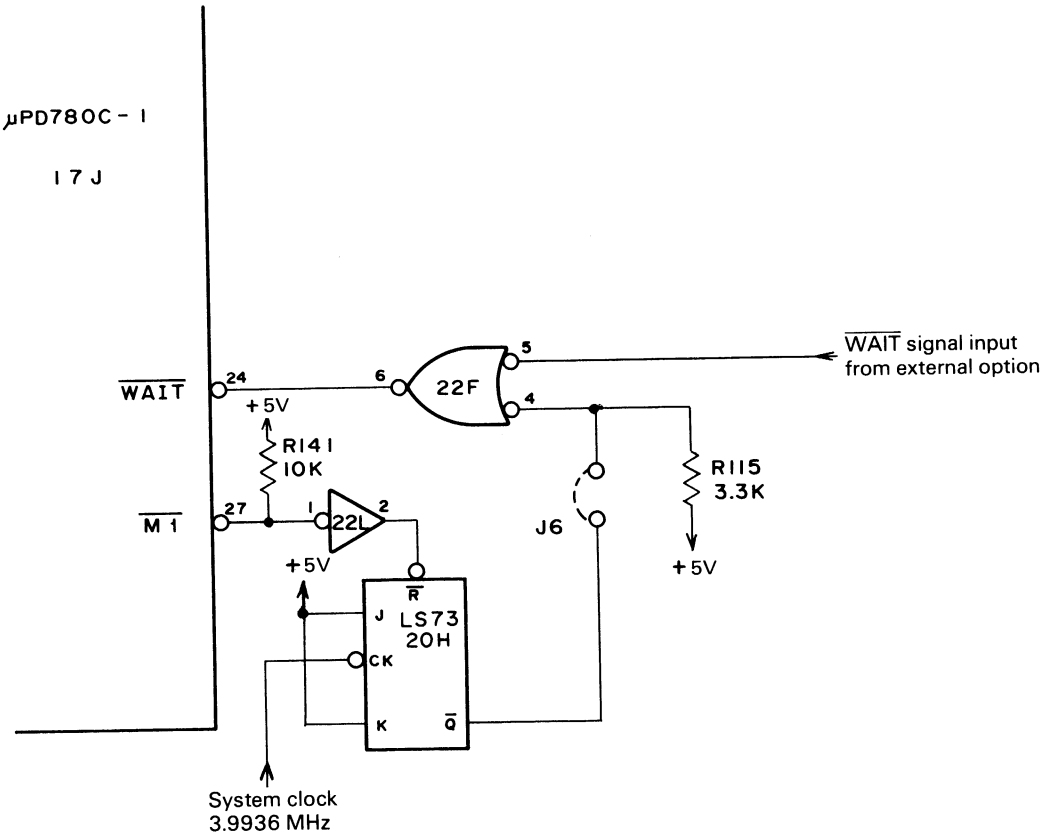
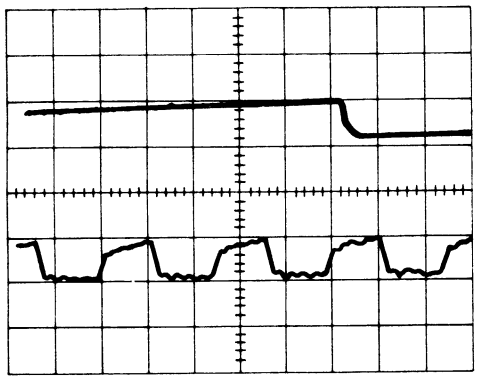
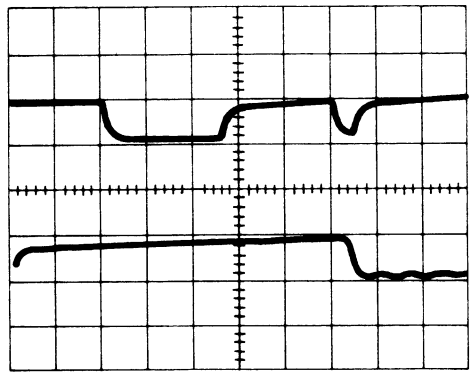


Fig. 4-16 $\overline{\text{WAIT}}$ signal supply circuit



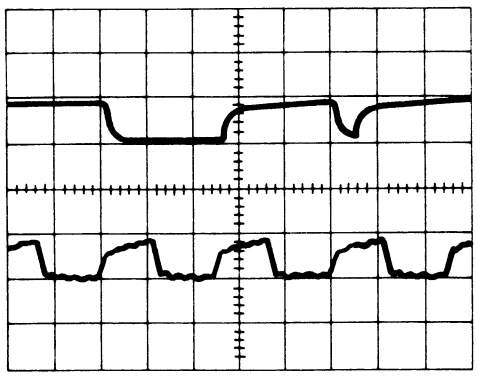
Upper: $\overline{\text{M1}}$ signal
Lower: CLK
(Sweep 0.1 μsec. 5 volts/div.)

Fig. 4-17



Upper: $\overline{\text{WAIT}}$ signal (with J6)
Lower: $\overline{\text{M1}}$ signal
(Sweep 0.1 μsec. 5 volts/div.)

Fig. 4-19



Upper: $\overline{\text{WAIT}}$ signal
Lower: CLK
(Sweep 0.1 μsec. 5 volts/div.)

Fig. 4-18

4.9 I/O Selector

Each I/O port is accessed by decoding the low-order 4 bit addresses (A2 ~ A5) of the CPU by the I/O selector LS154 (16H).

The functions of this I/O selector are shown in Table 4-1. One output terminal must be set to low level for the inputs at terminals A ~ D. The output signal provides the $\overline{CS}$ signal for each I/O device or CLK signal, and thereby a desired I/O device is selected.

In this case, to the terminals $\overline{1G}$ and $\overline{2G}$ which control the gate of LS154 (16H), the signal of the address line A6 is applied to the $\overline{1G}$ terminal, and the AND of the signal of the address line A7 and the $\overline{BUSAK}$ signal from CPU is applied to the $\overline{2G}$ terminal. The $\overline{BUSAK}$ signal indicates that the bus line can be used by the other devices when the signal level is low. The $\overline{2G}$ terminal is made active when the $\overline{BUSAK}$ signal and the address line A8 are at high level.

Therefore, selection of I/O device is made when the $\overline{BUSAK}$ signal is at high level and the address line and bus line are inhibited from being used by the other devices except for the CPU.

The I/O port address map is shown in Table 4-2.

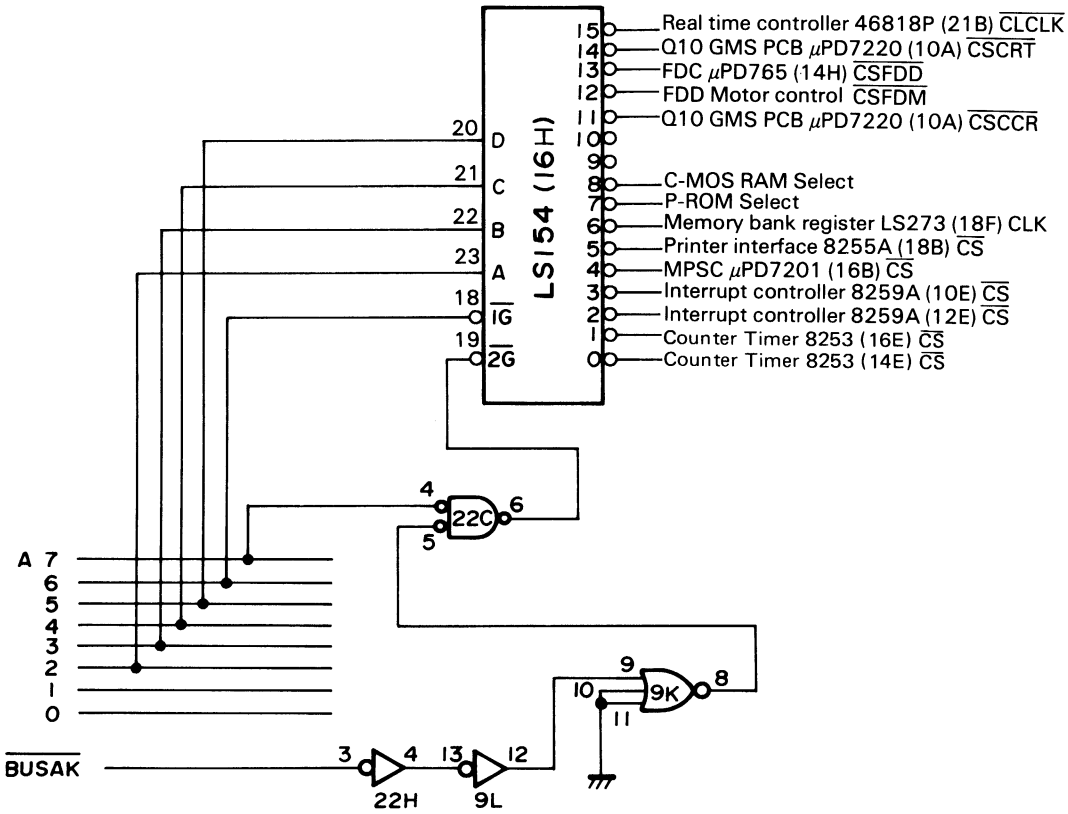


Fig. 4-20 I/O selector

FUNCTION TABLE

INPUTS						OUTPUTS															
$\overline{1G}$	$\overline{2G}$	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

Table 4-1

I/O PORT ADDRESS MAP (Table 4.2)

	0	1	2	3
0 0	Speaker timer	SOFT timer No.2	SOFT timer No.1	8253 No. 1 command
0 4	Speaker Freq.	Keyboard clock	RS232C clock	8253 No. 2 command
0 8	8259 (Master)			
0 C	8259 (Slave)			
1 0	Keyboard data	RS232C data	Keyboard command	RS232C command
1 4	Printer data	Printer status	Printer control	8255 command
1 8	DIP./SW./Mem. bank reg.			
1 C	P·ROM select			
2 0	C·MOS select			
2 4				
2 8				
2 C	CRT, PCB TYPE			
3 0	FDD motor control			
3 4	FDC status	FDC data		
3 8	GDC 7220	GDC	Zoom	Light pen
3 C	Clock data	Clock adress		

	0	1	2	3
4 0	8237 DMA controller # 1			
4 4				
4 8				
4 C				
5 0	8237 DMA controller # 2			
5 4				
5 8				
5 C				
6 0				
6 4				
6 8				
6 C				
7 0				
7 4				
7 8				
7 C				

	0	1	2	3
8 0				
8 4				
8 8	GPIB Interface Q10IE			
8 C				
9 0				
9 4	Memory Box (Optical Fiber) Interface Q10OF			
9 8				
9 C	Pulse Transformer Interface Q10PT			
A 0	AD/DA Interface Q10AD			
A 4	RS-232C Interface Q10RS			
A 8				
A C				
B 0	Direct Modem Interface Q10DM			
B 4				
B 8				
B C				

	0	1	2	3
C 0	Bar-code Reader Interface			
C 4				
C 8				
C C				
D 0				
D 4				
D 8				
D C				
E 0				
E 4				
E 8				
E C				
F 0				
F 4				
F 8				
F C				

Table 4.2

4.10 I/O Commands

The commands and status of each I/O device are described below. An important I/O device is initialized within IPL, and need not be re-set. The appropriate command is marked by "Set in IPL".

LSI 8253 **Function: Timer counter** #1, #2

I/O address 00H ~ 03H #1
04H ~ 07H #2

	7	6	5	4	3	2	1	0
03H (07) W	00: Counter 0 01: Counter 1 10: Counter 2		00: Counter latch 01: LSB Read/write 10: MSB Read/write 11: 2 byte Read/write		000: Terminal count 001: One shot 010: Repeated waveform	011: Squre wave output 100: Software trigger 101:Hardware trigger		0: Binary 1: BCD

Command register

00H ~ 02H (04 ~ 06) R/W	Counter value (Low-order and high-order digits are continuously read and written in this order.)

Timer counterof each channel

03H W	0	0	1	1	0	0	1	0
	Counter 0		2-byte mode		One shot mode			Binary
00H W	0	1	1	1	0	0	0	0
00H W	0	0	0	0	0	0	0	0

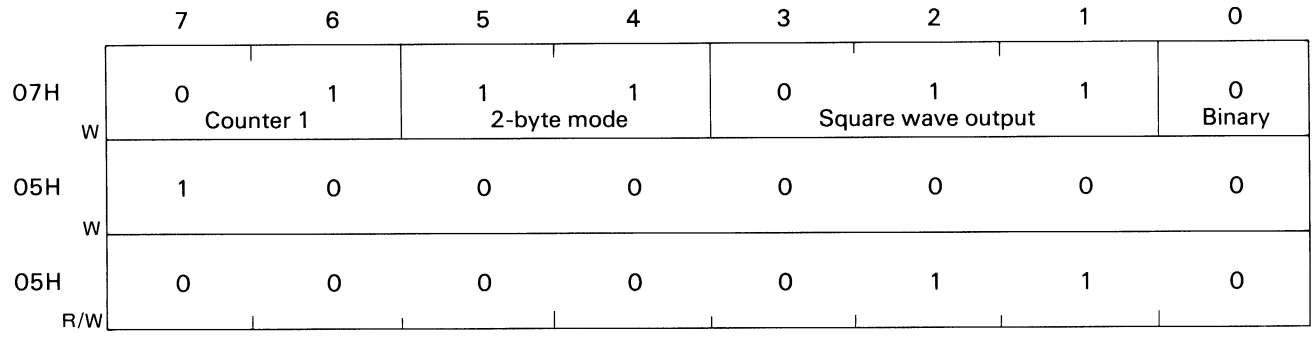
Initial setting related to speaker timer (Set in IPL)

Set to about 100 ms (1200 Hz ÷ 112)

07H W	0	0	1	1	0	1	1	0
	Counter 0		2-byte mode		Square wave output			Binary
04H W	0	0	0	0	0	0	0	0
04H W	0	0	0	0	1	0	0	0

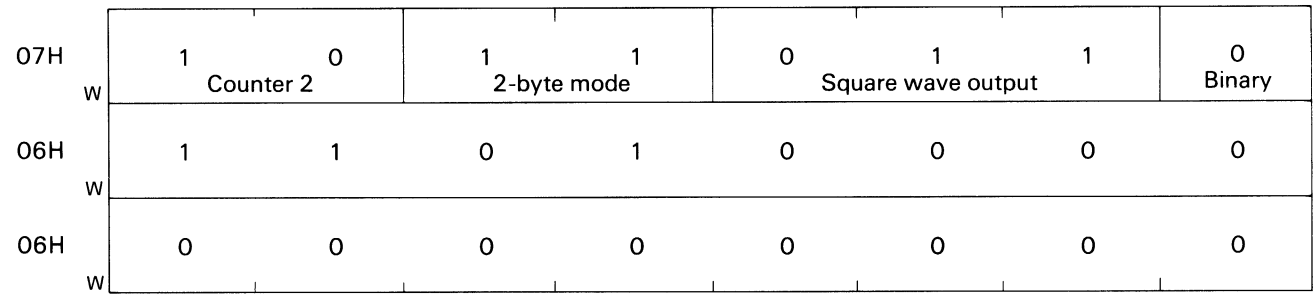
Initial setting of speaker frequency (Set in IPL)

Set to about 1kHz (2 MHz ÷ 2048)



Initial setting related to keyboard clock (Set in IPL)

Set 1200 BPS. (1.9968 MHz ÷ 1664)



Initial setting RS-232C clock (Set in IPL)

Set 9600 BPS. (1.9968 MHz ÷ 208)

I/O address 08H ~ 09H

	7	6	5	4	3	2	1	0
08H W	A7 ~ 5 (Interrupt address)			1	0: Edge sense 1: Level sense	0: 8-byte 1: 4-byte	0: Multi 8259 1: Single 8259	0: Without ICW4 1: With ICW4
	1	0	0		0	1	0	0

Setting of ICW1 (Set in IPL)

	7	6	5	4	3	2	1	0
09H W	0	0	0	0 A15 ~ 8 (Interrupt address)	0	1	1	1

Setting of ICW2. Start interrupt address is 780H in IPL. (Set in IPL)

	7	6	5	4	3	2	1	0
09H W	1	0	0	0 A15 ~ 8 (Interrupt address)	0	0	0	0

Setting of ICW3. Indicates slave 8259 is connected to the master IR7. (Set in IPL)

	7	6	5	4	3	2	1	0
09H W	0	0	0	0	0	0	1 Automatic end of interrup)	0

Setting of ICW4. (Set in IPL)

	7	6	5	4	3	2	1	0
09H R/W	Interrupt mask bit				{ 0: Interrupt enable 1: Mask }			

OCW1

	7	6	5	4	3	2	1	0
08H W	1: Priority rotate 0: Non	1: Specific 0: Non	1: EOI 0: Non	0	0	Interrupt level No. IR0 ~ IR7		

OCW2 End. of intr. command and priority rotate command

(Attention)

- ICW1 ~ 4 must be set continuously.
- Even when the interrupt address is changed, ICW1 ~ 4 must be set in sequence.
- OCW1 is usually readable and writable.

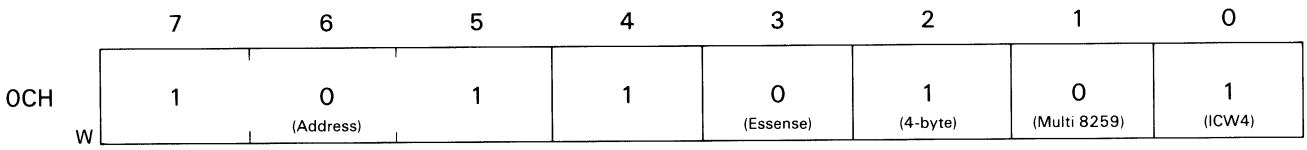
	7	6	5	4	3	2	1	0
08H W	0	1: Bit 5 valid 0: Bit 5 invalid	1: Set special mask 0: Reset	0	1	1: Pole mode 0: Non	1: Bit 0 valid 0: Bit 0 invalid	1: ISR read 0: IRR read

OCW3 When bit 1 = 1, 08H must be read next.

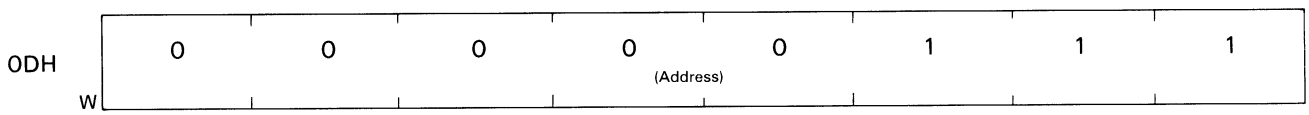
08H R	ISR: In Service Register or IRR: Interrupt Reqest Register

LSI 8259A **Function: Interrupt controller (master)**

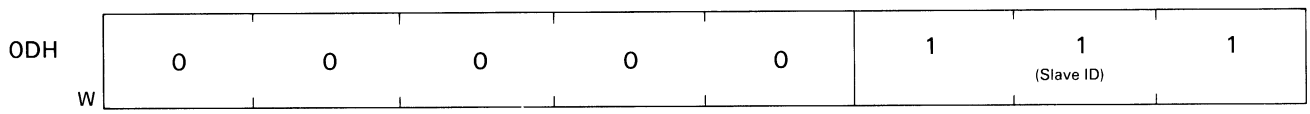
I/O adress 0CH ~ 0DH



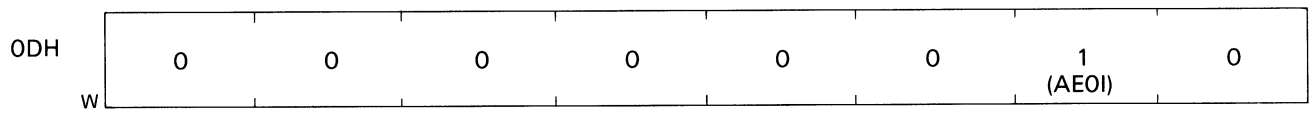
ICW1 (See 8259 master) (Set in IPL)



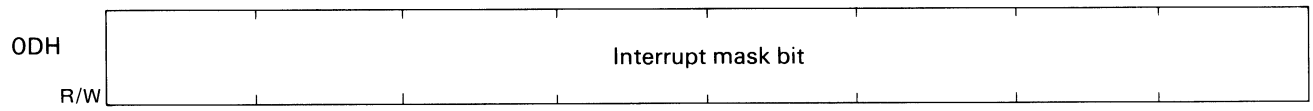
Setting of ICW2. Start interrupt address is 780H in IPL. (Set in IPL)



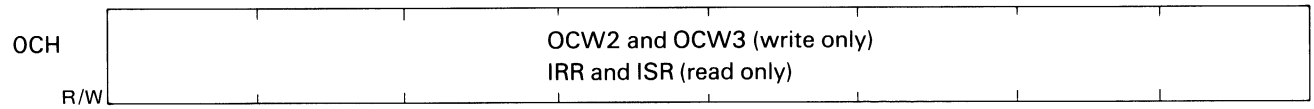
Setting of ICW3. Interrupt level of slave in master (Set in IPL)



ICW4 (See 8259 master) (Set in IPL)



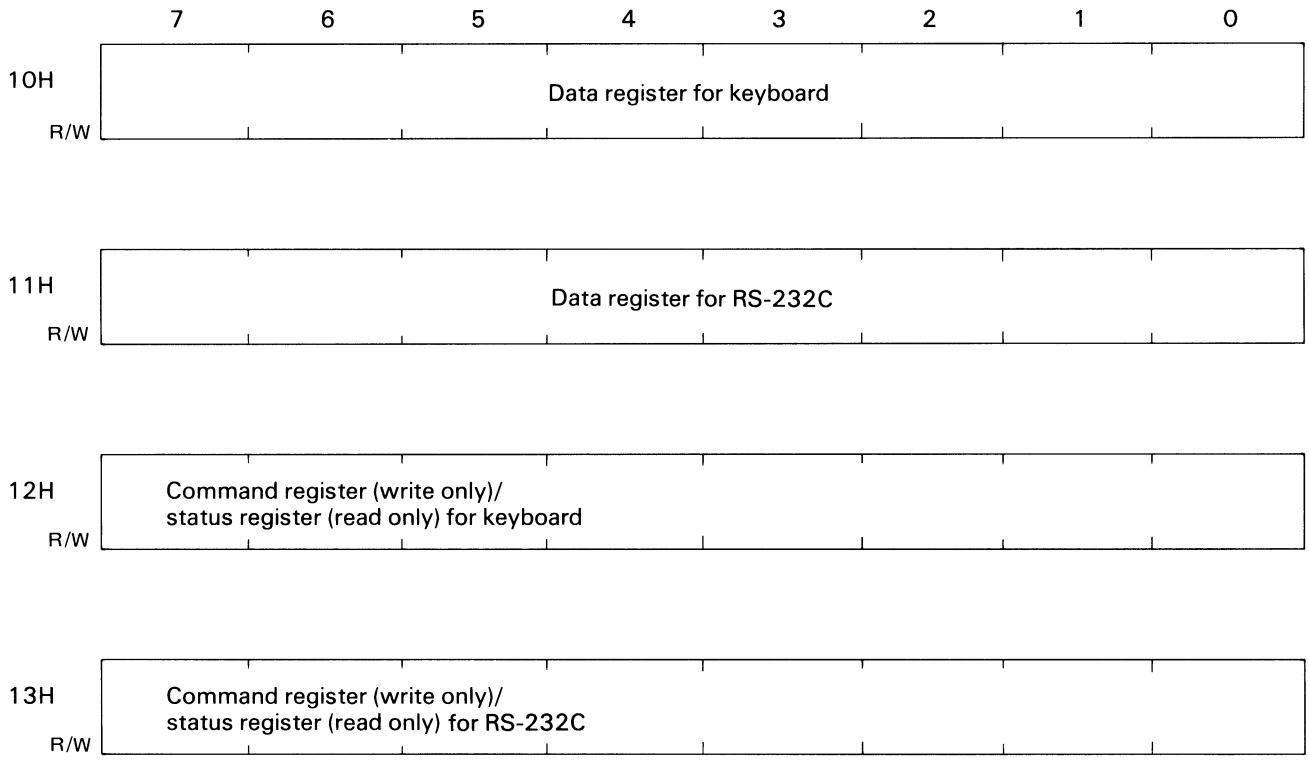
OCW1



(See 8259 master)

LSI 7201 **Function: Serial interface**

I/O address 10H ~ 13H



Continued

I/O adress H ~ H

		7	6	5	4	3	2	1	0
WR0 12H (13)	W	00: NO-op 01: Reset Rx CRC 10: Reset Tx CRC 11:Reset Tx underline		000: No-op 001: Send abort 010: Reset EX/INT 011: Channel reset	100: Next Rx. interrupt enable 101: TxINT hold reset 110: Error reset 111: Return from INT		Resister pointer 0 ~ 7		
WR1 12H (13)	W	Wait enable	0	Wait on Rx/Tx	00: Rx INT/DMA disable 01: First chr. Int enable 10: All chr. Int enable 11: All chr. Int enable		Status affect Vector	Tx INT/DMA enable	Ex/ST INT enable
WR2 12H	W	1: $\overline{SYNCB}$ 1: $\overline{RTSB}$	0	Vector mode	0: 85 mode 1: 86 mode Intr.	0: 85 IM1 1: 85IM2 Intr.	Priority Select	Intr./DMA mode	
WR3 12H (13)	W	Rx bits/chr. 00: 5 bit/chr. 01: 6 bit/chr. 10: 7 bit/chr. 11: 8 bit/chr.			Enter Hunt Mode	Rx CRC Enable	Address Search Mode	Sync chr. latch Inhibit	Rx enable
WR4 12H (13)	W	Clock Rate 00: X1 01: X16 10: X32 11: X64		Sync Mode 00: 8 bit 01: 16 bit 10: SDLC 11: External		00: Sync 01: 1 bit STOP bit 10: 1-1/2 bit STOP bit 11: 2 bit STOP bit		Parity 0: ODD 1: EVEN	Parity 0: Disable 1: Enable
WR5 12H (13)	W	0: $\overline{DTR}$ = 1 1: $\overline{DTR}$ = 0	Tx Bits/chr. 00: 5 bit/chr. 01: 6 bit/chr. 10: 7 bit/chr. 11: 8 bit/chr.		Send Break	Tx enable	CRC-16/ CCITT	0: $\overline{RTS}$ = 1 1: $\overline{RTS}$ = 0	Tx CRC enable
WR6 12H (13)	W	SYNC chr. Bit 7 ~ 0							
WR7 12H (13)	W	SYNC chr. Bit 15 ~ 8							
RR0 12H (13)	R	Break/Abort	Tx underrun/EOM	CTS	$\overline{SYNC}$/Hunt	DCD	Tx Buff Empty	Int. Pending (ch. A only)	Rx chr. Available
RR1 12H (13)	R	End of Frame (SDLC)	CRC/Framing Error	Rx Overrun Error	Parity Error	Result Code			All Send
RR2 13H	R	Interrupt vector							
WR2 13H	W	Interrupt vector							

(Attention)

Though WR0 and RR0 are able to be read or written at any time, when the other resistors (WR1 ~ 7, RR1 ~ 2) are to be read or written, the resistor-pointer should be set to WR0 right before being read or being written.

LSI 8255 **Function: Printer interface**

I/O address 14H ~ 17H

17H W

7	6	5	4	3	2	1	0
1 Mode select	Port A Mode Select 00: Mode ϕ (bit) ★01: Mode 1 (byte) 10: Mode 2 (two-way)		Port A 1: Input ★0: Output	Port C High-order 1: Input ★0: Output	Port B Mode 1: Mode 1 (byte) ★0: Mode ϕ (bit)	Port B ★1: Input 0: Output	Port C Low-order 1: Input ★0: Output

Mode set command (Set ★mark in IPL)

17H W

7	6	5	4	3	2	1	0
0 Bit control	0	0	0	Bit No. (Port C) 0 ~ 7			1: Set 0: Reset

Bit control

14H W

7	6	5	4	3	2	1	0
Printer Output Data							

Output data

15H R

7	6	5	4	3	2	1	0
Select out	Power off detect	Ready	No paper detect	Error	0	0	RS-232C DSR signal

Status input

16H R

7	6	5	4	3	2	1	0
OBF	Interrupt enable	Reset	No paper detect	Interrupt flag	0	0	Strobe signal

Control Use the above bit controls to set/reset each bit of this register.

MSI74LS273 **Function: Memory bank switch and DIP switch**

I/O address 18H

	7	6	5	4	3	2	1	0
18H W	#3	#2	#1	#0 Memory bank register	External memory select	Speaker continuous ON	Software timer trigger	Speaker timer trigger

18H R	DIP switch data input

LSI **Function: FDD motor control/memory bank status**

I/O address 30H

	7	6	5	4	3	2	1	0
30H W	FDD motor start pulse							

FDD motor is started by accessing this port. See the calendar clock of 46818 about the motor on time.

	7	6	5	4	3	2	1	0
30H R	#3	#2	#1	#0 Memory bank register	FDD ready signal	Interrupt flag from the clock LSI	$\overline{\text{FDD motor ON}}$	Interrup flag from FDC

The above status information can be obtained by reading this port.

LSI 765AC **Function: FDD Controller**

I/O address 34H ~ 35H

	7	6	5	4	3	2	1	0
34H R	RQM request	Data In/Out Read/Write	Non DMA	DDC Busy	#3	#2	#1	#0 Device Busy

Status register

35H R/W	Data register

Data and command register

For control of this port, see the μPD765AC user's manual.

I/O address 38H ~ 3BH

38H R

7	6	5	4	3	2	1	0
Light Pen Detect	Horizontal Blank	Vertical Sync.	DMA Excute	Drawing	FIFO EMPTY	FIFO FULL	DATA READY

39H W

GDC command

For details, see the 7220 manual.

38H W

GDC parameter

39H R

GDC data

3AH W

Zoom control (Zoom magnification: x 1)

A command to set the zoom magnification at the hardware level, since the functions of 7220 are insufficient at the zoom read command.

3BH W

Light pen service request F/F clear (DATA / Don't care)

Next light pen interrupt is not effected unless the port is accessed each time the light pen interrupt is accepted.

2CH

This port informs whether the video board which is provided on QX-10 is for the color monitor or for the mono chrome monitor.

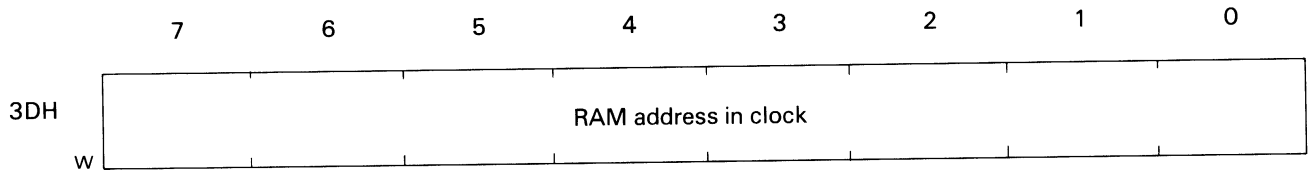
When this port is read, following signals will be provided.

In case of being provided the mono chrome board: bit 0 = 0, bit 1 ~ 8 = 1

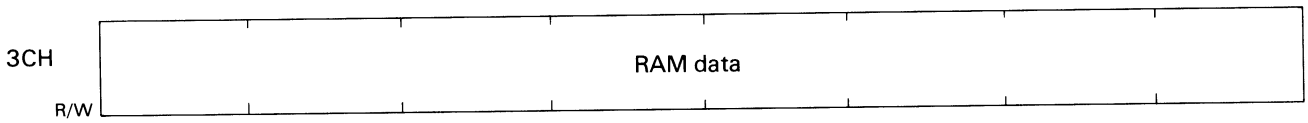
In case of being provided the color monitor: bit 1 = 1, bit 1 ~ 8 = 1

LSI 46818 **Function: Clock with calender**

I/O address 3CH ~ 3DH



When the RAM in the clock IC is accessed, first the RAM address must be written into this port and then the RAM data must be read/writen.



Address and data come as follows.

3DH port		3CH port
00H R/W	Second data	00 ~ 59 (BCD mode) 00 ~ 3B (Binary mode)
01H R/W	Alarm second data	00 ~ 59 (BCD mode) 00 ~ 3B (Binary mode)
02H R/W	Minute data	00 ~ 59 (BCD mode) 00 ~ 3B (Binary mode)
03H R/W	Alarm minute data	00 ~ 59 (BCD mode) 00 ~ 3B (Binary mode)
04H R/W	Hour data	01 ~ 0C/81 ~ 8C (Binary 12-hour mode) 01 ~ 12/81 ~ 92 (BCD 12-hour mode) 00 ~ 17 (Binary 24-hour mode) 00 ~ 23 (BCD 24-hour mode)
05H R/W	Alarm hour data	01 ~ 0C/81 ~ 8C (Binary 12-hour mode) 01 ~ 12/81 ~ 92 (BCD 12-hour mode) 00 ~ 17 (Binary 24-hour mode) 00 ~ 23 (BCD 24-hour mode)
06H R/W	Day-of-week data	(01 ~ 07)
07H R/W	Day data	01 ~ 31 (BCD mode) 01 ~ 1F (Binary mode)

LSI 46818 **Function: Clock with calender**

Continued

I/O address 3CH ~ 3DH

	3DH port 7	6	5	4	3CH port 3	2	1	0
08H R/W	Month data { 01 ~ 12 (BCD mode) / 01 ~ 0C (Binary mode) }							
09H R/W	Year data { 00 ~ 99 (BCD mode) / 00 ~ 63 (Binary mode) }							
0AH R/W	Update in-process (Ready only)	0	1	0	Setting of FDD motor timer length 01: 1/8 sec. ~ 0F: 1024 sec. (1/16 x 2^n sec.)			
		Setting of reference clock (32.768 kHz)						
0BH R	0: Update start 1: Update stop	Periodic interrupt enable	Alarm interrupt enable	Update end interrupt enable	Square wave output enable (FDD timer)	0: BCD mode 1: Binary mode	0: 12-hour 1: 24-hour	Special update enable
0CH R	Interrupt flag	Periodic interrupt flag	Alarm interrupt flag	Update end interrupt flag	0	0	0	0
0DH R/W	RAM valid	0	0	0	0	0	0	0
0EH ~ 3FH R/W	User RAM area							

PWD (When the battery power drops to zero). Indicates that the power supply is dropping.

LSI **Function: PROM, CMOS RAM select**

I/O address 1CH, 20H

	7	6	5	4	3	2	1	0
1CH W								1: disable 0: enable

P-ROM Select

	7	6	5	4	3	2	1	0
20H W								1: enable 0: disable

C-MOS RAM select

LSI 8237-5 **Function:** **DMA controller #1, #2**

I/O address 40H ~ 4FH (#1)
50H ~ 5FH (#2)

	7	6	5	4	3	2	1	0
40H (50) R/W	Ch.0 Base address							
41H (51) R/W	Ch.0 Word address							
42H (52) R/W	Ch.1 Base address							
43H (53) R/W	Ch.1 Word address							
44H (54) R/W	Ch.2 Base address							
45H (55) R/W	Ch.2 Word address							
56H R/W	Ch.3 Base address							
57H R/W	Ch.3 Word address							
48H (58) W	PACK 0: Low act 1: High	DREQ 0: High 1: Low	Write Select 0: Late Wr. 1: Extend.	Priority 0: Fix 1: Rotate	Timing 0: Normal 1: Compres.	Controller 0: enable 1: disable	Address Holt Ch. 0 0: disable 1: enable	Mem to Mem. 0: disable 1: enable
				Command register				
48H (58) R	#0	#1	#2	#3	#0	#1	#2	#3
	Existence of DREQ signal				Existence of terminal count			
	Status register							
49H (59) W	0	0	0	0	0	DREQ 0: Reset 1: Set	DMA channel #0 ~ #3	
	Request status							
4AH (5A) W	0	0	0	0	0	DMA mask 0: No mask 1: Mask	DMA channel #0 ~ #3	
	Single mask register							
4BH (5B) W	00: Demand mode 01: Single mode 10: Block transfer mode 11: Cascade mode	Address 0: increment 1: decrement	Auto Init. 0: disable 1: enable		Transfer mode 00: Verify 10: Read 01: Write		DMA channel 0 ~ 3	
			Mode register to/from Mem.					
4CH (5C) W	Clear byte pointer F/F							
	Clears the F/F to determine high or low order when the address work count is read/written.							
4DH (5D) R	Temporary register							
	Latest data transferred with memory							
4DH (5D) W	Master clear							
	Same as the hardware reset							
4FH (5F) W	0	0	0	0	#3	#2	#1	#0
	All mask register					o: Clear mask bit 1: Set mask bit		

4.11 Speaker Circuit (Sound Generator)

The QX-10 is designed to permit free programming of the scale and length of the sound from the speaker by changing the frequency using the timer counter μPD8253.
This function is enabled by I/O selection of the timer counter μPD8253 (14E/16E) or memory bank register LS273 (18F) and setting appropriate data.
Connection of these signals is shown in Fig. 4-21.
The signal supply line to the speaker and sound setting items bythat signal are shown in Table 4-3.

Connection		Setting item
IC' 23H' pin 13	Timer counter 8253-5 (16E) OUT φ output	Setting of speaker frequency. Usually, the speaker frequency is set to about 1 kHz by IPL.
IC' 23H' pin 5	Time counter 8253-5 (14E) OUT 0 output	Approx. speaker timer setting. Usually, the speaker timer is set to about 100 ms by IPL.
IC' 23H'pin 4	Memory bank register LS273 (18F) Q2 output	Setting of continued or discontinued speaker sound. Continued sound is obtained by setting 1 in the bit 2 of the memory bank register.

Table4-3 Setting of speaker sound

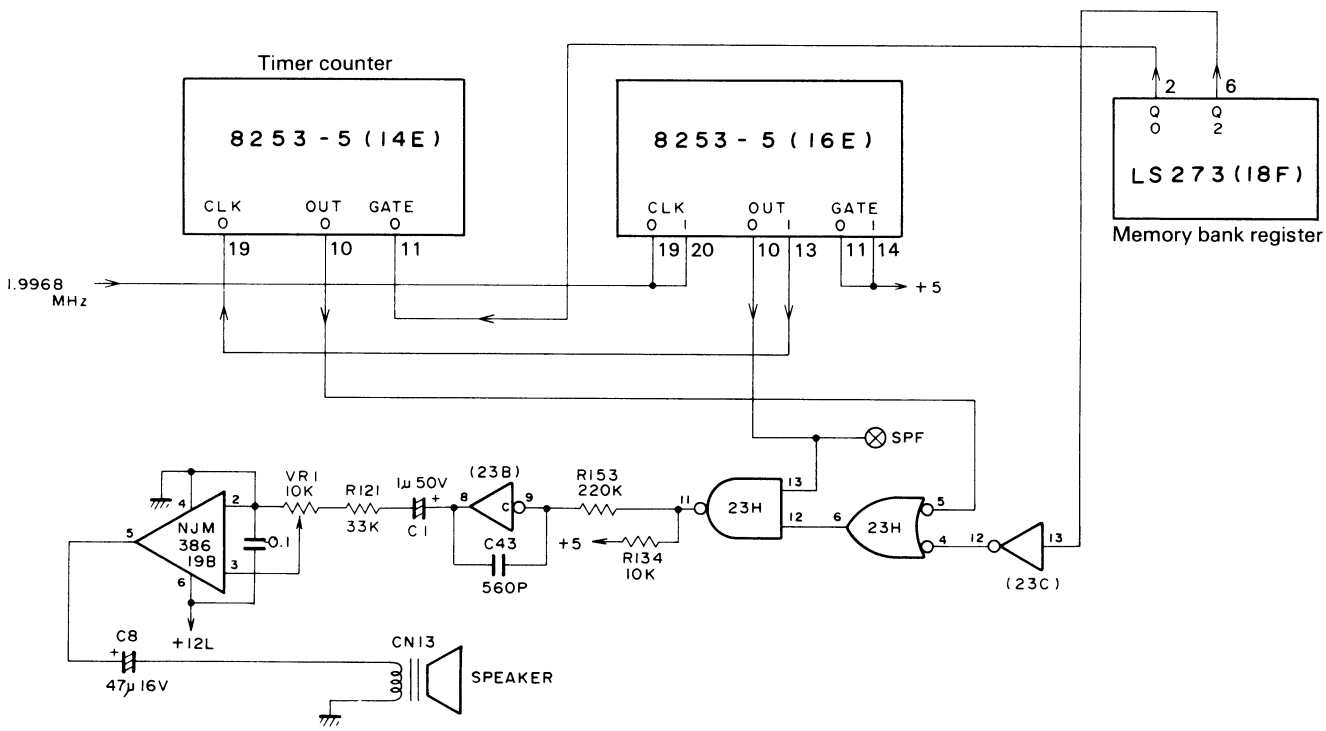


Fig. 4-21 Sound generator

4.12 Programmable Interval Timer μPD8253-5

Two programmable interval timers μPD8253-5 (14E/16E) compatible with Z80 are provided to set the speaker frequency, keyboard clock or RS-232C baud rate.
The μPD8253-5 (14E/16E) has three counters with the same function, enabling setting of operation mode at a program level.

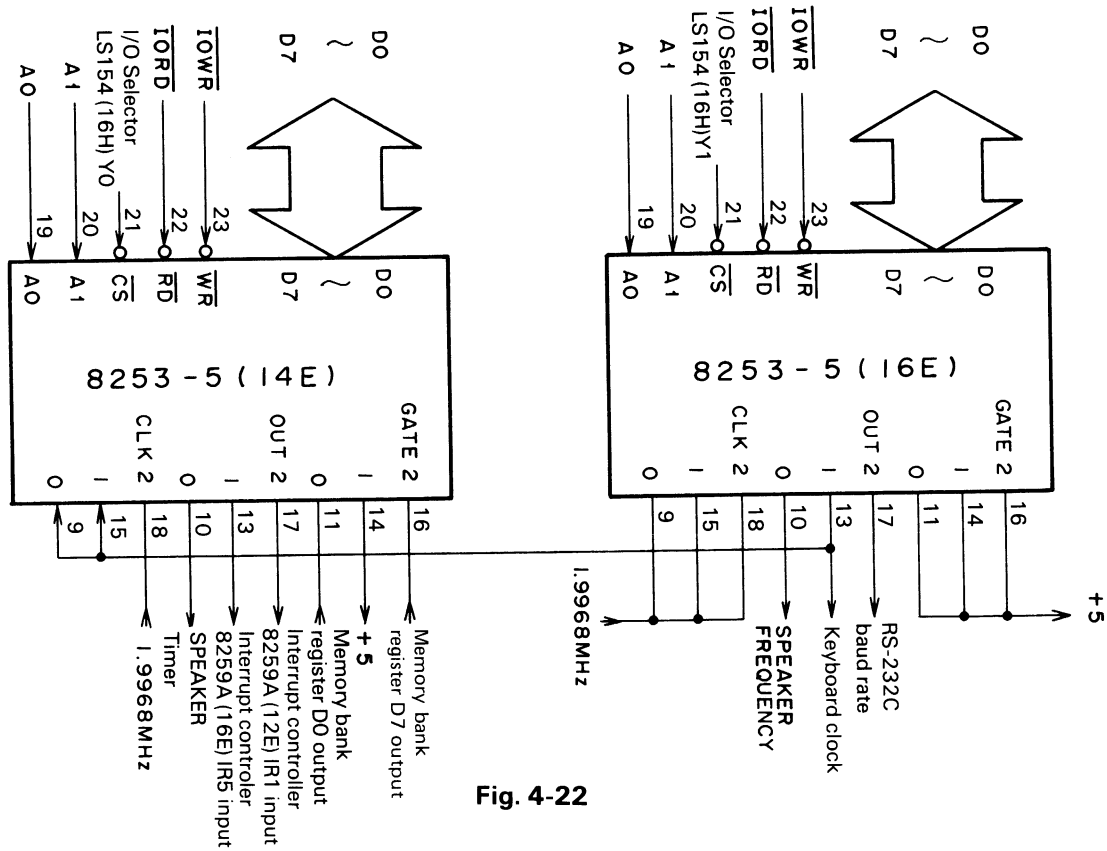


Fig. 4-22

Setting of this timer counter operation is as shown in 4.10 I/O command. The operation mode is set by the binary data of low-order 1 to 3 bits of the I/O command.

The relationship between the operation mode and gate signal is as shown in Table 4-4.

Mode	Operation	Gate signal		
		"L" or trailing edge	Leading edge	"H"
0	OUT becomes 1 when the specified count ends.	Count stop	–	Count
1	One shot pulse (active low) of the specified length is output.	–	Count start OUT becomes L by the next CLK.	–
2	An n-dividing counter of input clock. However, since OUT becomes 0 only for one clock cycle, the duty becomes 1/n.	Count stop OUT = H	Count start	Count
3	An n-dividing counter of input clock. The duty is 1/2 when the count is even, and n-1/2n when it is odd.	Count stop OUT = H	Count start	Count
4	When the specified count ends, a strobe pulse of one clock cycle (active low) is output.	Count stop	–	Count
5	Count is started by a trigger input, and when the specified count ends, a strobe pulse of one clock cycle (active low) is output.	–	Count start	–

Table 4-4

Connection and operation of the μPD8253-5 in QX-10 are shown in Table 4-5. For detailed functions of each terminal, see the attached μPD8253-5.

	Counter No.	CLK	Gate	OUT	Operation
#1	0	Keyboard clock 1200 bps	Memory bank register D0 output	Speaker timer	Approx. speaker timer setting. Set to about 100 ms in IPL.
	1	↑	+5V	Interrupt controller 8259A (10E) IR5: input	Software timer
	2	clock 1,9968 MHz	Memory bank register D7 output	Interrupt controller 8259 (12E) IR1 input	Software timer
#2 (16E)	0	↑	+5V	Speaker frequency	Setting of the speaker frequency. Set to about 1kHz in IPL.
	1	↑	↑	Keyboard clock	Setting the keyboard clock. Set to 1200 bps in IPL. (1,9968 MHz ÷ 1664)
	2	↑	↑	RS-232C baud rate	Setting RS-232C clock. Set to 9600 bps in IPL. (1,9968 MHz ÷ 208)

Table 4-5

4.13 Serial Interface μPD7201

The μPD7201 MPSC (Multi-protocol Serial Controller) controls serial-parallel and parallel-serial conversions for data processing between the CPU and MODEM or other serial data processors.
The MPSC has two channels, and uses channel A as an interface for QX-10 and B for RS-232C.

Channel	Interface
A	Keyboard
B	RS-232C

(1) Channel A: Keyboard interface

Data transfer between the CPU and keyboard is made through channel A of μPD7201. Data transfer with the keyboard is made at the speed of 1200 bps in the start-stop tuning format (8 bits/chr, 1 stop bit odd parity).

The meanings of each signal line are shown in Table 4-6.

Keyboard	Direction	QX-10	Function
RTS	→	$\overline{\text{DCDA}}$	Indicates transmission permission from an external device. Operates in the same way as CTS.
CTS	←	$\overline{\text{DTRA}}$	Informs the receiving device that the transmitting communication channel is ready.
DTR	→	$\overline{\text{CTSA}}$	Indicates transmission permission from an external device and controls data transmission.
RXD	←	TXDA	Serial data line for transmission.
TXD	→	RXDA	Serial data line for reception.

Table 4-6

(2) Channel B: RS-232C interface

USART IC (11B: 75188 line driver, 13B, 13C: 75189 line receiver) conformable to the specifications of RS-232C is used as an interface between RS-232C and μPD7201.

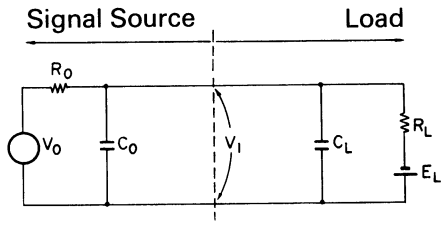
When a positive voltage is supplied, these operate on the specifications of RS-232C. The meanings of each signal line are shown in Table 4-7. The jumper wires of the interface are shown in Table 4-8.

External device	Direction	QX-10	Function
TXD	←	TXDB	Serial data line for transmission
RTS	←	RTSB	Signal to indicate that the transmitting side is making a transmission request.
TXC	←	–	Output as a clock to TXD.
CTS	→	$\overline{\text{CTSB}}$	Indicates transmission permission from an external device and controls data transmission.
DCD	→	$\overline{\text{DCDB}}$	Indicates transmission permission from an external device. Function is the same as $\overline{\text{CTSB}}$.
DSR	→	8255A(18B) PBO	This signal shows whether machine is ready or not.
RXD	→	RXDB	Receiving data input terminal
REV	←	DTRB	Informs the receiving device that the transmitting communication channel is ready.
DTR	←	DTRB	Informs the receiving device that the transmitting communication channel is ready.
RXC	→	$\overline{\text{RXCB}}$	Samples the receiving data at the leading edge of this signal.
DB	→	$\overline{\text{TXCB}}$	Transmitting data is output at the trailing edge of this signal.

Table 4-7

► Specifications of RS-232C

(1) Interconnection equivalent circuit (JIS C 6361)



V_O: Open circuit voltage of signal source.
R_O: Total effective DC resistance of signal source measured at interconnection point.
C_O: Total effective capacity of signal source measured at interconnection point.
V_I: Voltage for signal grounding line or common return line at interconnection point.
C_L: Total effective load capacity measured at interconnection point.
R_L: Total effective load resistance measured at interconnection point.
E_L: Open circuit voltage of load.

Signal Source		Load	
Open circuit voltage V0	: 25V (absolute value) or less	Load resistance RL	: 3 ~ 7 kΩ
Signal voltage V1 (for load 3 ~ 3 kΩ)	: 5 ~ 15V (absolute value)	Input threshold	: 3V (absolute value)
Minimum output resistance at power off	: 300Ω	Input voltage	: Max. 25V (absolute value)
Maximum output current at short	: 500 mA (absolute value)	Total effective load capacity CL	: 2500 pF or less
Through rate: Max	: 30V/μs	Open circuit voltage EL	: 2V or less

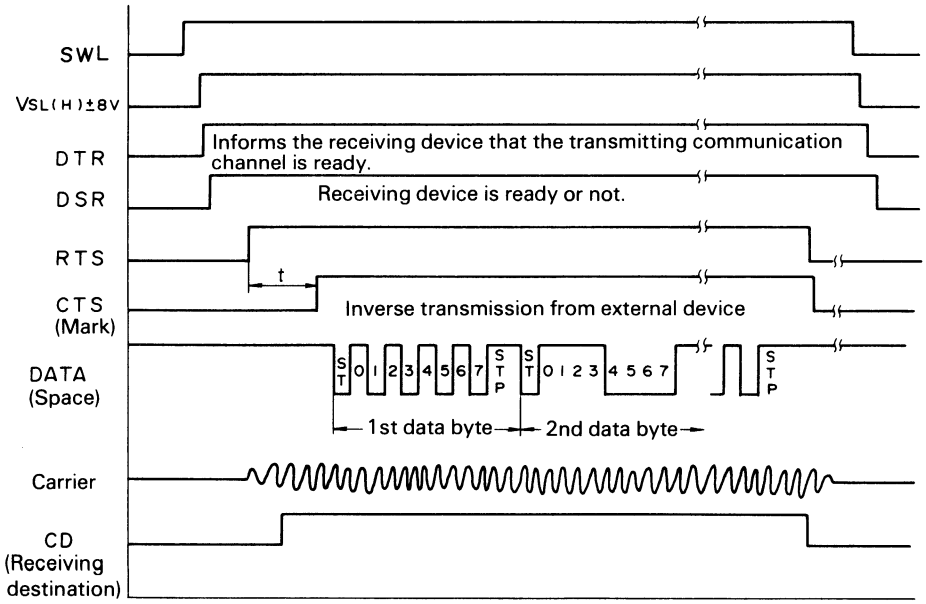
Fig. 4-23

(2) Signal polarity
Mark = Logic "1" (–3 ~ –25V): Stop bit
Space= Logic "0" (+3 ~ +25V): Start bit

(3) Word length
Start bit: 1 bit
Data bit: 7 or 8 bits
Stop bit: 1-bit length or longer

(4) Bit rate
110 BPS ~ 4800 BPS

► Operation timing of RS-232C (Using MODEM)



*t: Delay time registered by MODEM to be ready for transmission.

Fig. 4-24

► **Jumper Wires of RS-232C Interface**

Jumper			Direction	μPD7201	Function
J1	A	DTR	←	$\overline{DTRB}$	Normal use
	B	REV	←		Reverse channel
J2	A1	Input of RXCK signal from CTC	→	$\overline{TXCB}$	Operated by the internal clock.
	A2			$\overline{RXCB}$	
	B1	RXC	→	$\overline{TXCB}$	Operated by an external clock.
	B2	DB	→	$\overline{RXCB}$	
J3	A	Pull-up of +5V power line		PBO(8255)	Pull-up of the control line. Space status is set with the pull-up on.
	B			$\overline{DCDB}$	
	C			$\overline{CTSB}$	

Table 4-8

(3) MPSC μPD7201 ⇄ CPU or memory

Data, command and status are transferred in parallel between MPSC μPD7201 and the CPU or memory. The meanings of each signal line are shown in the Table 4-10. Modes set by combination of signals are shown in Table 4-9.

B/$\overline{A}$	C/$\overline{D}$	$\overline{WR}$	$\overline{RD}$	$\overline{CS}$	Function
0	0	0	1	0	Channel A — Writing transmission data
1					Channel B
0	0	1	0	0	Channel A — Reading received data
1					Channel B
0	1	0	1	0	Channel A — Writing the command/parameter register.
1					Channel B
0	1	1	0	0	Channel A — Reading from the status/vector register.
1					Channel B

Table 4-9

MPSC μPD7201	Direction	CPU/MEM	Function
D0 ~ D7	→	D0 ~ D7	An 8-bit two-way data bus used for transmission of data, command and status between MPSC and CPU.
$\overline{INTR}$	→	Interrupt controller 8259A (12E) IR4 input	An interrupt request signal output terminal.
B/$\overline{A}$	←	A0	Specifies the channel to write data onto the data bus or read the data from the data bus in the write/read operation. H: Channel B L: Channel A
C/$\overline{D}$	←	A1	Indicates that the information on the data bus is data, command or status, in the write/read operation.
$\overline{CS}$	←	I/O decoder LS154 (16H) Y4 output	Enables data/command transfer from CPU to MPSC (write cycle) or data/status transfer from MPSC to CPU (read cycle). This SIO is assigned to the I/O addresses 10H ~ 13H.
$\overline{RESET}$	←	$\overline{RESET}$	The same signal as the reset signal for the CPU is connected. Namely, the MPSC μPD7201 is reset in the following cases. 1 Reset by power on 2 Reset by the RESET switch (manual reset) 3 Reset from an external option
$\overline{RD}$	←	$\overline{IORD}$	Controls reading data/status from MPSC μPD7201 to CPU or memory.
$\overline{WR}$	←	$\overline{IOWR}$	Controls writing data/command from CPU or memory to MPSC.
$\overline{RXCA}$	←	CTC 8253-5 (16E) OUT1 output	Samples the data received from the keyboard at the leading edge of this signal.
$\overline{TXCA}$	←	CTC 8253-5 (16E) OUT1 output	Data is transmitted to the keyboard at the trailing edge of this signal.
ϕ	←	3.9936 MHz	A signal of 3.9936 MHz is supplied like the clock of CPU. The system clock rate needs to be increased to 4.5 times the data rate.

Table 4-10

► **Keyboard Power Supply Circuit**

The keyboard is powered by +12V of Q10SYM board through pin 3 of connector 1. To prevent a malfunction caused by unstable voltage at power on, supply of +12V is stopped by the circuit shown in Fig. 4-26 by making the reset signal to the CPU active for the duration while a low pulse is output from the Q-terminal which follows the time constant of the externally mounted CR of the single shot LS123 (24K). That is, when the reset signal to the CPU is active, the B-terminal input of LS123 is set to low level. On the other hand, since the A-terminal input is connected to the ground, when the B-terminal input rises to high level, a low level signal of 100 ~ 200msec which follows the time constant of the externally mounted RC is generated at the Q-terminal as an output.

By the gate of IC23K, these signals make the output of pin 11 of IC23K high level for about 100 ~ 200msec. from power on to leading edge of the Q-terminal output signal.

Since this signal makes the base of transistor Q2 high level via the two-stage inverter, it cuts off Q2. Therefore, during this reset period, +12V is not supplied to the keyboard.

When the reset signal is released, the base of Q2 is set to low level, and Q2 is turned on and +12V is supplied to the keyboard. The voltage waveform of this circuit is shown in Fig. 4-25.

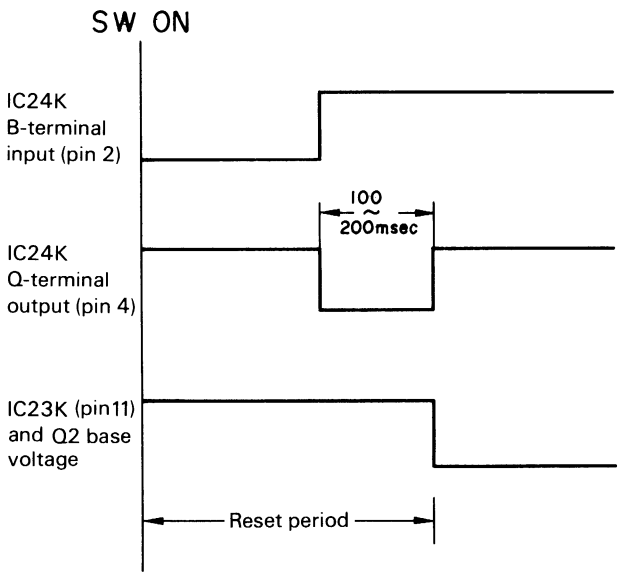


Fig. 4-25 Timing chart of keyboard power supply circuit

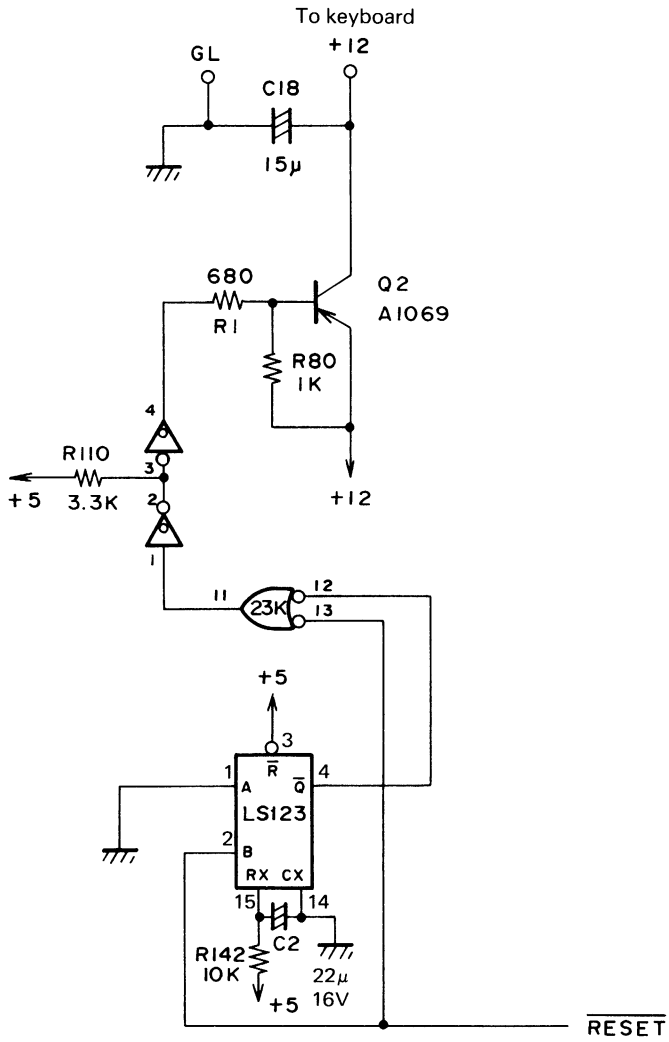


Fig. 4-26 Keyborad power supply circuit

4.14 Interrupt Controller μPD8259

This system uses two programmable interrupt controllers μPD8259 to give priority to 15 levels of interrupt requests made from an external device for controlling the interrupt to the CPU. In this case, as shown in Fig. 4-27, the SP (Slave Program) terminal of IC 12E is connected to +5V and SP terminal of IC 10E to GND, thereby allocating the μPD8259 to the master and slave programs.
The master program is preferentially interrupted. Regarding IR (Interrupt Request) terminals, IR0 has priority over IR7.
Interrupt addresses are shown in Table 4-11.
The actual address table after completion of IPL will be the value obtained by adding 780H to the relative addresses of the left side.

▶ Interrupt Sequence

When an interrupt routine address is generated, the μPD8259 is capable of jumping directly or indirectly to the requested specific interrupt routine without polling the interrupt requesting device.

(1) When one or more interrupt request inputs (IR0 ~ 7) become high level, all the corresponding bits of IRR (Interrupt Request Register) are set.
(2) The μPD8259 evaluates these requests and sends the INT signal to the CPU when they are recognized as appropriate.
(3) Recognizing the INT signal, the CPU returns one $\overline{\text{INTA}}$ pulse to the μPD8259.
(4) Receiving the first $\overline{\text{INTA}}$ pulse sent from the CPU, the μPD8259 outputs the CALL instruction code (11001101) to the data bus.
(5) Receiving the CALL instruction, the CPU sends two $\overline{\text{INTA}}$ pulses back to the μPD8259.
(6) Synchronizing with these two $\overline{\text{INTA}}$ pulses, the μPD8259 outputs the programmed subroutine address to the data bus: the low-order 8 bit addresses for the first pulse and the high-order 8 bit addresses for the second pulse.
    At the trailing edge of the second pulse, the μPD8259 sets the ISR (In-Service Register) bit with the highest priority and resets the corresponding IRR bit.
(7) Generation of a 3-byte call instruction by the μPD8259 has now been completed.

Connection		Relative address	Interrupt cause	
Master	IR0	0000	Power down detection interrupt	High-order
	IR1	0004	Software timer # 1 interrupt	
	IR2	0008	External (option) interrupt # 1	
	IR3	000C	External (option) interrupt # 2	
	IR4	0010	Keyboard/RS-232C interrupt	
	IR5	0014	CRT/light pen interrupt	
	IR6	0018	Floppy controller interrupt	
				Priority
Slave	IR0	0020	Printer interrupt	
	IR1	0024	External (option) interrupt # 3	
	IR2	0028	Calendar clock interrupt	
	IR3	002C	External (option) interrupt # 4	
	IR4	0030	External (option) interrupt # 5	
	IR5	0034	Software timer # 2 interrupt	
	IR6	0038	External (option) interrupt # 6	
	IR7	003C	External (option) interrupt # 7	Low-order

Table 4-11 Interrupt addresses

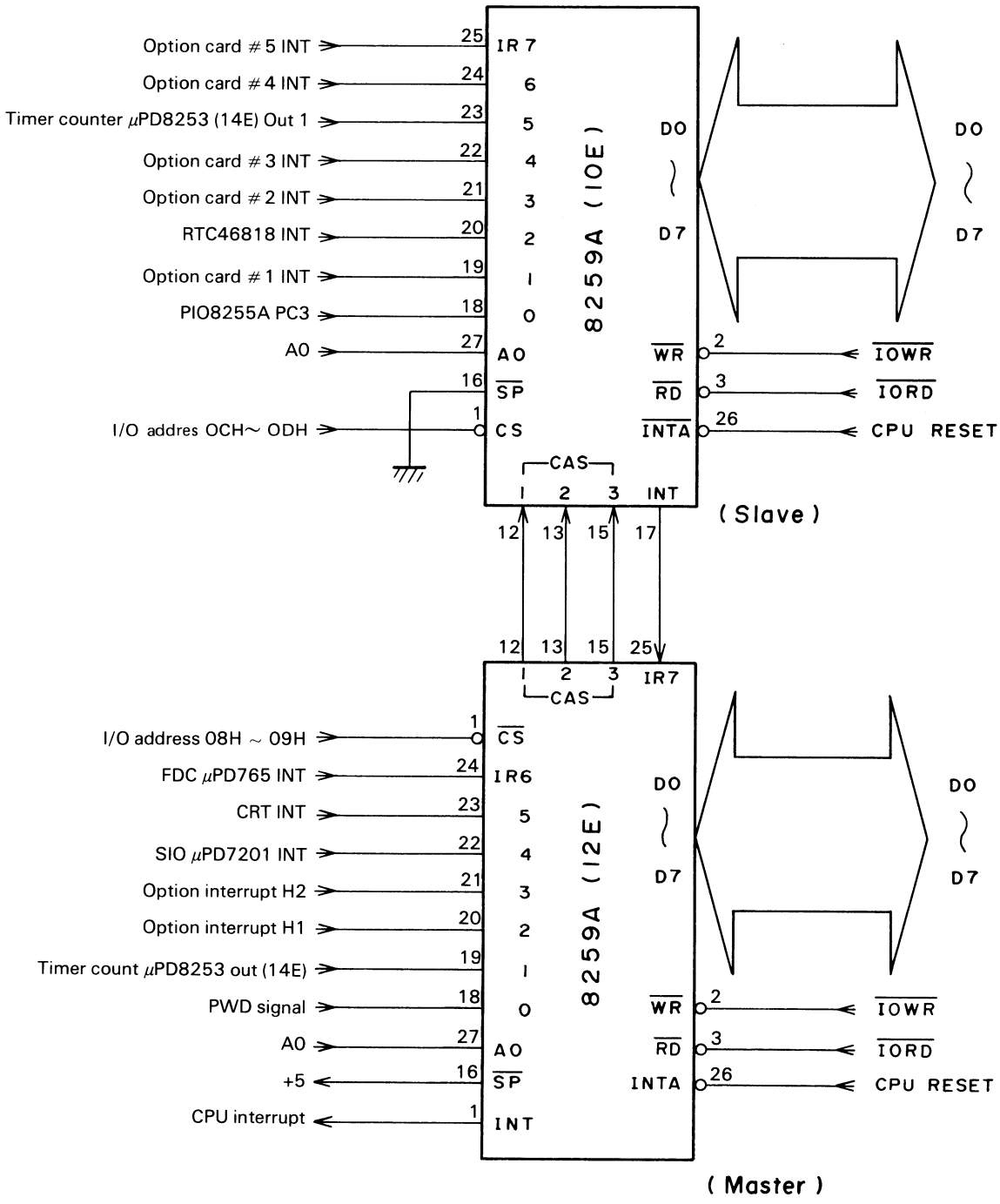

Option card # 5 INT
Option card # 4 INT
Timer counter μPD8253 (14E) Out 1
Option card # 3 INT
Option card # 2 INT
RTC46818 INT
Option card # 1 INT
PIO8255A PC3
A0
I/O addres OCH~ ODH
25
24
23
22
21
20
19
18
27
16
1
IR 7
6
5
4
3
2
1
0
A0
SP
CS
8259A (IOE)
DO
D7
WR
RD
INTA
2
3
26
IOWR
IORD
CPU RESET
CAS
1 2 3
INT
(Slave)
12 13 15 17
12 13 15 25
1 2 3
IR7
I/O address 08H ~ 09H
FDC μPD765 INT
CRT INT
SIO μPD7201 INT
Option interrupt H2
Option interrupt H1
Timer count μPD8253 out (14E)
PWD signal
A0
+5
CPU interrupt
1
24
23
22
21
20
19
18
27
16
1
IR6
5
4
3
2
1
0
A0
SP
INT
8259A (12E)
(Master)

Fig. 4-27

4.15 Printer Interface Circuit

The QX-10 uses PIO (Parallel Input/Output Controller) 8255 to realize the interface of Centronics parallel specifications.

The interface circuit is shown in Fig. 4-29. The functions of terminals are shown in Table 4-13.

► PIO Operation Mode

The PIO 8255 (18B) is originally set to mode 1.

In this mode, port A is assigned as a data bus output to the printer and port B as a data line input of status information from the printer.

Port C is, as shown in Fig. 4-28, designed to supply $\overline{INT}$ and $\overline{ACK}$ signals accompanying transfer of input/output data of ports A and B.

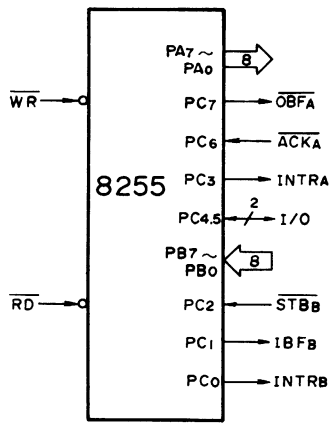


Fig. 4-28

► Data Transfer Sequence

Data transfer with the printer is made in the following sequence. The timing is shown in Fig. 4-30.

(1) Data is output from the QX-10 to the printer via data buses DB0 ~ DB7, and at the same time a data strobe pulse is output from PC0.
The printer reads the data at the trailing edge of the data strobe pulse.

(2) After reading the data, the printer goes into data processing for printing. During this period, the printer cannot accept data, and sets the $\overline{RDY}$ signal for data input inhibition to the high level.

(3) After completing the data processing, the printer sets the $\overline{RDY}$ signal to low level and then sends the $\overline{ACK}$ signal for data transfer request to the QX-10 and goes into the next data accept operation.

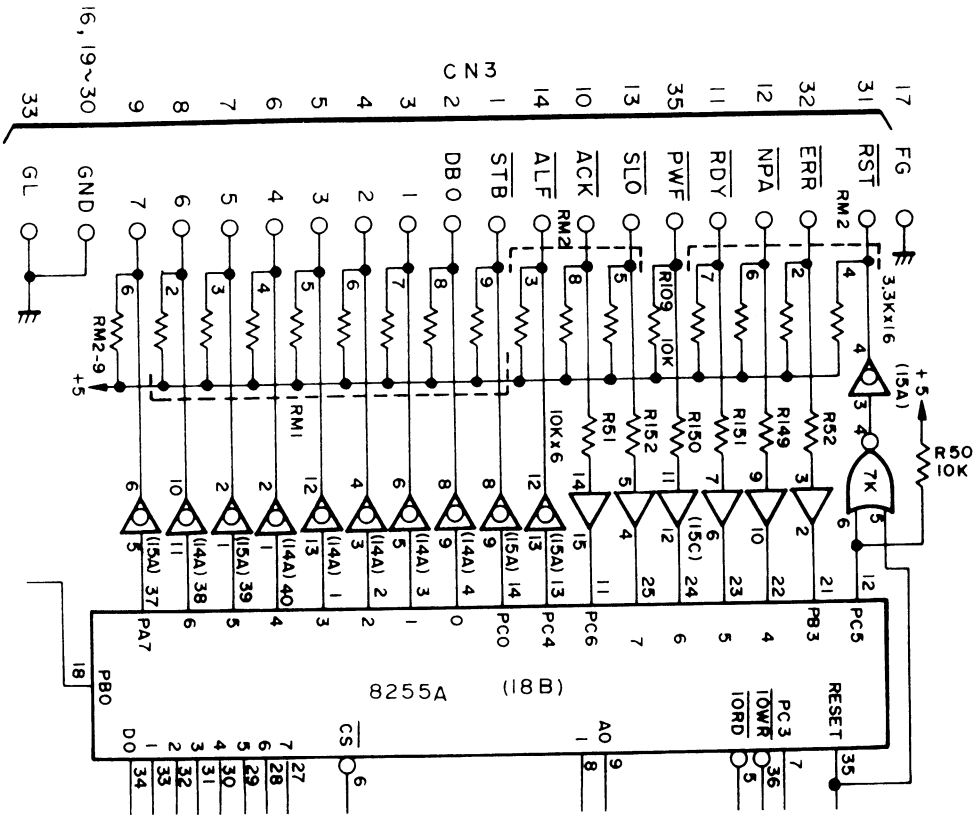


Fig. 4-29

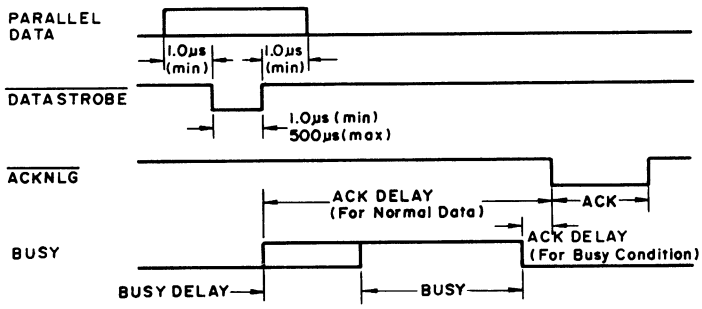
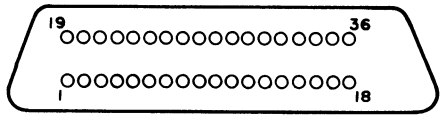


Fig. 4-30 Centronics timing chart

Terminal	Signal	Terminal	Signal
1	DATA STROBE	19	TWISTED PAIR GND
2	DATA 1	20	TWISTED PAIR GND
3	DATA 2	21	TWISTED PAIR GND
4	DATA 3	22	TWISTED PAIR GND
5	DATA 4	23	TWISTED PAIR GND
6	DATA 5	24	TWISTED PAIR GND
7	DATA 6	25	TWISTED PAIR GND
8	DATA 7	26	TWISTED PAIR GND
9	DATA 8	27	TWISTED PAIR GND
10	ACKNLG	28	TWISTED PAIR GND
11	BUSY	29	TWISTED PAIR GND
12	PE	30	INPUT PRIME RETURN
13	SLCT	31	INPUT PRIME
14	±0V	32	FAULT
15	OSCXT	33	LD
16	±0V	34	EX PRIME
17	CHASSIS GND	35	
18	+5V	36	

Table 4-12 Centronics connectors specifications



Connector part No. 552742-1 (AMP)

Terminal name	Signal	I/O	Function
D0 ~ D7	Data bus input	I/O	Connected to the CPU data bus and used for data transfer with the CPU.
$\overline{CS}$	Chip select	I	A signal obtained by decoding the CPU address bus (A0 ~ A7) by the I/O selector LS154 (16H) is supplied. This PIO μPD8255A is allocated to the I/O addresses 14H ~ 17H.
PA0 ~ PA7	Data bus output	O	Used as a data output bus to the printer.
PB0	DSR	I	This signal shows whether machine is ready or not. (RS-232C signal)
PB3	$\overline{ERR}$	I	Accepts the error signal from the printer. A low active signal.
PB4	$\overline{NPA}$	I	Accepts the no paper detect signal from the printer.
PB5	$\overline{RDY}$	I	Low level: Indicates that the printer is ready to receive data. High level: Indicates that the printer is busy for data processing.
PB6	$\overline{PEF}$	I	A signal to detect printer power down. Low active.
PB7	$\overline{SLO}$	I	A signal to indicate that the printer is not in the error state, but in the select (effective operation) state.
PC0	$\overline{STB}$	O	A strobe pulse generated when data is sent to the printer. Low active signal.
PC3	IR0	O	An interrupt input to the interrupt controller 8259A (10E).
PC4	$\overline{ALF}$	O	By setting this signal to low level, the printer automatically feeds line after printing the input data.
PC5	RST	O	Valid at reset by power on, reset switch or an external I/O. At this time, all the internal registers (including the control register) are cleared. An active low signal.
A0, A1	A0, A1 (CPU) Port Address	I	Connected to the CPU addresses A0 and A1 and used for mode setting of 8255A in cooperation with $\overline{IORD}$ and $\overline{IOWR}$ signals.
$\overline{IORD}$	$\overline{IORD}$ (From CPU)	O	Supplied from the CPU and used to set the mode of 8255A.
$\overline{IOWR}$	$\overline{IOWR}$ (From CPU)	O	A write signal to 8255A. By applying a low level signal to this terminal, data or control words can be written.

Table 4-13

4.16 Floppy Disk Controller μPD765

4.16.1 FDC Clock Supply Circuit

The FDC clock supply circuit has its own clock different from the clock of the main CPU.

The clock is 4 MHz, which is obtained by dividing the original oscillation of 8 MHz into two by the 4-bit binary counter LS393 (19H).

The $\overline{WCLK}$ signal which gives the timing signal of data writing into a drive is obtained by taking the logic of Q_B, Q_C and Q_D outputs of the counter LS393 (19H) and dividing the original oscillation to make a timing signal of 500 kHz.

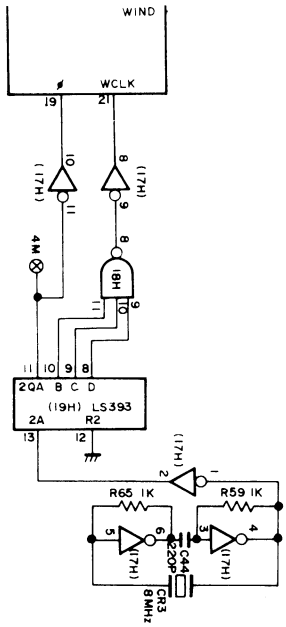


Fig. 4-31

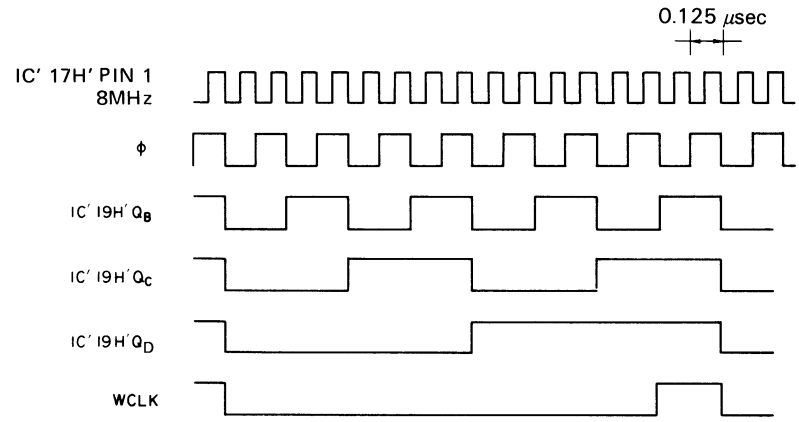


Fig. 4-32

4.16.2 Reading the Memory Bank Resister and the Status of FDC

As shown in Fig. 4-33, the memory bank register and FDC status information are read into the CPU or other I/O device through the 3-state buffer LS541 (20E).

$\overline{E1}$ and $\overline{E2}$ signals which permit data output of LS541 are supplied by the $\overline{IORD}$ signal from the CPU and Y12 output ($\overline{CSFDM}$) signal of the I/O selector LS154 (16H), respectively.

Therefore, the status information is read by reading the I/O address 30 H.

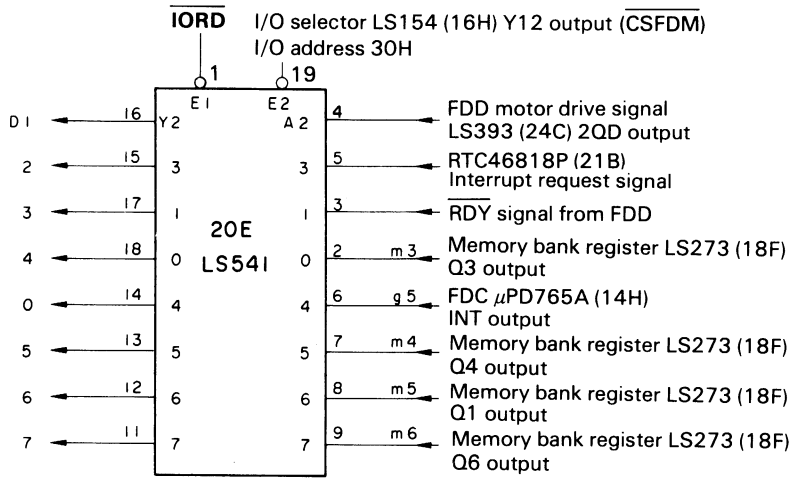
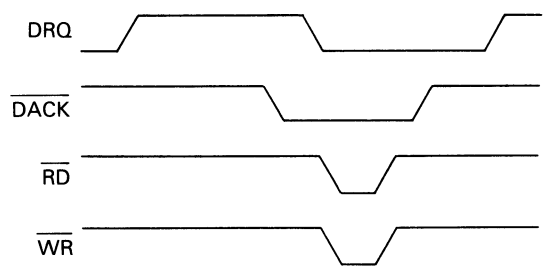
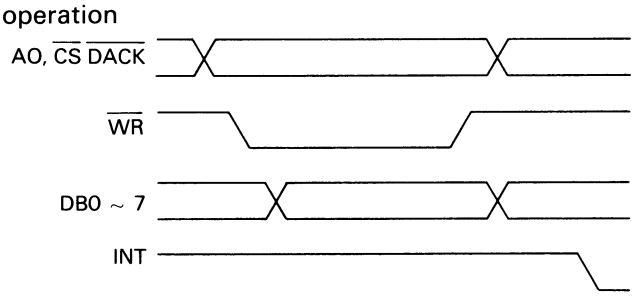
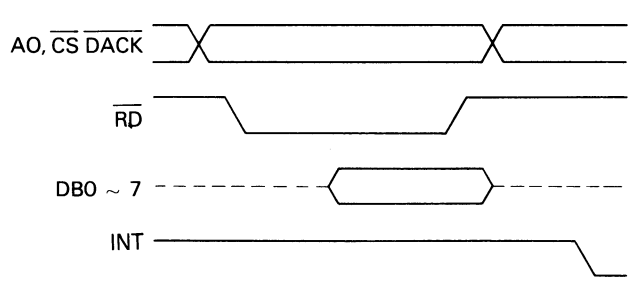


Fig. 4-33

4.16.3 CPU ⇆ FDC μPD765

The FDC μPD765 and system data and control signals are connected as shown in Table 4-14.

Signal name	I/O	Function
D7 ~ D0	I/O	Bidirectional 3-state data bus connected to the system data bus.
INT	O	A signal to indicate that the FDC is requesting service. This signal is output at every one byte in the NON DMA mode, and at the end of command operation in the DMA mode. This signal is connected to the IR6 terminal of the interrupt controller μPD8259 (12E).
RESET	I	The drive interface output which sets the FDC to the idle state and eliminates the WDATA output (indifinite). It also sets INT and DREQ outputs to low level. D7 ~ D0 are set to the input state. The same as the reset signal to the CPU is connected to this signal. The reset signal must be 1.68 μsec. minimum.
DREQ	O	A signal to request data transfer between FDC and memory in the DMA mode. This signal is connected to the DREQ1 terminal of the DMA controller μPD8237AC (21J).
$\overline{DACK}$	I	A signal to indicate that the DMA cycle is given. The function is the same as that of the $\overline{CS}$ signal in the DMA cycle. This signal is connected to the DACK1 terminal of the DMA controller μPD8237AC (21J). Receiving the above DREQ signal, the $\overline{DACK}$ signal is made active. DMA operation 
$\overline{WR}$ $\overline{RD}$	I	Write operation  Read operation 

Signal name	I/O	Function
A0	I	A signal to select the status register and data register in FDC to be accessed via the data bus. The status register is selected when this signal is "0", and the data register when it is "1". This signal is connected to the CPU address A0.
TC	I	A signal to indicate the end of read or write operation from the main system. This signal is supplied by the Q output of FFs LS73 (20H). The FFs is reset at the leading edge of the $\overline{DACK}$ signal. This TC pulse must be 120 ns minimum.

Table 4-14

► FDD Motor Contrl Circuit

The FDD motor control signal is supplied by the circuit shown in Fig. 4-34. The motor is started by specifying the I/O address 30H and making the $\overline{IOWR}$ signal active low.

The motor driving time depends upon the SQW signal supplied by RTC46818 (21B).

The FDD motor timer length is set in the low-order 4 bits of port OAH of RTC46818 assigned to the I/O address 3DH, and the motor driving time is set by turning on/off the square wave (SQW wave) output from bit 3 of port OBH. Namely, assuming that the data set in the low-order 4 bits of port OAH is n in decimal notation, the motor on time of $1/16 \times 2^n$ is set by two LS393 as shown in Fig. 4-34.

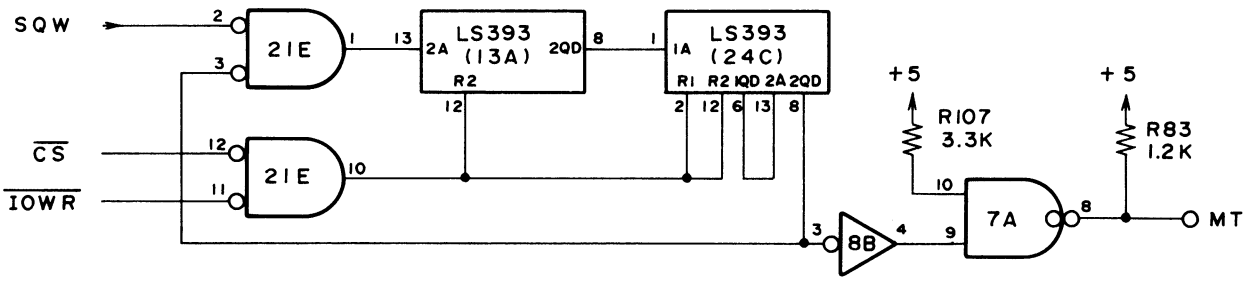


Fig. 4-34

4.16.5 Interface between Drive and FDC μPD765

The FDC μPD765 and FDD SD-321 are connected by the control signals shown in Table 4-15.

SD-321		Direction	μPD765	Function
4	HLD (Head Load)	←	HOLD	A signal to set the drive read/write head to the load state.
34	RDY(Ready)	→	RDY	A signal to indicate that the drive is in the ready state.
28	WPT (Write Protect)	→	WPRT	A signal to indicate when the write protect is set and the drive or media is inhibited from being written when the RW/SEEK signal specifies RW, and the two-side is set and the two-side media is inserted when the RW/SEEK signal specifies SEEK.
26	T0 (Track 00)	→	FLT/TRK0	A signal to indicate the FAULT state when the RW/SEEK signal specifies RW.
32	HDS (Side Select)	←	SIDE	A signal to select the head 0 (low level) and 1 (high level) of the two-side drive.
24	WG (Write gate)	←	WE	A signal to specify writing to the drive.
22	WD (Write data)	←	WD	Data to be written into the drive.
20	STP (Step)	←	FLTR/STEP	This signal works as a reset signal of the fault state held by the drive when the RW/SEEK signal specifies RW, and as a step signal of seek when the RW/SEEK signal specifies SEEK.
	↑↓	←	RW/SEEK	0: RW (Read/Write mode) 1: SEEK (Seek mode)
18	DIR	←	LCT/DIR	This signal indicates that the drive read/write head selects more than 43 cyclinders, when the RW/SEEK signal specifies RW. It specifies the seek direction when the RW/SEEK signal specifies SEEK. 0: Centrifugal direction 1: Centripetal direction
8	INDX (Index)	→	INDX	A signal to indicate the physical start point of the track on the media.
10	US0	←	US0 0	A signal to select FDD NO. to be drived.
			US1 0	
12	US1		US0 1	
			US1 0	
14	US2		US0 0	
			US1 1	
6	US3		US0 1	
			US1 1	

Table 4-15

The timing of these control signals for the FDD SD-321 is shown in Fig. 4-35.

(a) Seek operation

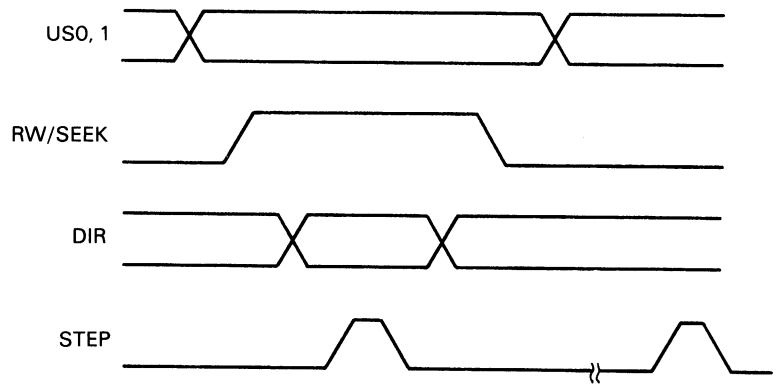


Fig. 4-35

4.16.6 VFO

► Circuitry of the VFO

The VFO is the "data window" generator which provides read data with sufficient margins. (See Fig. 4-36.)

The VFO is synchronized with the pulse train of the sync field where data "00" of the disk format is written, to obtain an accurate data window. (See Fig. 4-37.)

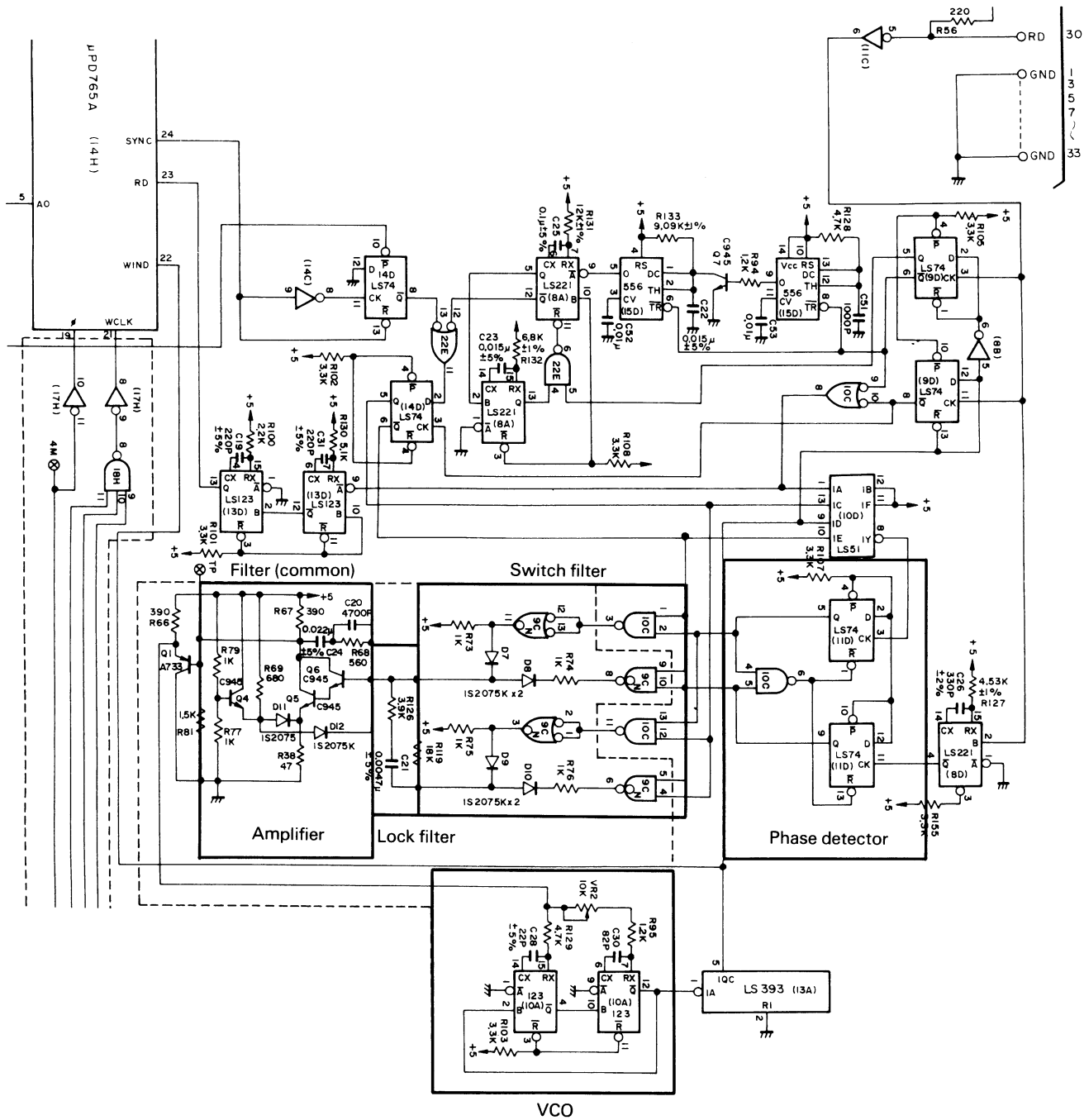


Fig. 4-36

Once synchronization is established, the VFO operates only to follow variation of bit phase resulting from variation of disk rotation speed but ignores bit phase variation due to shift of individual peaks. The operating principles of the VFO are explained below.

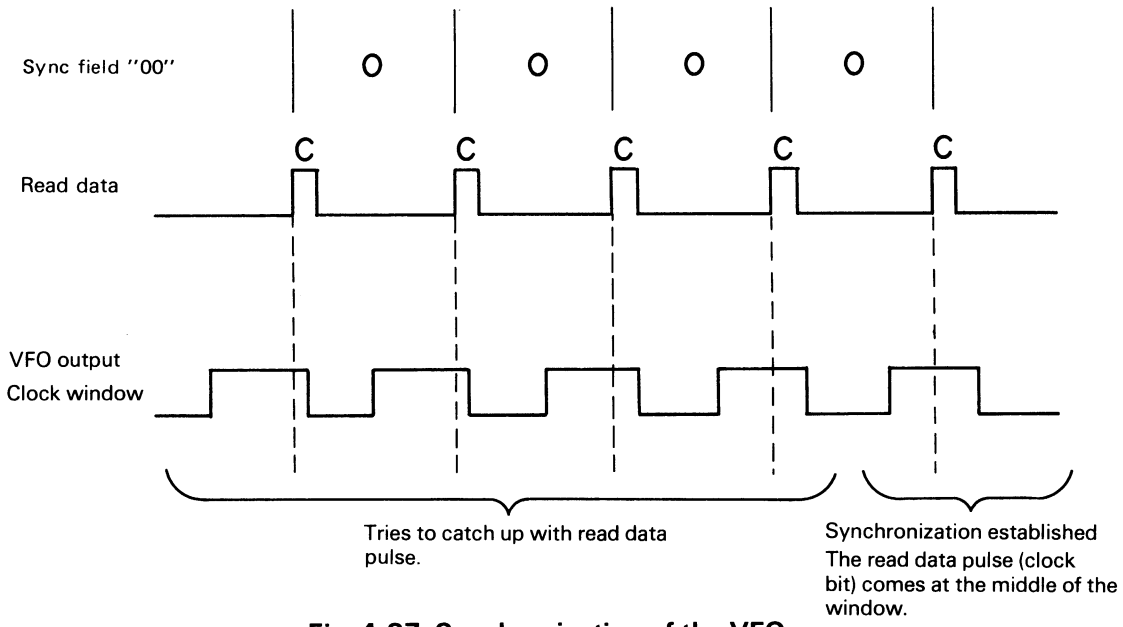


Fig. 4-37 Synchronization of the VFO

► Operation of the VFO

(1) Before establishment of synchronization

D flip-flop LS74(11D) detects phase difference of read data which is applied via one-shot LS221(8D) to pin 11 (clock input) and Clock window applied to pin 3 (clock input).

The output of flip-flop (11D) is the sync field, which is as shown in Fig. 4-40 depending on phase difference of clock inputs.

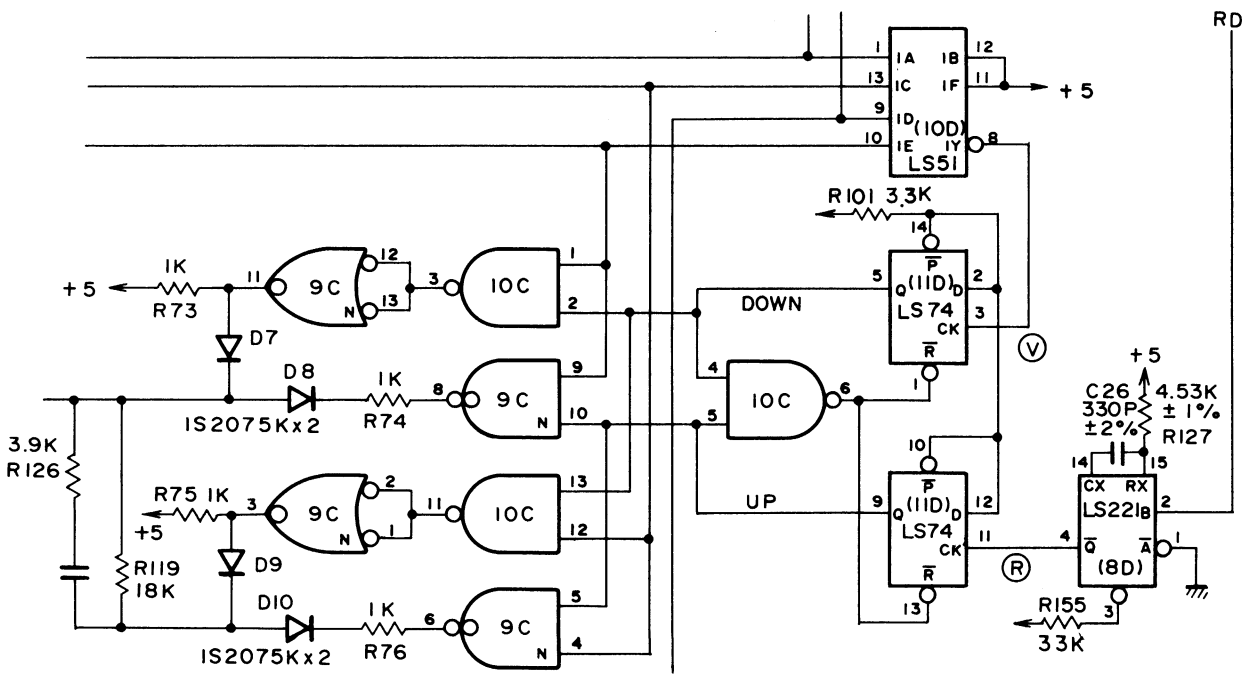


Fig. 4-38 Phase difference detector

Fig. 4-40 (a) shows the case when Clock Windows come later than clock bits of the sync field. Signal UP is High level at this time and the amplifier input is as shown in Fig. 4-40 (a) so that the frequency of the VCO becomes higher.
Fig. 4-40 (a) shows the case when Clock Windows come earlier than the clock bits of the sync field. Signal DOWN is H level in this case and the amplifier input is as shown in Fig. 4-40 (b) so that the frequency of the VCO becomes lower.
Fig. 4-40 (c) shows the case when Clock Windows are synchronized with the clock bits of the sync field. At this time, each bit of read data rises at the middle of Clock Window.

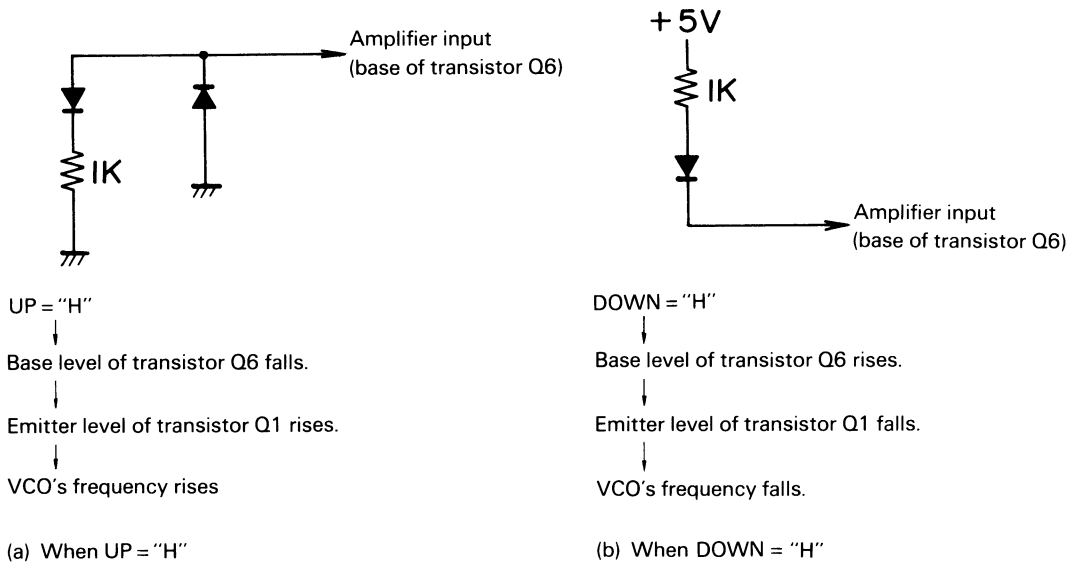


Fig. 4-39 Variations of amplifier input

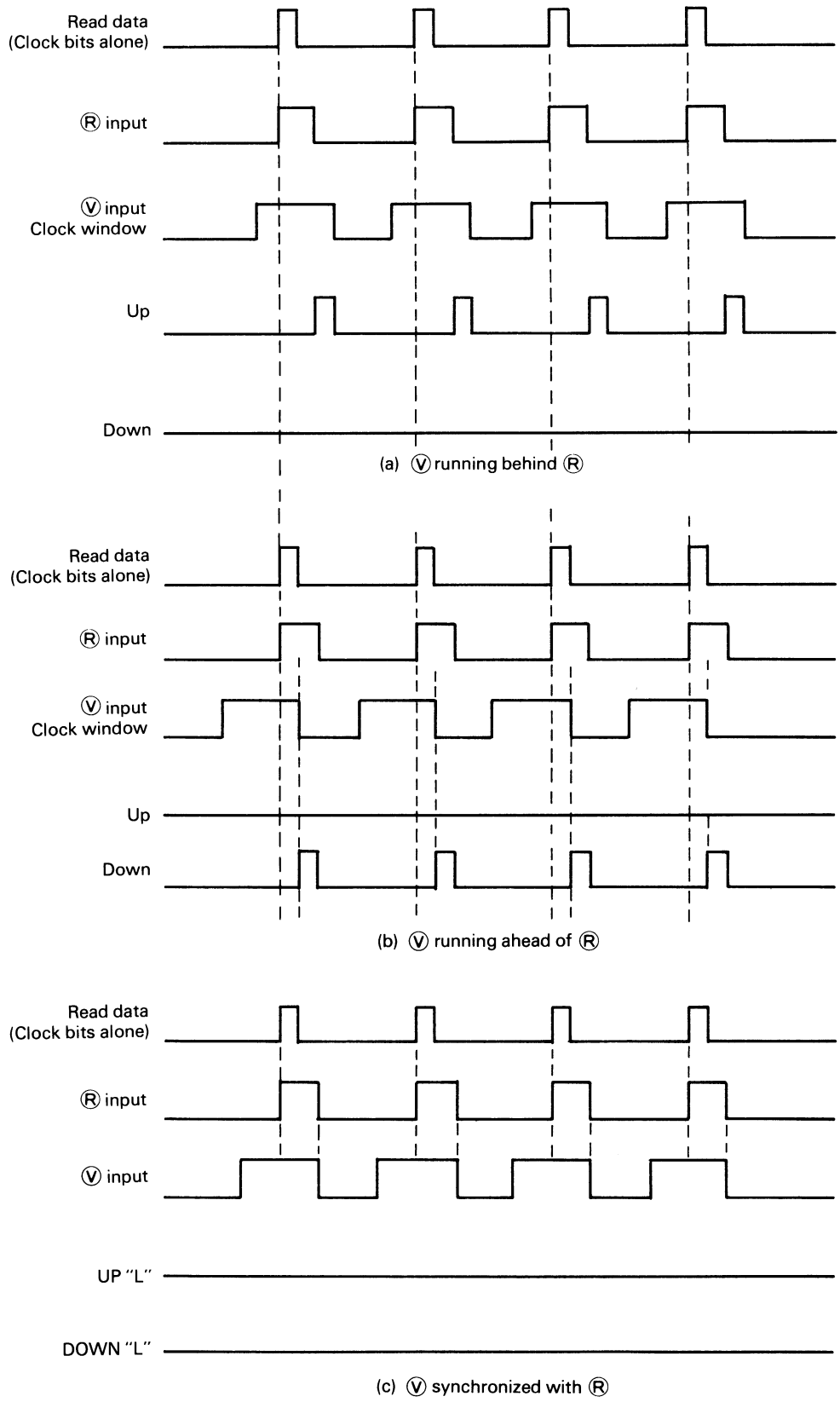


Fig. 4-40 Operation of the VFO in the sync field

(1) After establishment of synchronization

Fig.4-41 shows how the VFO operates after establishment of synchronization. Input (V) is a pulse train each bit of which rises at the rise of read data and decays at the rise or decay of Clock Window.

Since peaks of read data shift in the direction shown by the arrow, signals UP and DOWN remain at high level for the durations corresponding to the peak shifts even when Clock Window is properly timed. These signals, however, scarcely affect Clock Window because they are fed back to the oscillator via the lock filter composed of R119, R126, and C21 (see Fig. 4-36).

Thus, once synchronization has been established, the VFO operates to follow only slow phase changes due to changes of disk rotation speed, etc. but does not respond to rapid phase changes due to peak shift.

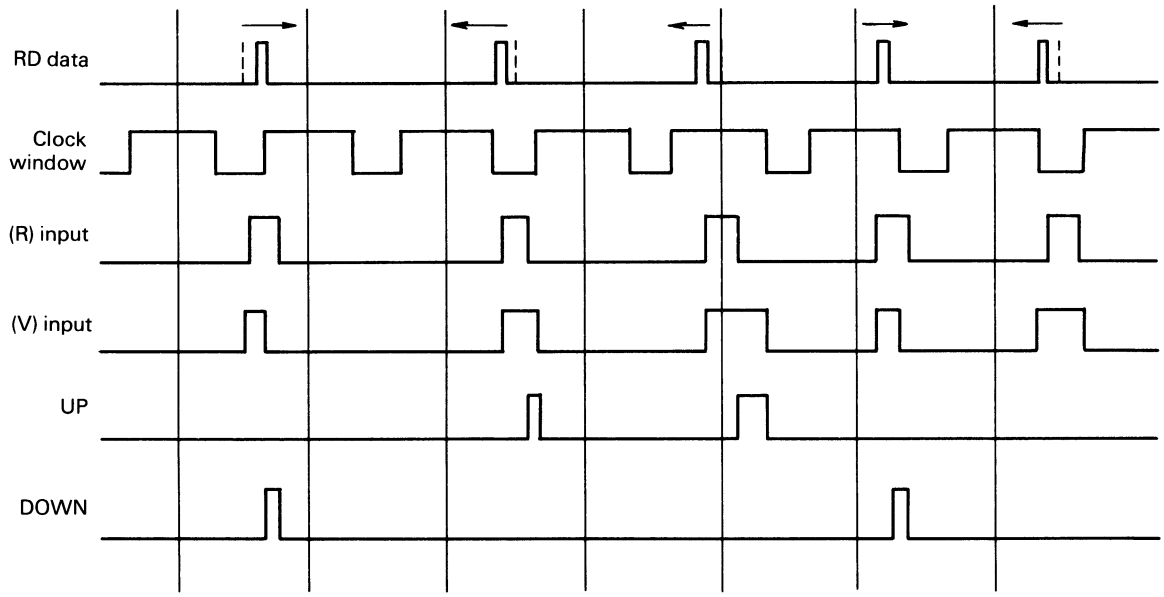


Fig. 4-41 Operation of the synchronized VFO in the data field

4.17 HD146818P (Real Time Clock Plus RAM)

► **Functions**

The QX-10 uses RTC (Real Time Clock Plus RAM) HD146818P to provide the following functions.

1) Clock function

The RTC updates the time and calendar RAM at the rate of once per second, and displays the time.

2) Static C-MOS RAM

A 50-byte general purpose RAM is provided. Since the RTC is backed up by the battery, the data needed to be held in the system can be stored in this RAM.

3) Generating square wave

The RTC is provided with an internal frequency divider, which generates a square wave at the SQW terminal. The wave frequency can be selected by the program.

4) Three independent interrupts

(a) Periodic interrupt

An interrupt request can be generated at the rate of once per 30μs ~ 500ms.

(b) Alarm interrupt

An interrupt request can be generated when the time set for alarm (second, minute and hour) coincides with the timing.

(c) Update ended interrupt

An interrupt request can be generated each time the time is updated.

Terminal name	I/O	Function
OSC1	I	Supplies an external pulse of 32.768 kHz. The OSC2 terminal should be set to the open state when the clock is supplied.
CKFS (Clock Out Frequency Select)	I	This terminal is an input signal to specify the CKOUT output signal dividing rate, but connected to GND as the CKOUT terminal is used.
AD0 ~ AD7	I/O	Bidirectional bus used for address information transfer or data input/output as the processor accesses the RTC. It is used for address information transfer in the first half of the cycle, and for data transfer in the latter half. The address information must be defined at the trailing edge of the M-signal. The RTC uses AD0 ~ AD5 for the address information. The data must be defined in the latter half of the cycle. The data bus driver is a three-state output buffer, which is set at the high impedance state except when the RTC outputs data.
M (Multiplexed Address Strobe)	I	A strobe signal to take in the address information from the address bus. It is composed of the write signal ($\overline{\text{IOWR}}$) to 46818 and RTC system chip select signal ($\overline{\text{CSCLK}}$). The address information is taken into the RTC at the trailing edge of this signal.
$\overline{\text{G}}$ (Data Strobe)	I	The logical products of $\overline{\text{IORD}}$ signal and chip select signal ($\overline{\text{CSCLK}}$) is input. When the CPU writes the data, the data is input at trailing edge.
$\overline{\text{W}}$ (Read/Write)	I	When CPU reads the RTC, this signal holds high. When CPU writes the RTC data, this signal becomes low.
$\overline{\text{CS}}$ (Chip Select)	I	This signal is the reverse logic of reset signal. It is low level except under reset.
$\overline{\text{IRQ}}$ (Interrupt Request)	0	A signal to request the CPU to make an interrupt. Pulled up to +5V and active low level.
$\overline{\text{RES}}$ (Reset)	I	Supplied by the power on reset signal. The RTC is reset by this signal, but the functions of the clock calendar RAM are not influenced.
PS (Power Sense)	I	Supplied from the address line A7. After initializing the RTC contents, the CPU sets this bit to "1" to prepare for power down or other power failure.

Table 4-16

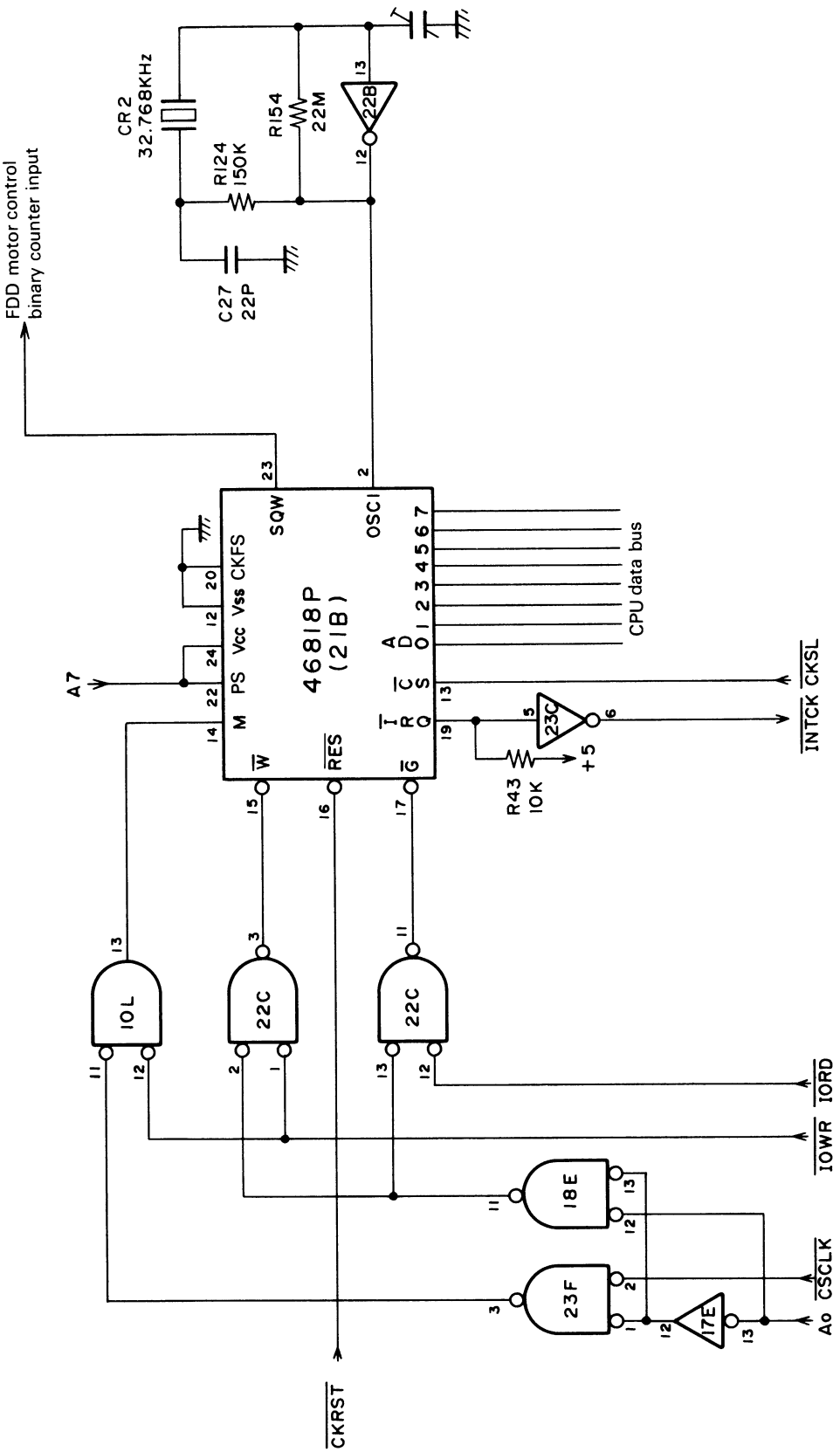


Fig. 4-42 Real time clock plus RAM 46818

4.18 DMA Controller μPD8237AC

The programmable DMA controller μPD8237 with four independent channels as shown in Fig. 4-43 is used.

Two DMA controllers are connected in two-stage cascade to provide seven channels. In this case, the μPD8237 (21J) works as a master and the μPD8237 (19J) as a slave.

HRQ and HLA signals of the slave DMA controller are connected to the 4th channel of the master controller.

Channel 0 is given the highest priority. The priority in this circuit is as shown in Table 4-17.

When the service of one channel is accepted, the service of the other channels can not be accepted until the service of that channel is completed.

Channel		Connection	
Master	1	Floppy disk	High
	2	Monitor	
	3	Option slots (One of OP # 1 through OP # 5)	
			Priority
Slave	1	Option slots (OP # 1)	
	2	Option slots (OP # 2)	
	3	Option slots (OP # 3)	
	4	Option slots (OP # 4)	Low

Table 4-17

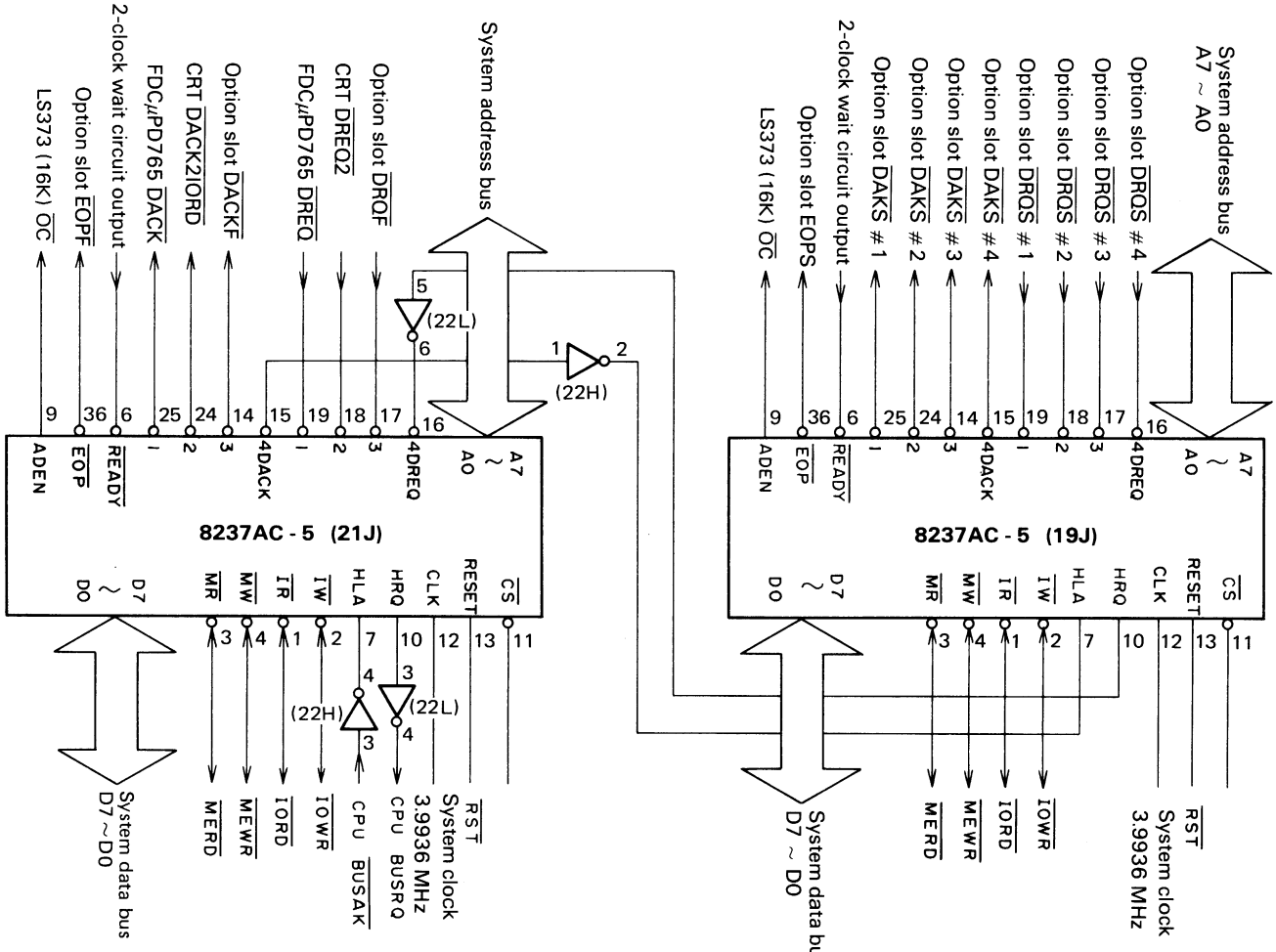


Fig. 4-43 DMA controller μPD8237

4.18.1 DMA Controller $\overline{CS}$ Signal Supply Circuit

The CS (Chip Select) signal of two DMA controllers μPD8237 (IC19J and IC21J) is supplied as shown in Fig. 4-44.

When either of these two DMA controllers is selected, the bus line must be used only by the CPU and use by the other devices is inhibited. So the $\overline{BUSAK}$ signal output from the CPU and supplied to the gate to provide the $\overline{CS}$ signal must be at high level. The address lines A7, A6 and A4 are used to supply the $\overline{CS}$ signal.

Therefore, DMA controllers are selected when A7 is 0 and A6 is 1.

Address line	A7	A6	A5	A4	A3	A2	A1	A0	I/O address
8237 (21J) $\overline{CS}$	0	1	0	0	×	×	×	×	40 ~ 4FH
8237 (19J) $\overline{CS}$	0	1	0	1	×	×	×	×	50 ~ 5FH

Table 4-18

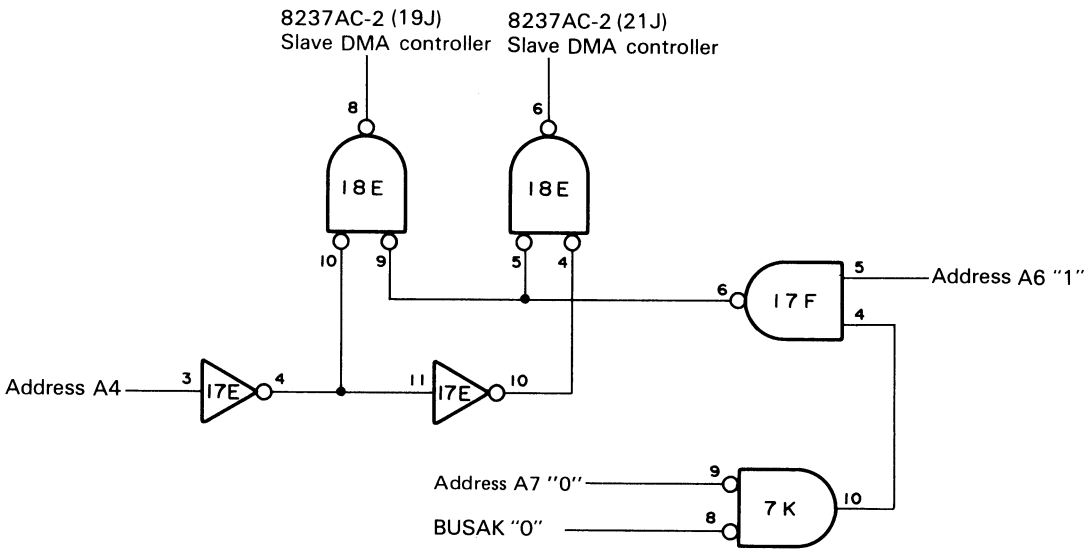


Fig. 4-44 Controller $\overline{CS}$ Signal Supply Circuit

4.18.2 Circuit to Supply DRQ Signal from CRT Drive Circuit

DMA transfer of the GDC is valid only during the CRT display period. If the DRQ is output from the Q10GMS board at the end of the display period as shown in the Fig. 4-45, the $\overline{DRQ}$ signal duration is ensured by the circuit shown in Fig. 4-46 to make DMA transfer valid until the $\overline{DACK}$ signal is output from the DMA controller μPD8237.

The timing chart is shown in Fig. 4-47.

When the high level $\overline{DRQ}$ signal from the Q10GMS board is applied to the D-type flip-flop LS74 (24M), a low level signal is generated at the $\overline{Q}$-terminal and sent to the DMA controller μPD8237 (21J). The Q-terminal is then set to high level. The signal goes through the OR gate IC20L and re-enters LS74 (24M) as its D-input.

Therefore, even if the $\overline{DRQ}$ signal is set to low level, the D-input signal is held and the $\overline{DREQ}$ signal to the μPD8237 is held at low level.

Receiving the $\overline{DRQ}$ signal, the μPD8237 transfers HRQ and HLA signals with the $\overline{DRQ}$ and then outputs the active low $\overline{DACK}$ signal. The $\overline{DACK}$ signal resets LS74 (24M), and the $\overline{DREQ}$ signal is released as a result.

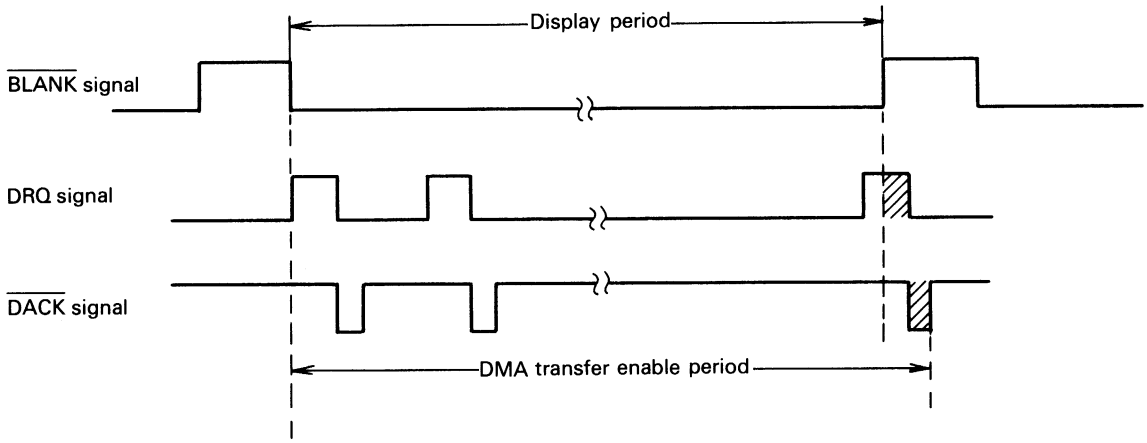


Fig. 4-45

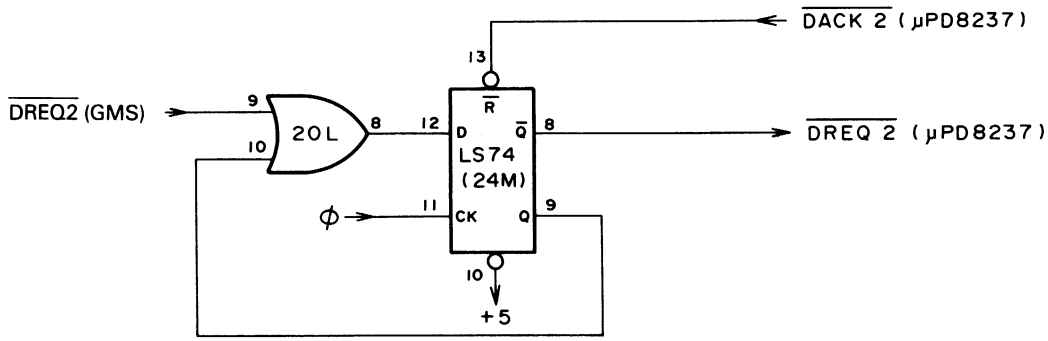


Fig. 4-46 Circuit to supply $\overline{\text{DRQ}}$ signal from CRT display circuit

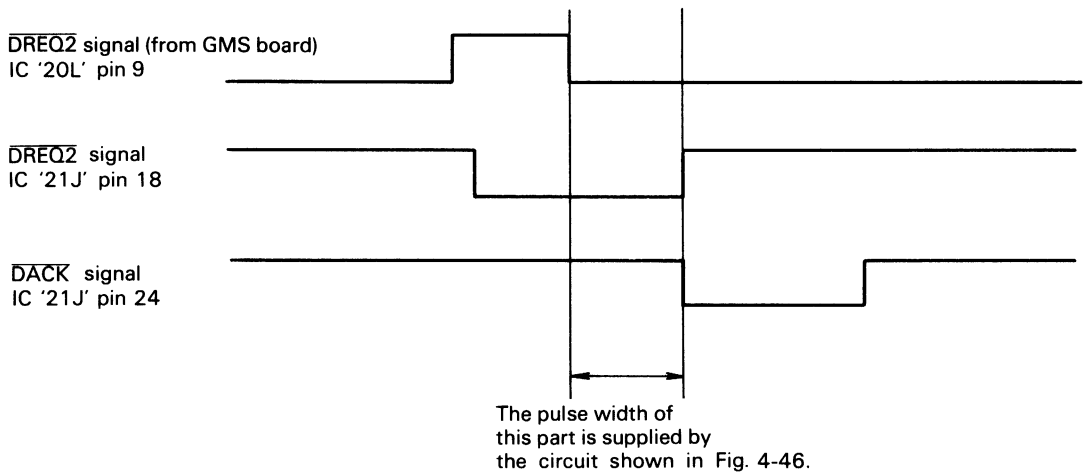


Fig. 4-47

4.18.3 DMA Transfer from Option Card

In the case of DMA transfer by connecting a low-speed memory and I/O device using an option card, the data may not be defined because the pulses of $\overline{IOW}$ and $\overline{IOR}$ signals of the μPD8237 are too short. It is necessary to wait definition of data input/output by effecting WAIT to $\overline{IOW/IOR}$ cycle by making the ready signal terminals of the μPD8237 active at $\overline{IOW/IOR}$.

The circuit shown in Fig. 4-48 is used for this purpose.

WAIT is effected by holding the $\overline{IOW/IOR}$ signal for a duration equivalent to three clocks from its active time.

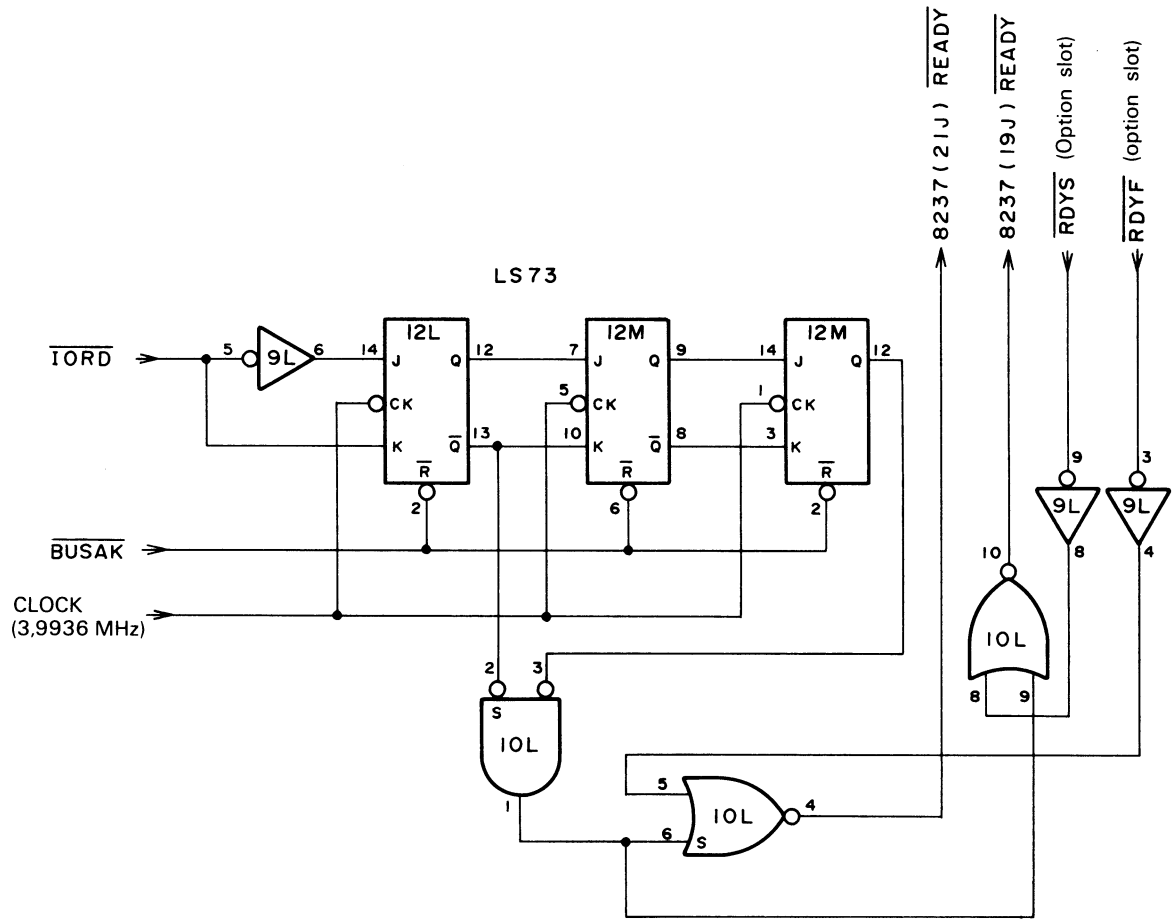


Fig. 4-48 Circuit to supply READY signal at DMA transfer from option card

4.18.4 DMA Transfer

The operation sequence of the μPD8237 for DMA transfer is described using the timing chart of Fig. 4-49.

(1) A DMA transfer request ($\overline{DREQ}$) signal from an external I/O device is applied to the μPD8237.

(2) The μPD8237 judges the priority of the $\overline{DREQ}$ signal, and supplies the active high HRQ signal to the $\overline{BUSRQ}$ signal input of the CPU through the inverter.

(3) Receiving the $\overline{BUSRQ}$ signal, the CPU sets the three-state address and data bus to the high impedance state, outputs the $\overline{BUSAK}$ signal and supplies and active high signal to the HLA signal terminal of the μPD8237 through the inverter.

(4) The μPD8237 outputs the ADEN (Address Enable) signal in order to output the memory address of the data to be sent in DMA transfer, and makes the OUTPUT CONTROL terminal of the external latch LS373 (16K) active.

(5) The μPD8237 makes the ADSTB (Address Strobe) signal and the ENABLE terminal of the external latch LS373 (16K) active, and sends the high-order eight bits of the address to be output to the data buses DB0 ~ DB7 to the system address buses A8 ~ A15.

(6) The address buses A0 ~ A7 are simultaneously output from the μPD8237 to define the address. The μPD8237 outputs the $\overline{DACK}$ signal to permit DMA transfer as an active signal to the I/O device which made the DMA transfer request.

(7) The μPD8237 outputs the $\overline{IOR}$ signal and accesses the data from the peripheral circuit, or outputs the $\overline{IOW}$ signal to load data into the peripheral circuit.

(8) DMA transfer can be terminated by the EOP (End of Process) signal.

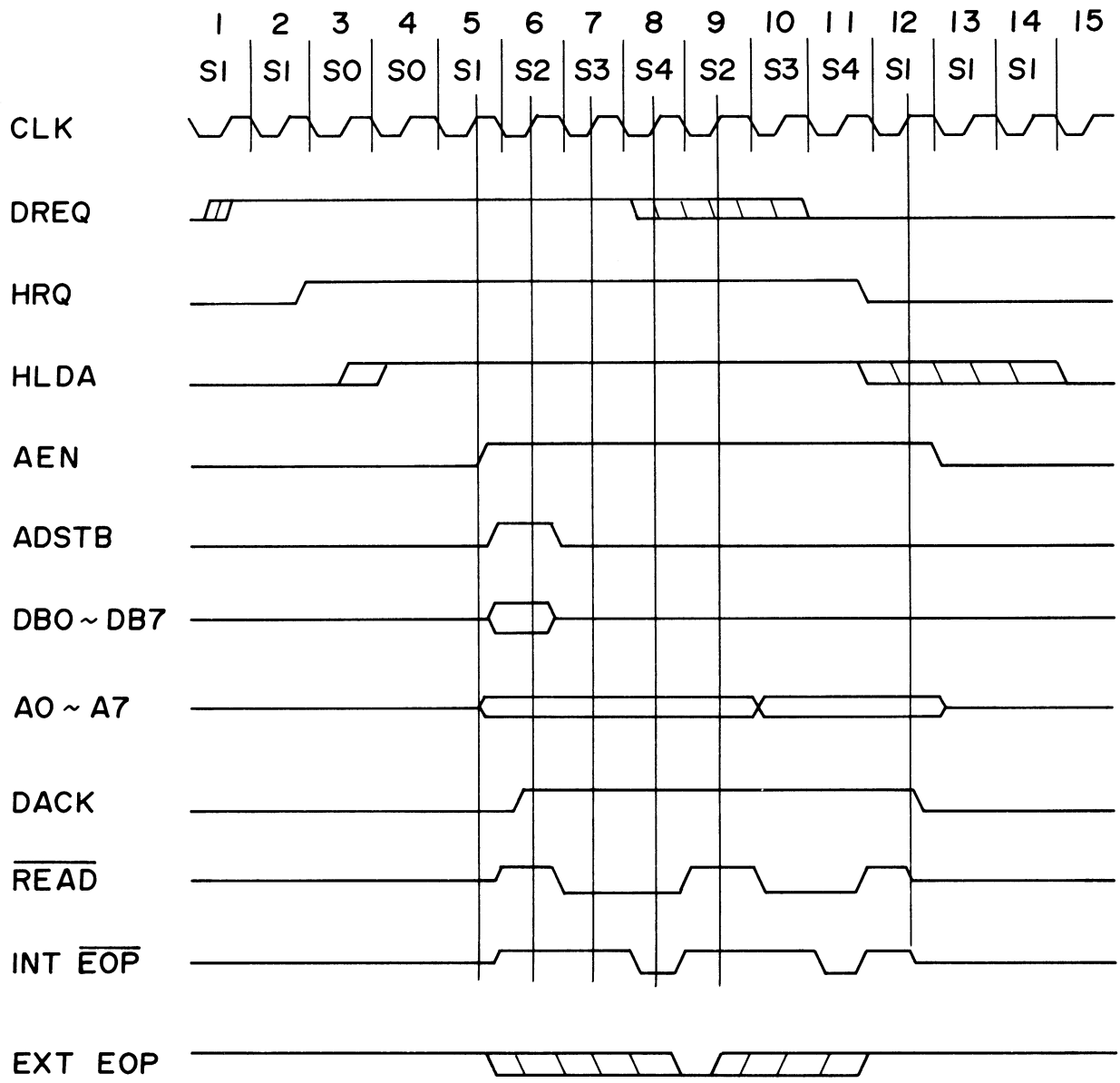


Fig. 4-49 Timing chart of DMA transfer

4.18.5 Memory-Memory Transfer

Memory-memory transfer is made as shown in the timing chart in Fig. 4-50.

(1) Output the memory address of the reading data onto the address bus. In this case, the high-order addresses A8 ~ A15 are once output onto the data buses DB0 ~ DB7 and transferred onto the address bus when the ADSTB signal is set to the high level.

(2) By making the $\overline{MEMR}$ signal active low, take out the data from the selected memory location and put it on the data bus and hold it in the temporary register provided in the μPD8237.

(3) The μPD8237 gives an address to the writing memory as in step (1).

(4) When the $\overline{MEMW}$ signal is made active low, the written data is output from the temporary register and stored in the memory.

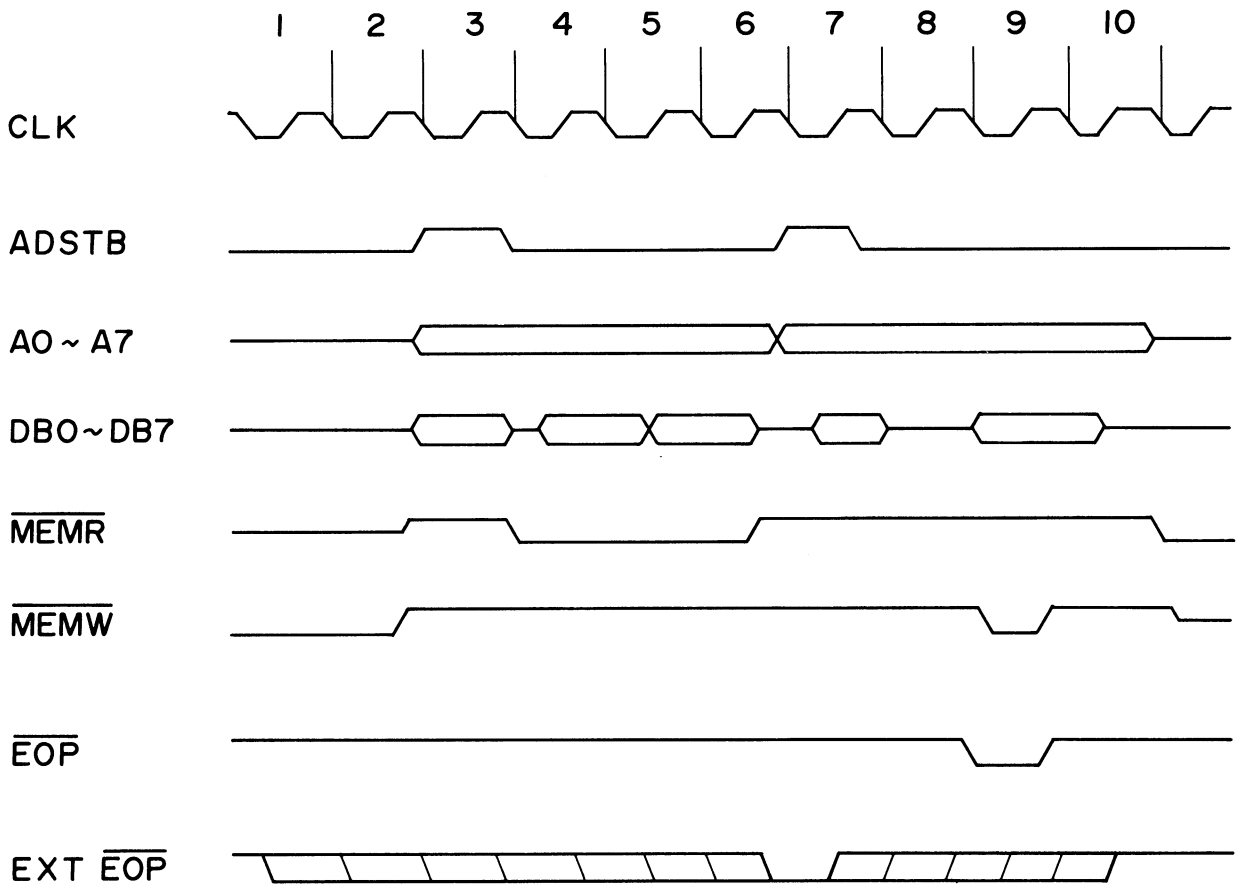


Fig. 4-50 Timing chart of memory-memory transfer

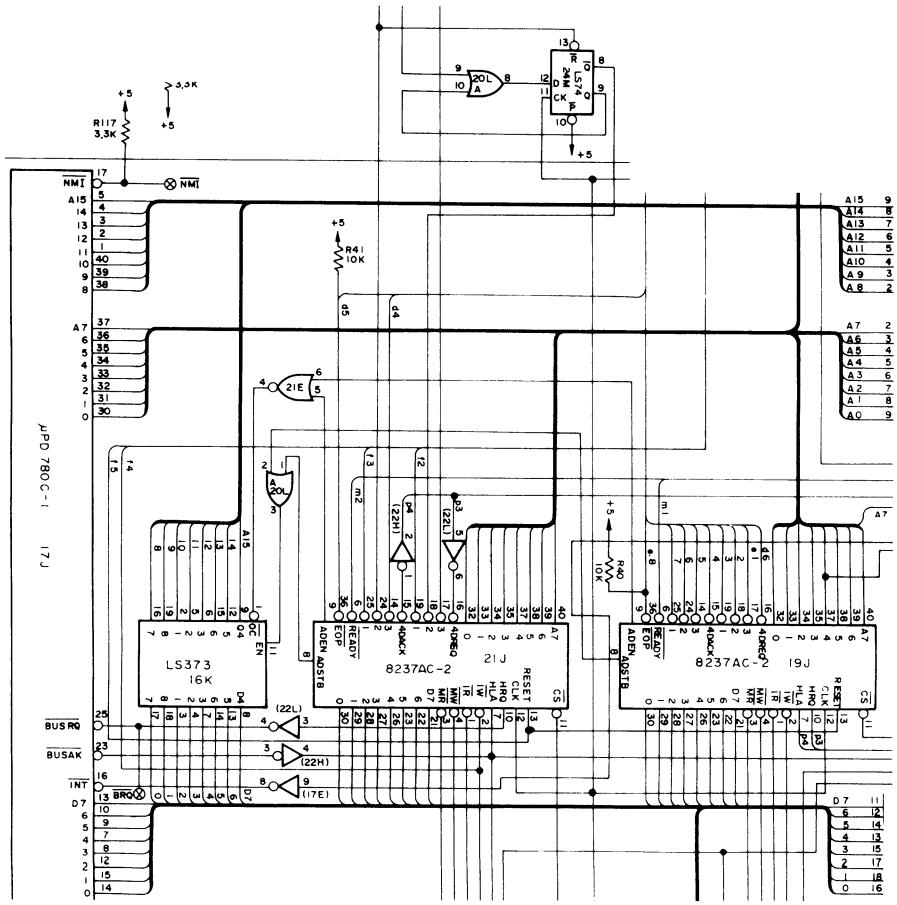


Fig. 4-51 DMA circuit

4.19 MEMORY CIRCUIT

4.19.1 Memory Address Map

The memory space comprises a resident RAM, a memory bank RAM, a P-ROM and a C-MOS RAM. Address allocation is as shown in Fig. 4-52 for power on, normal operation and use of C-MOS RAM.

- The resident RAM area is selectable in 4 KB, 8 KB, 16 KB, 30 KB and 32 KB by the jumper wire on the main circuit board.

The P-ROM can be selected in 2 KB, 4 KB and 8 KB.

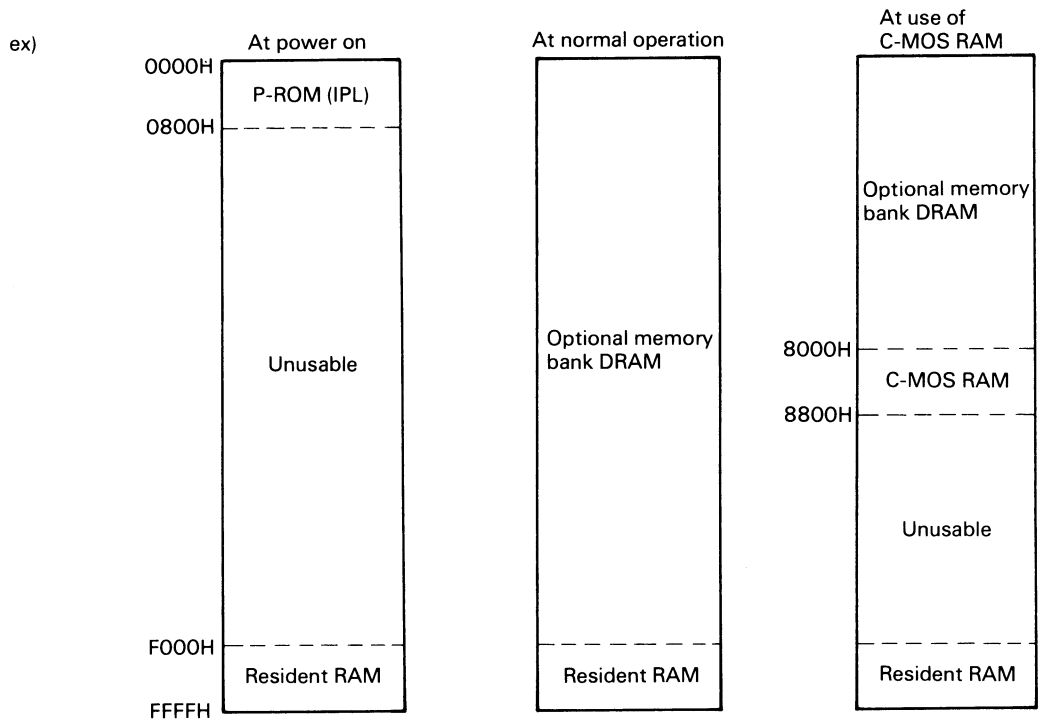


Fig. 4-52 Memory map

The resident RAM capacities of P-ROM and D-RAM are shown in Table 4-19 for each specification.

At power on, the CPU executes IPL (Intial Program Loader) stored in and after the address 0000H of P ROM, and allocates the addresses of the resident RAM area as shown in Fig. 4-53.

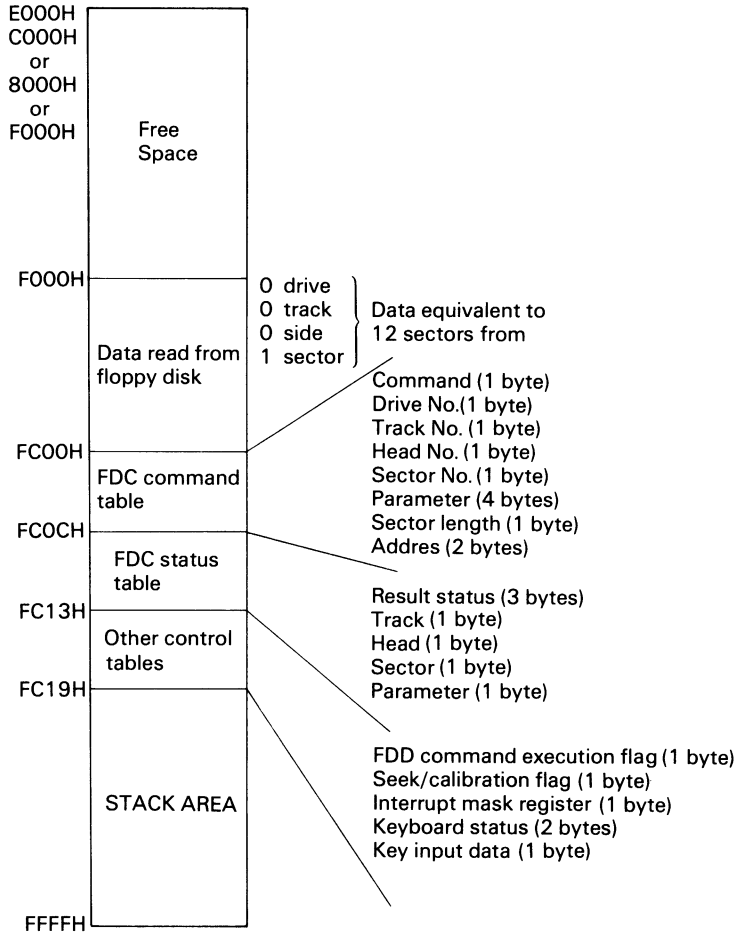


Fig. 4-53 Address Allocation of Resident RAM

	Model	QX-10 U.S.A. Specifications		QX-10 Europe Specifications		QC-10 Japan Specifications	
	Derivative version / Item	HASCI version	ASCII version	Standard version	Multifonts version	Standard version	Kanji version
ROM	IPL	U.S.A. specifications 2 KB 2716 × 1	←	Europe specifications 2 KB 2716 × 1	←	Japan specifications 2 KB 2716 × 1	←
	Character generator (for display)	U.S.A. specifications 4 KB 2732 × 1	←	Europe specifications 4 KB 2732 × 1	←	Japan specifications 4 KB 2732 × 1	←
RAM	For Video	128 KB 64KRAM × 16	32 KB 16KRAM × 8	32 KB 16KRAM × 16	←	32 KB 16KRAM × 16	←
	Main	256 KB 64KRAM × 32	64 KB 64KRAM × 8	64 KB 64KRAM × 8	192 KB* 64KRAM × 24	64 KB 64KRAM × 8	192 KB* 64KRAM × 24
	Resident RAM	8 KB	←	8 KB	←	8 KB	←

*: Increase memory stage

Table 4-19

4.19.2 Setting of Resident RAM Capacity

The resident RAM capacity is set by the jumper wire J4 of the circuit shown in Fig. 4-54. The jumper wires and address wires are connected as shown in Table 4-20.

The resident RAM capacity is set as shown in Table 4-21.

The setting of each resident RAM capacity is described here.

Address line	Jumper wire
A11 + A12 + A13 + A14	B
A12	C
A13	D
A14	E

Table 4-20

Setting of Resident RAM Capacity (By J4)	Resident RAM capacity
Without jumper	32 kB
E	16 kB
E, D	8 kB
E, D, C	4 kB
B	All of the back of C-MOS RAM area (30kB)

Table 4-21

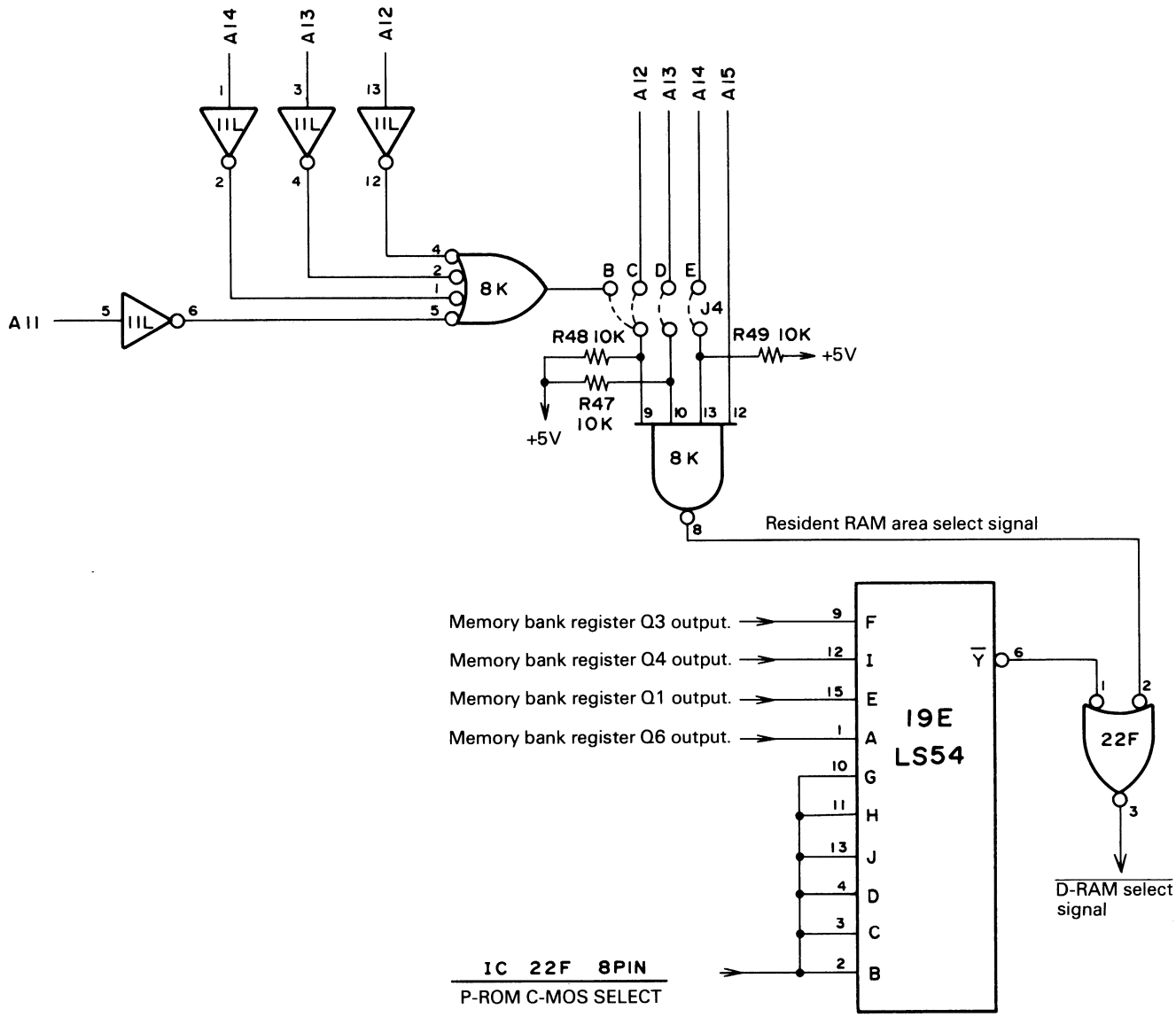


Fig. 4-54 Setting of Resident RAM Capacity (By J4)

(1) Setting the resident RAM capacity to 32 KB

When the resident RAM capacity is set to 32 KB, the resident RAM area is allocated to 8000H ~ FFFFH in the memory map as shown in Fig. 4-55. In this case, the jumper wire J4 is not used for connection.

Since only the most significant bit A15 of the address line is usually 1, when the addresses 8000H ~ FFFFH are specified, the output of pin 8 of IC8K is set to high level, and the outputs of pin 6 of IC21F and pin 3 of IC10K are set to high level in order to make the output of pin 3 of IC21F low level.

Finally, to make the $\overline{CS1}$ terminal of the C-MOS RAM μPD449, the C-MOS RAM set in the addresses 8000H ~ 87FFH is not selected and the resident RAM area is set.

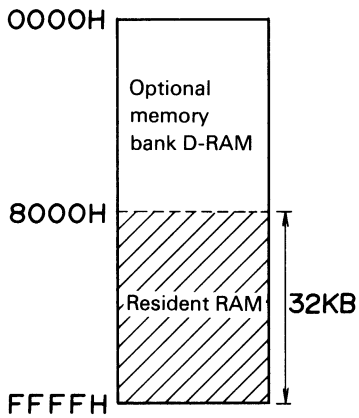


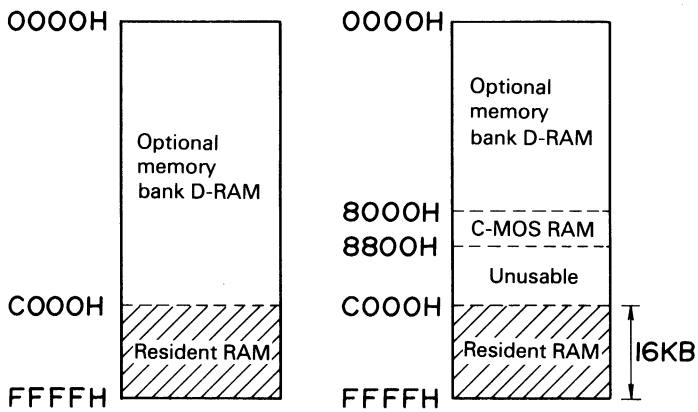
Fig. 4-55 Address map at setting resident RAM to 32 KB

(2) Setting the resident RAM capacity to 16 KB

When the resident RAM capacity is set to 16 KB, the resident RAM area is allocated to C000 ~ FFFFH in the memory map as shown in Fig. 4-56. When the C-MOS RAM is used, the C-MOS RAM area should be set to 2 KB in 8000 ~ 8800H.

Thus, only the E-terminal of the jumper wire J4 is used to set the resident RAM area and C-MOS RAM area as above described.

That is, when the resident RAM area is specified, the high-order two bits of the address lines A15 and A14 are usually "1", the input signals of pins 12 and 13 of IC8K are set to high level, and a low level signal is output from pin 8 and the C-MOS RAM is not selected.



(1) At normal operation (2) Use of C-MOS RAM

Fig. 4-56 Address map at setting resident RAM to 16 KB

On the other hand, when the C-MOS RAM area of 8000H ~ 87FFH is specified, the address line A14 becomes zero bit and the output of pin 8 of IC8K is set to high level.

All the inputs of IC21F are set to high level, and a low level signal is supplied from pin 3 of IC10K of the next stage, and the $\overline{CS1}$ terminal of the C-MOS RAM μPD449 (16M) is made active, providing the condition to select the C-MOS RAM.

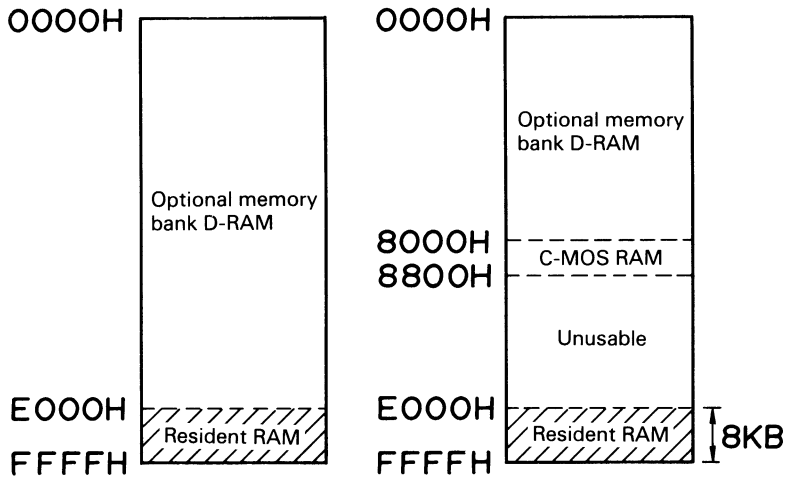
(3) Setting the resident RAM cpacity to 8 KB

The resident RAM area is allocated to 8 KB, E000H ~ FFFFH on the memory map. In this case, D and E terminals of the jumper wire J4 should be connected.

When the resident RAM area is specified, the high-order three bits of the address lines A15, A14 and A13 are usually "1", the output of pin 8 of IC8K is set to low level and the C-MOS RAM is not selected.

When the C-MOS RAM area is specified, only the bit the address A15 is set to "1", and A14 and A13 are "0".

The output of pin 8 of IC8K is set to high level making the CS1 terminal of the C-MOS RAM μPD449 (16M) active and enabling setting of the C-MOS RAM area.



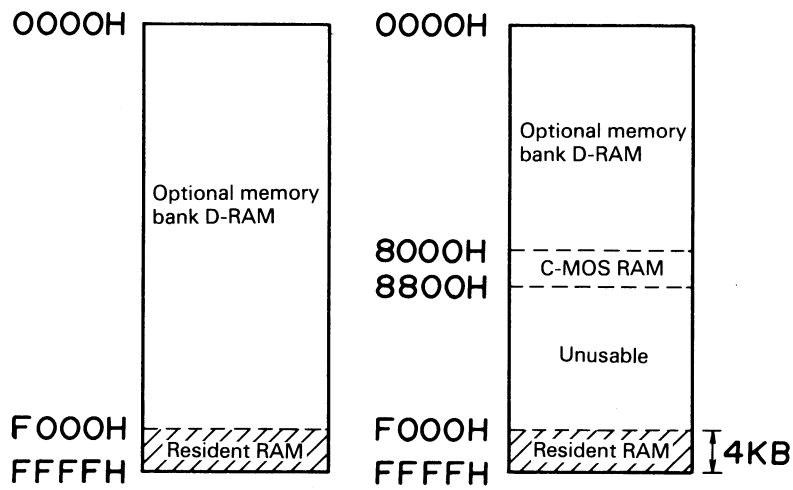
(1) At normal operation **(2) Use of C-MOS RAM**

Fig. 4-57 Address Map at Setting Resident RAM to 8 KB

(4) Setting the resident RAM capacity to 4 KB

The resident RAM are is allocated to 4 KB, F000 ~ FFFFH on the memory map. One of C, D and E terminals of the jumper wire J4 should be connected. As in the case of (3), when the resident RAM area address is specified, all the input bits of IC8K are set to "1", and the output of pin 8 is set to low level and the C-MOS RAM is not selected.

When the C-MOS RAM area is specified, all the signals except for the address line A15 are set to low level, and the output of pin 8 of IC8K is set to high level, making the $\overline{CS1}$ terminal of the C-MOS RAM μPD449 (16M) low level and enabling selection of the C-MOS RAM.



(1) At normal operation **(2) Use of C-MOS RAM**

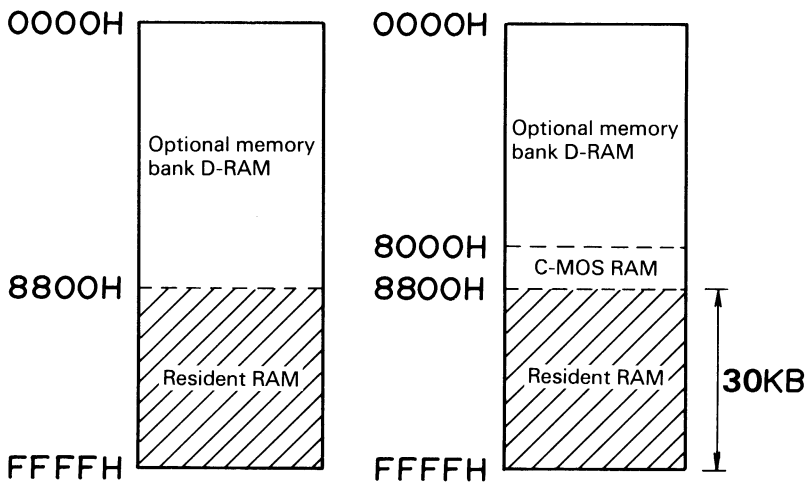
Fig. 4-58 Address Map at Setting Resident RAM to 4 KB

(5) Setting all memory areas after C-MOS RAM area to the resident RAM area

By connecting the B-terminal only of the jumper wire J4, set the C-MOS RAM area and resident RAM area to 8000H ~ 87FFH and 8800H ~ FFFFH respectively on the memory map.

The OR output of four address lines A11 ~ A14 is connected to the B-terminal of the jumper wire J4.

That is, when the addresses 8000H ~ 87FFH are specified, the output of pin 6 of IC8K is usually set to low level, and the output of pin 8 of IC8K is set to high level, making the C-MOS RAM μPD449 (16M) low level, and the C-MOS RAM is selected.



(1) At normal operation **(2) Use of C-MOS RAM**

Fig. 4-59 Setting All Memory Areas after C-MOS RAM Area to Resident RAM Area

When the addresses 8800H ~ FFFFH are specified, the output of pin 6 of IC8K is usually set to high level, making the $\overline{CS1}$ terminal of the C-MOS μPD449 (16M) high level. So, 8800H ~ FFFFH can be ensured for the resident RAM area without selecting the C-MOS RAM.

4.19.3 P-ROM Select Signal Supply Circuit

The $\overline{CS}$ signal to select P ROM (14M) for IPL is supplied by the D-type flip-flop LS74 (22K) of the circuit shown in Fig. 4-60. When the power is turned on, the power on reset signal is applied to the reset terminals of pins 1 and 13. Receiving this signal, the $\overline{Q}$-output of pin 6 of the flip-flop is set to high level and the Q-output of pin 9 is set to low level, respectively.

The output of pin 6 of the NAND gate formed by IC21F is set to high level. This signal is applied to pin 1 of IC21F. Then, the AND of this signal, the input signal of pin 2 or D-RAM select signal (D-RAM is not selected and set to high level then) and the output signal of pin 6 of flip-flop LS74 (22K) is taken.

A low level signal is supplied from the output of pin 12 of IC21F to the P-ROM (14M), and the P-ROM is selected.

After IPL by selecting the P-ROM, the I/O address 1CH is specified and "1" is set to the least significant bit "D0" of the data line, thereby setting the $\overline{Q}$-output of pin 6 of flip-flop LS74 (22K) to the low level, and the $\overline{CS}$ signal to the P-ROM is set to high level and the memory map is transferred from the P-ROM area to the D-RAM area.

4.19.4 C-MOS RAM Select Signal Supply Circuit

The C-MOS RAM μPD449 (16M) which is used for writing the data such as a stack point at power down is selected by the CPU when the interrupt made by detection of PWD signal is received.

That is, receiving this interrupt, the CPU outputs the I/O address 20H to the low-order of the address bus in order to select the C-MOS RAM, and supplies a low level signal to pin 4 of IC23F, where the $\overline{IOWR}$ signal from the CPU is connected to the input of pin 5 of IC23F. The AND of these signals is supplied to pin 11 of flip-flop LS74 (22K).

The data line "D0" bit is connected to the D input terminal (pin 12) of this flip-flop. By setting "1" in this bit, a high level signal is output from the Q-output of pin 9 to the input of pin 5 of IC21F.

After supplying the I/O address to the C-MOS RAM, the CPU outputs the C-MOS RAM area 8000H ~ 87FFH onto the address line. At this time, the address line A15 is usually at high level and the input of pin 4 of IC21F connected with the address line A15 is also set to high level.

The input of pin 3 of IC21F is connected to the resident RAM select signal. Since this signal is set to high level when the C-MOS RAM area is specified, a low level signal is output from pin 6 of IC21F and a low level signal is supplied from pin 3 of IC10K. That is, the active low $\overline{CS1}$ signal of the C-MOS RAM μPD449 (16M) is supplied from this signal, and the C-MOS RAM is selected.

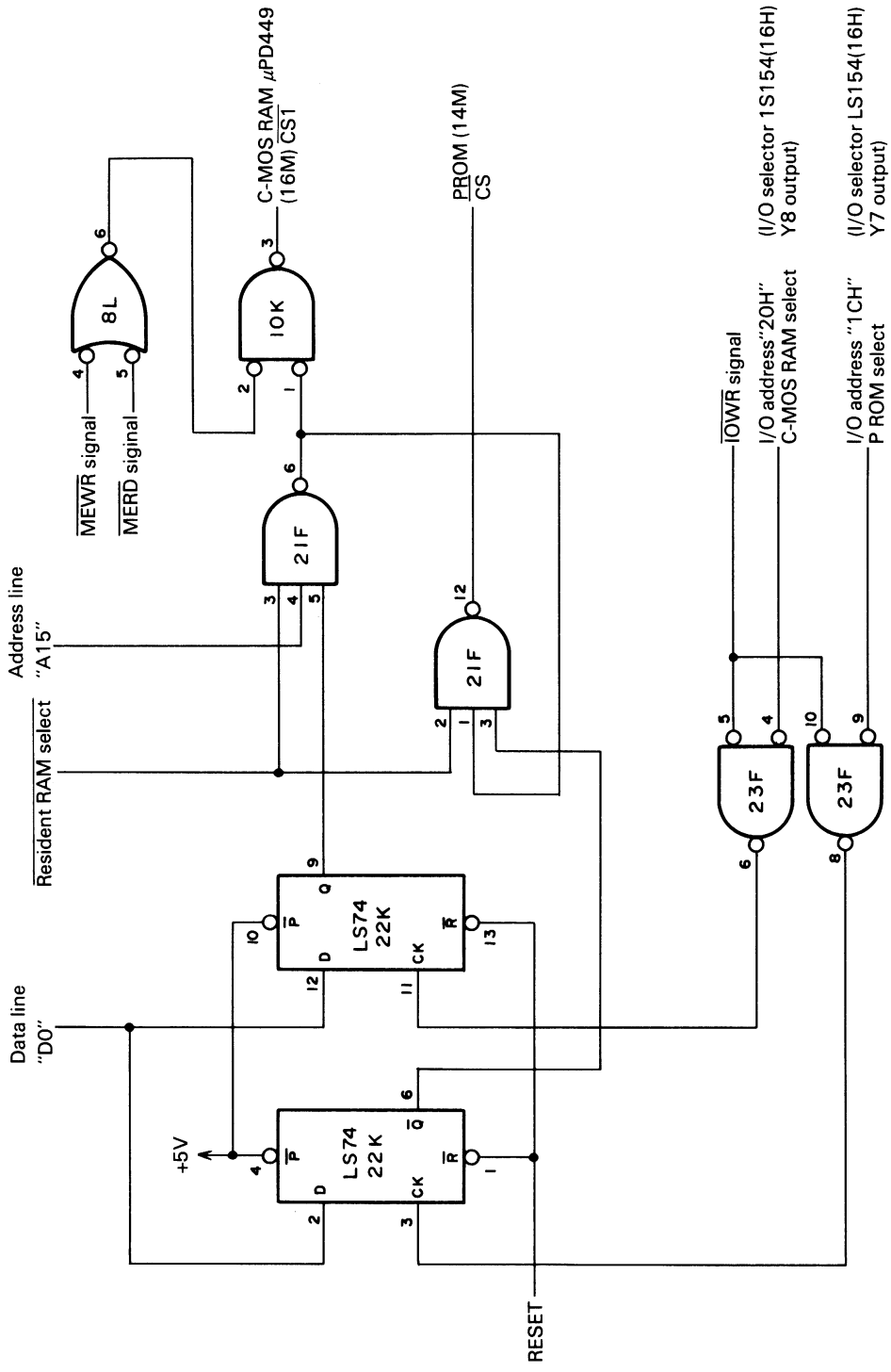


Fig. 4-60

4.19.5 D-RAM

The CPU (μPD780) can directly access a memory of 64 KB maximum through 16 address buses. The QX-10 has four memory banks (#0 ~ #3) and provides a memory capacity of 256 KB maximum by switching the memory bank register.

The memory bank configuration is shown in Fig. 4-61.

The memory bank #0 is usually selected by IPL after the power is turned on. The capacities of each memory bank can be selected by the jumper wire provided on the main board.

The relationship between the jumper wire connection and memory capacities is shown in Table 4-22.

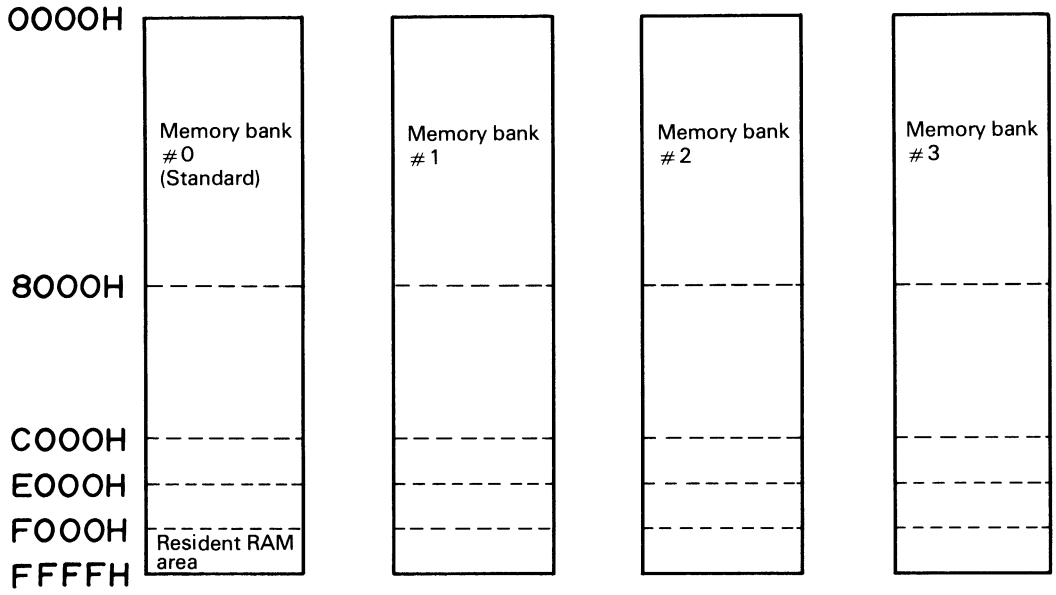


Fig. 4-61 Memory Banks

Jumper wire-connection	Memory Capacity
———	32KB
E	16
E, D	8
E, D, C	4
B	30

Table 4-22 Jumper Wire Connection and Memory Capacities

Memory banks #0 ~ #3 are selected by the memory bank register allocated to the I/O address 18H. The memory bank size depends on the resident RAM capacity. As the resident RAM area is increased, the memory bank capacity is decreased.

The D-RAM circuit configuration is described next.

4.19.6 D RAM Select Signal Supply Circuit

The D RAM select signal is supplied by the circuit shown in Fig. 4-62. LS74 (19E) comprises four internal AND gates, an OR gate to get the OR of the outputs of these gates, and an inverter. The memory bank register output is connected to the inputs of four AND gates.

An active low D-RAM disable signal is connected to the other inputs of these AND gates.

Therefore, when the memory bank is specified, the Y-output of LS54 (19E) is set to low level and the active low D-RAM select signal is supplied from the output of pin 3 of IC22H.

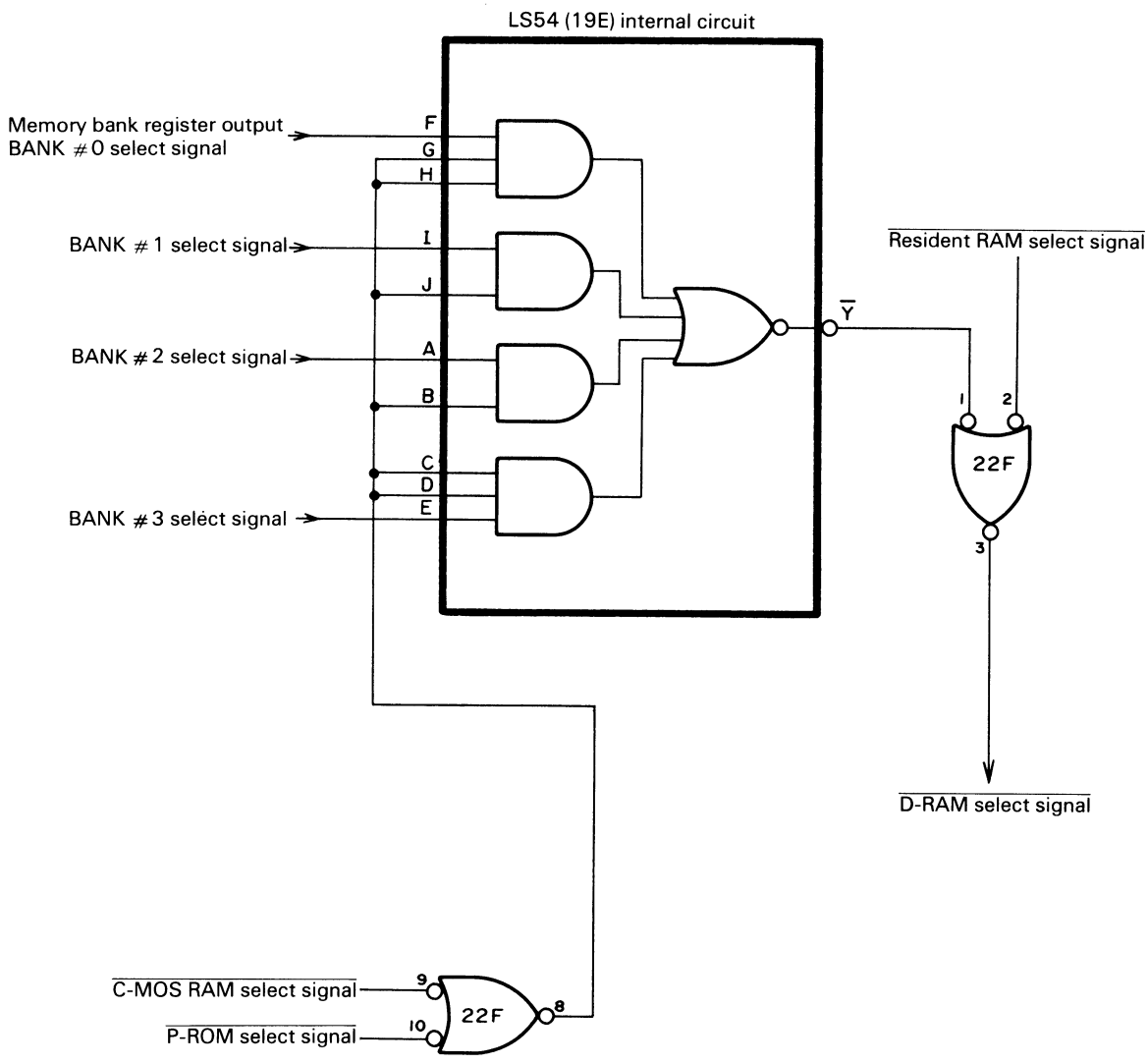


Fig. 4-62 D RAM Select Signal Supply Circuit

4.19.7 D-RAM Bank Selector

Since the CPU μPD780 has a16-bit address bus, it can access addresses of up to 64 KB at a time.

The QX-10 uses the 64K-bit dynamic RAM μPD4164-3 to ensure a large capacity, and has four banks with different specifications as shown in Table 4-19, enabling it to control a memory of 256 KB (64 KB x 4) maximum.

These memory banks are selected by the D-type FFs LS273 (18F) which is used as a memory bank register as shown in Fig. 4-63.

That is, this memory bank register is allocated to the I/O address 18H. An active low signal is output from the Y-6 terminal (pin 7) of the I/O selector LS154 (16H), and the OR of this signal and the $\overline{\text{IOWR}}$ signal from the CPU is taken by gate IC23F, and the output of this gate is used as a clock signal of the memory bank register LS273 (18F). The memory bank register is made active by this, and when it receives the bank select data input sent together with the I/O address 18H, it sets the bit of the bank to be selected in the output side.

As for the data corresponding to the I/O address 18H, since the memory bank register select signal is allocated to the high-order four bits out of eight bits and "1" is set in the bit corresponding to the memory bank to be selected, only one of Q1, Q3, Q4 and Q6 outputs must be a high level output even in the output side.

The memory bank select signal goes through the NAND gate of IC19F and OR gate formed by IC17F and IC18F, through which AND of this signal, RAS signal and PRI signal is taken.

One of these outputs supplies the $\overline{\text{RAS}}$ signal of one memory bank. Therefore, only the memory bank with the $\overline{\text{RAS}}$ supplied to it is selected as a direct access memory of the CPU.

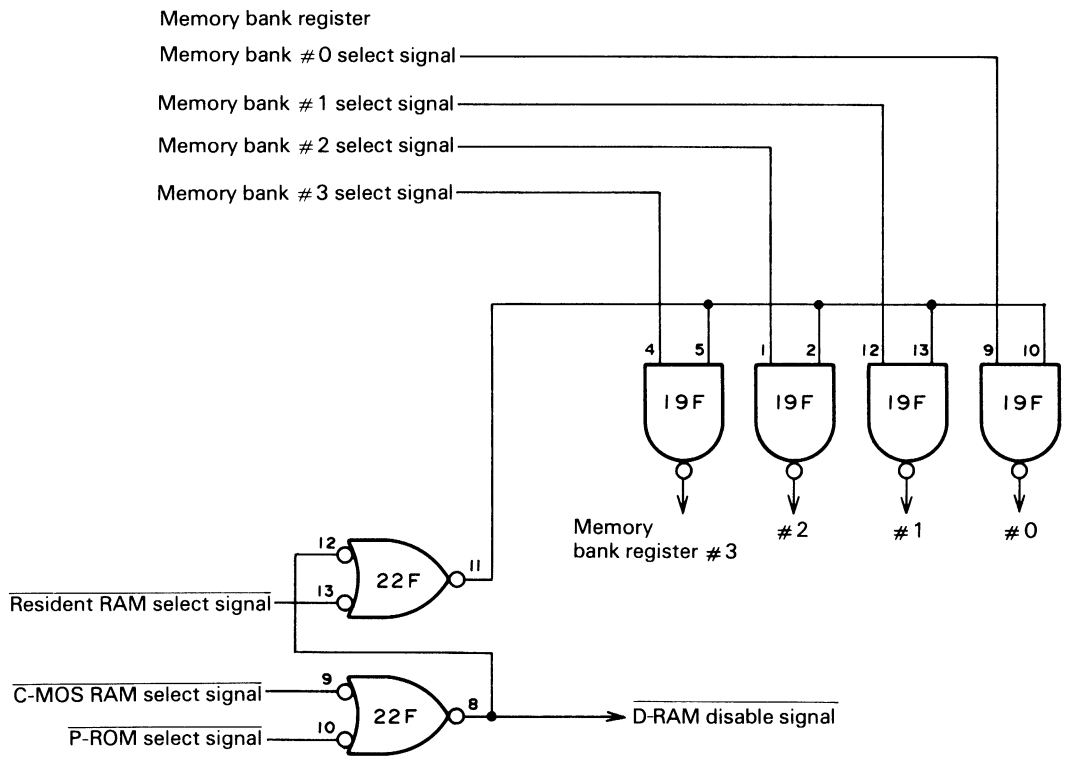


Fig. 4-63 Memory Bank Specify Gate Circuit

4.19.8 RAS Precharger

RAS and CAS signals are given to the D RAM at the timing shown in Fig. 4-64. In this case, the RAS signal is set to low level in the refresh cycle to refresh the D-RAM.

To define the trailing edge of the $\overline{RAS}$ signal in refreshing, it is necessary to fasten the leading edge of the $\overline{RAS}$ signal in OP code fetching to secure the pulse width shown in Fig. 4-64.

The two-stage flip-flop LS73 (20M) in the circuit shown in Fig. 4-65 is used for this purpose. It fastens the leading edge of the $\overline{RAS}$ signal to prolong the high level period of the signal double, about 0.14μsec.

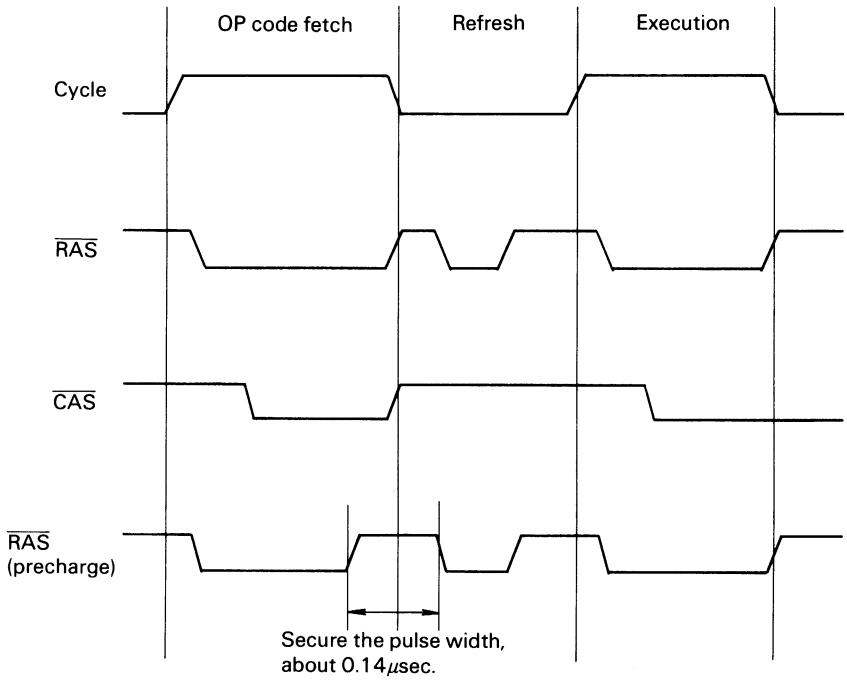


Fig. 4-64 D RAM RAS/CAS Signals Timing

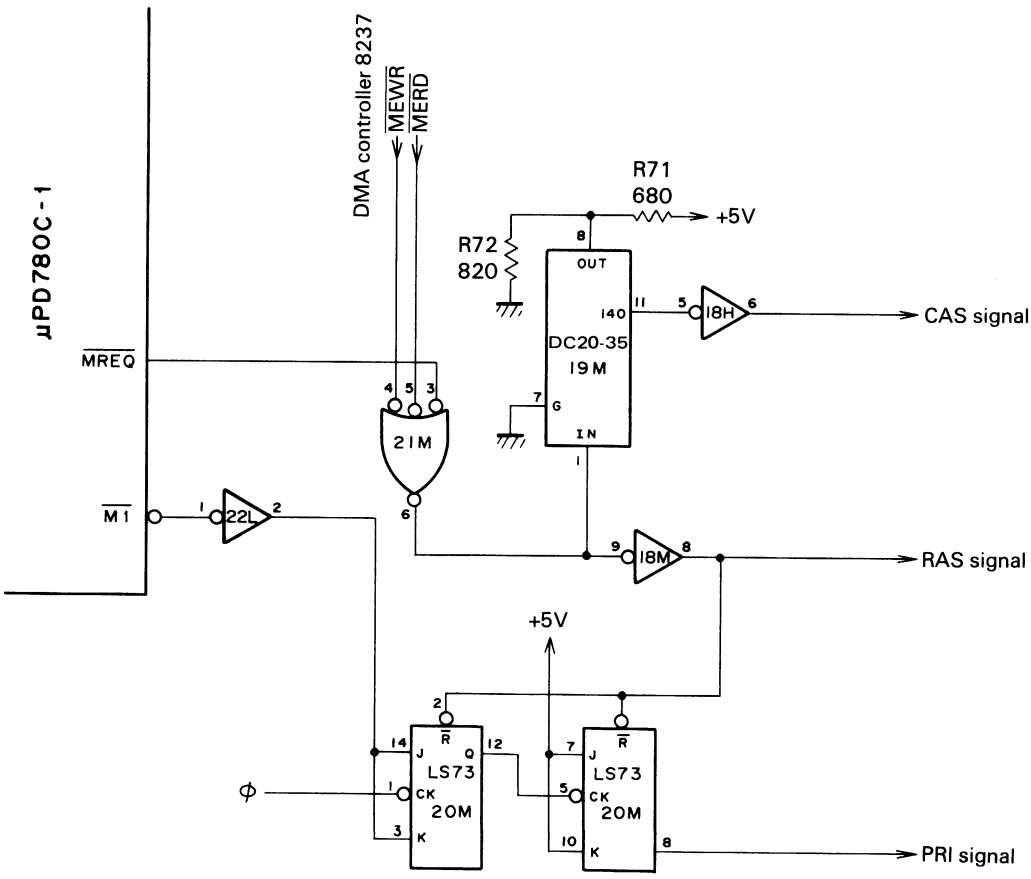
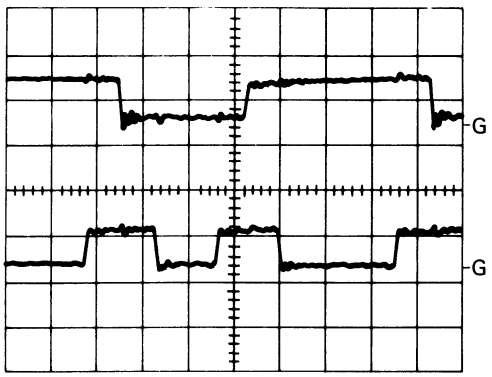
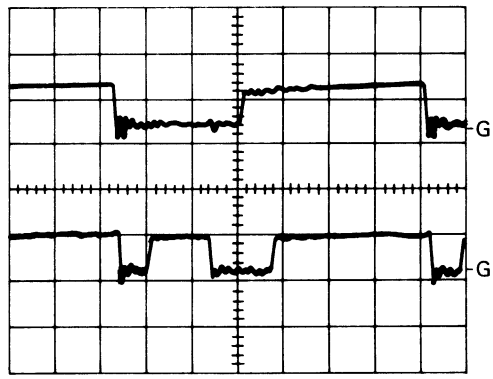


Fig. 4-65



Upper: M1
Lower: D RAM $\overline{RAS}$
sweep 0.1 μsec 5V/div.

Fig. 4-66



Upper: M1
Lower: RAS
Sweep 0.1 μsec 5V/div.

Fig. 4-67

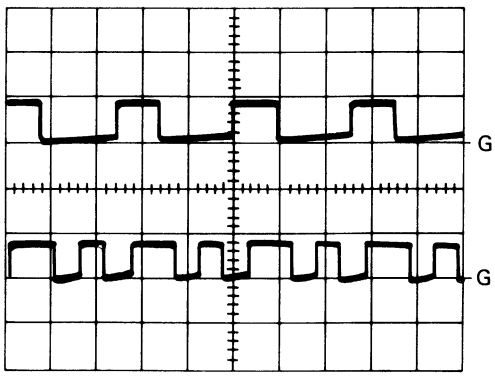
4.19.9 RAS/CAS Signal Supply Circuit

Address allocation of 64 KB RAM is made by dividing into high-order and low-order bits and accompanied by strobe signals called RAS (Row Address Select) and CAS (Column address select). The circuit shown in Fig. 4-65 is used for supply of RAS and CAS signals from the CPU.

The $\overline{RAS}$ signal is supplied by $\overline{WR}$, $\overline{RD}$ and $\overline{MREQ}$ signals output from the CPU. That is, address allocation to the D RAM is made when the $\overline{MREQ}$ signal is active and the $\overline{WR}$ or $\overline{RD}$ signal is active.

These signals are supplied through the gate of IC21M.

The $\overline{CAS}$ signal is obtained by applying the output of pin 6 of IC21M which is supplied as a $\overline{RAS}$ signal to the delay element IC19M to delay the signal 140 nsec.



Upper: RAS
Lower: CAS
Sweep 0.5 μsec. 5V/div.

Fig. 4-68

4.19.10 Gate circuit for Supplying $\overline{WE}$ Signal to D RAM

$\overline{WE}$ signal to DRAM is supplied by the gate circuit shown in Fig. 4-71.

► NON DMA transmission

As pin 2 input of IC23K is always low-level, pin 3 output of IC23K is high level, and $\overline{WE}$ signal to D RAM is controlled by only $\overline{MEWR}$ signal.

The timing chart in this time is shown in Fig. 4-69.

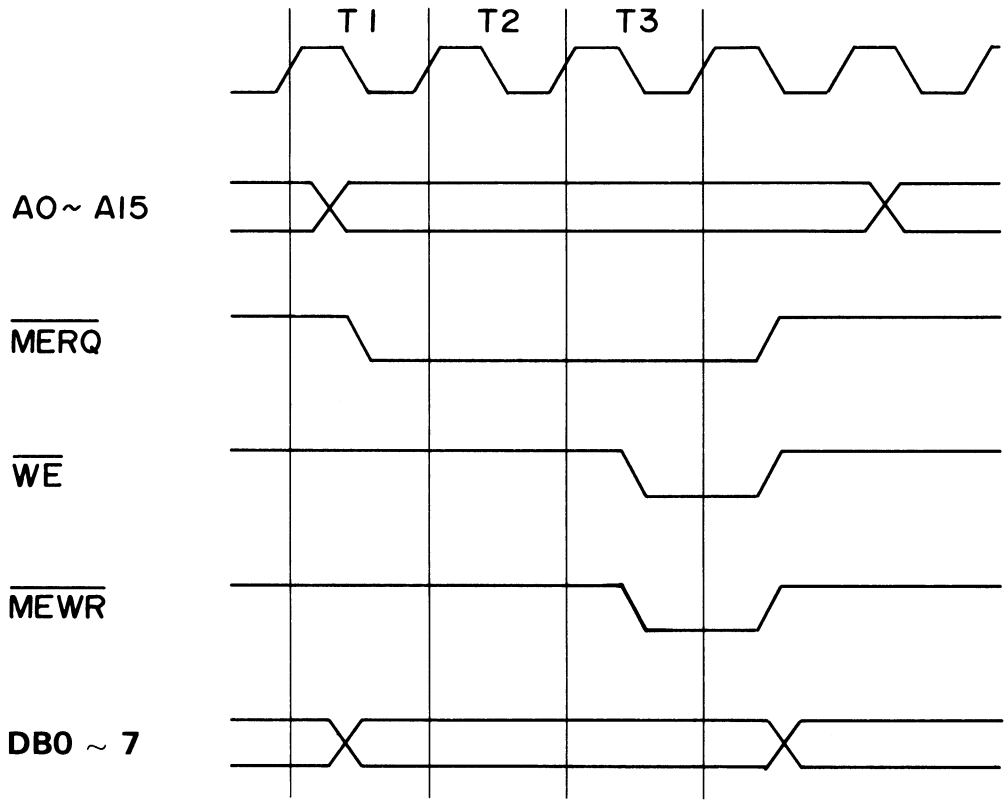


Fig. 4-69

► DMA transmission

In DMA transmission, data writing to the memory must be performed guaranteeing therefore, $\overline{WE}$ signal is supplied to D RAM with the two flip-flop of the circuit shown in Fig. 4-71 being late for 3 clocks from the trailing edge of $\overline{MEWR}$ signal.

The timing chart in this time is shown in Fig 4-70.

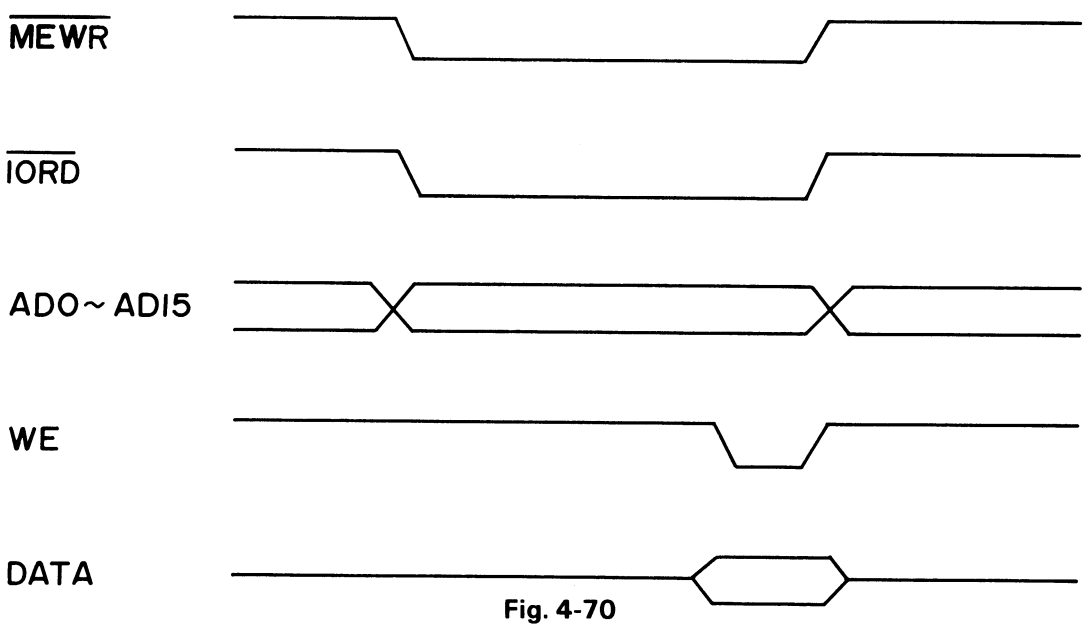


Fig. 4-70

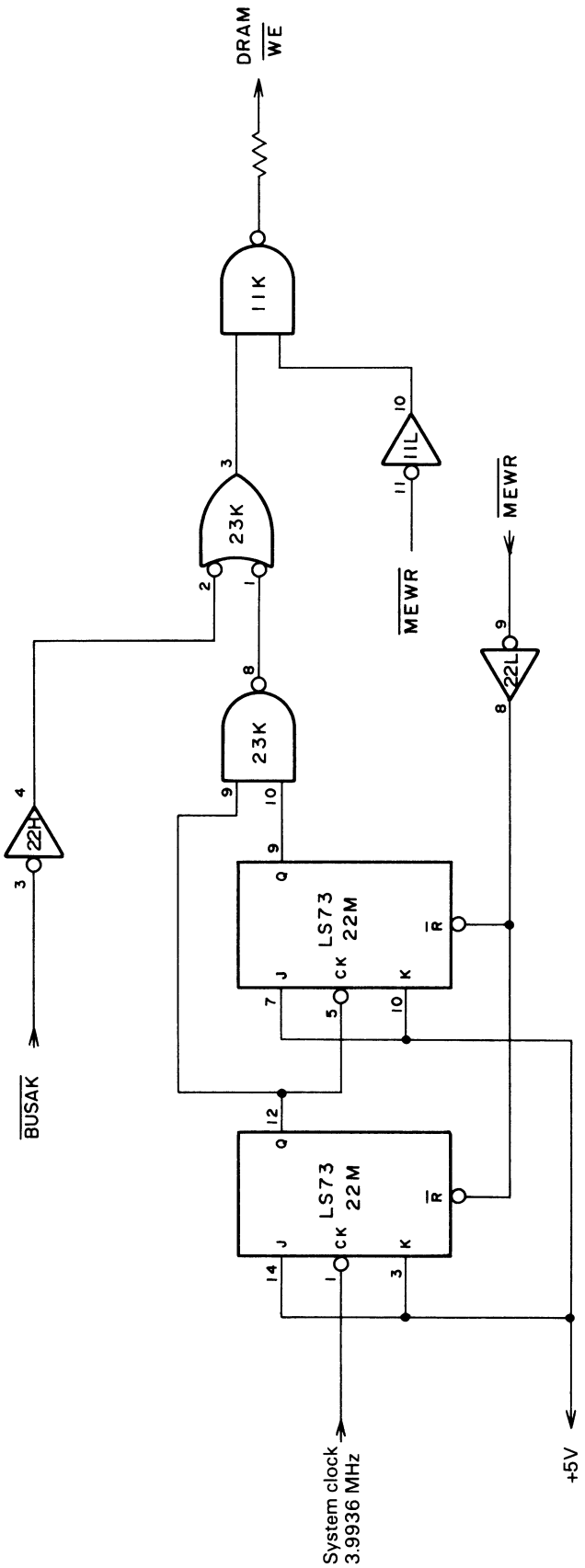


Fig. 4-71 D-RAM $\overline{WE}$ signal supply circuit

4.19.11 D-RAM $\overline{RAS}$ Signal supply gate circuit

The $\overline{RAS}$ signal applied to the D-RAM is supplied through the gate which takes the AND of the $\overline{RAS}$ and PRI signals supplied from the CPU through the delay element and the bank select signal supplied from the memory bank register.

The timing of input/output of the gate in the M1 cycle is shown in Fig. 4-73. The $\overline{RAS}$ signal of the memory bank selected in the M1 cycle is made active low at OP code fetching and refreshing. (RAS ONLY REFRESH)

The $\overline{RAS}$ signal of the memory bank not selected is made active low only at refreshing. At this time, all the D-RAMs are refreshed.

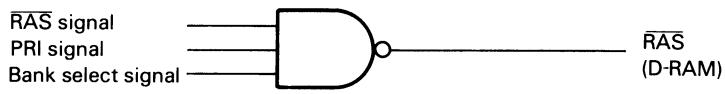


Fig. 4-72

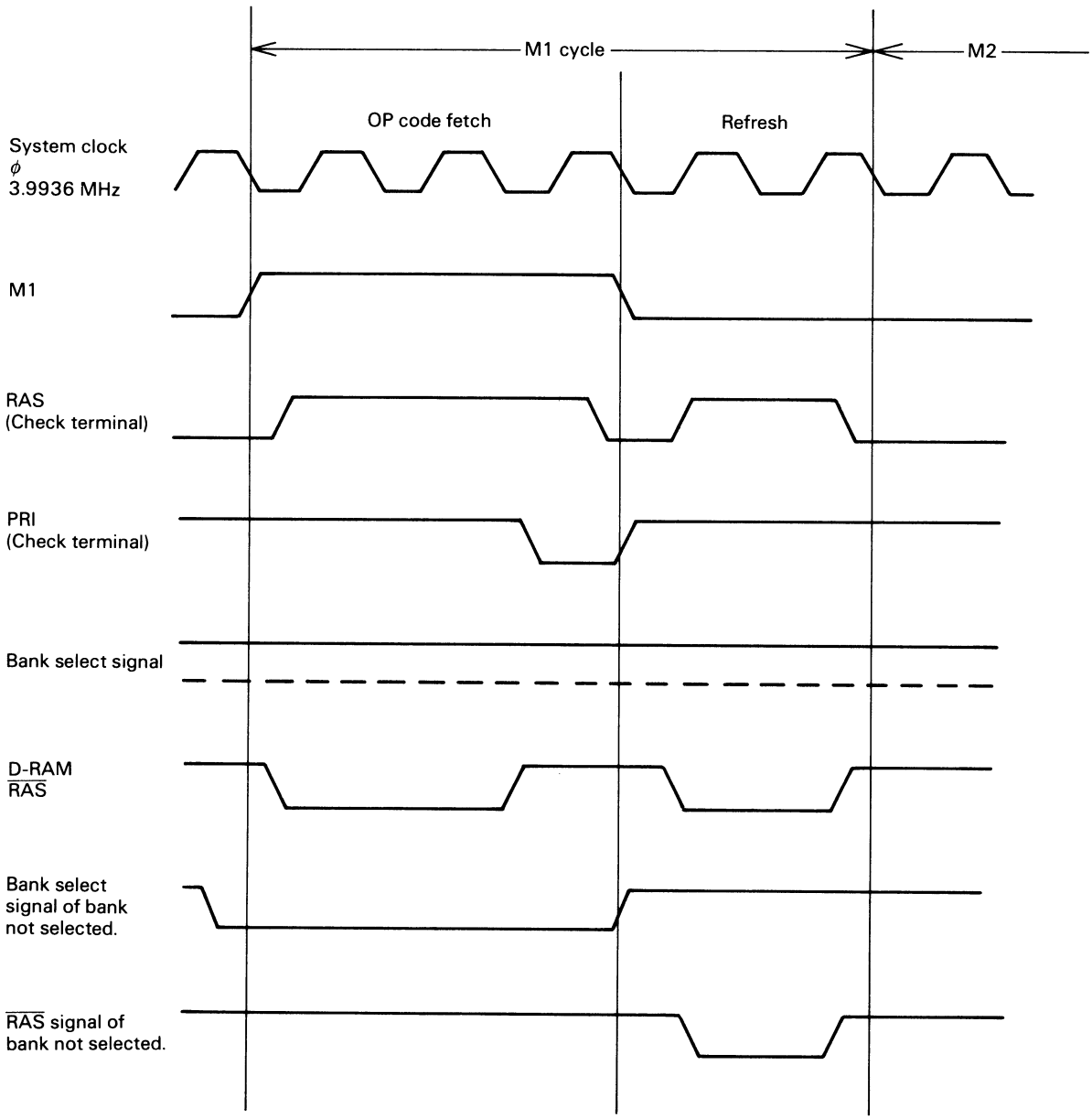
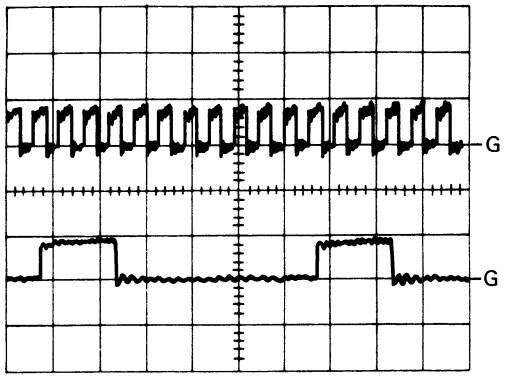
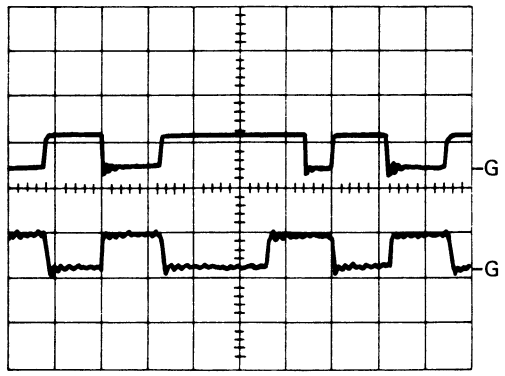


Fig. 4-73



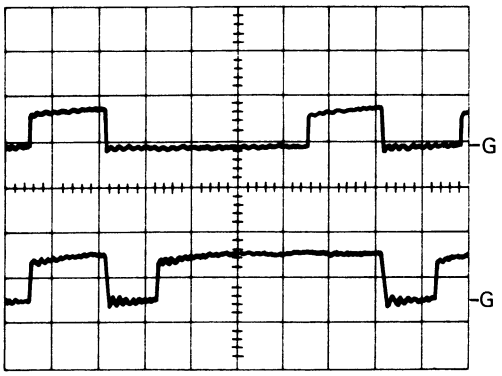
Upper: System clock
ϕ3.9936 MHz
Lower: M1
(Sweep 0.5μsec. 5 v/div.)

Fig. 4-74



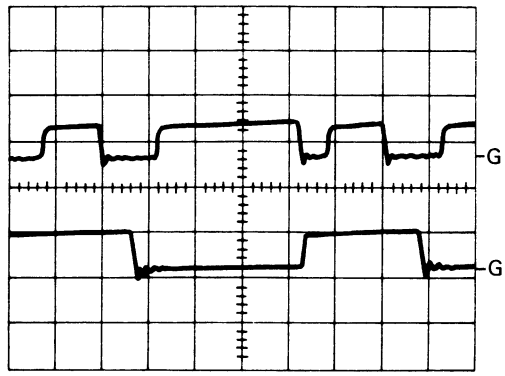
Upper: $\overline{RAS}$
Lower: $\overline{RAS}$
(Bank select)
(Sweep 0.2 μsec 5V/div)

Fig. 4-77



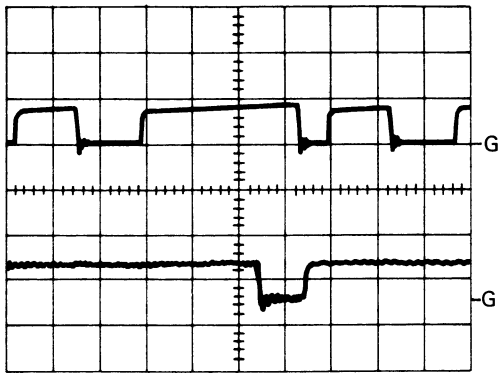
Upper: $\overline{M1}$
Lower: $\overline{RFSH}$
(μPD780, Pin 28)
(Sweep 0.5μsec. 5 v/div.)

Fig. 4-75



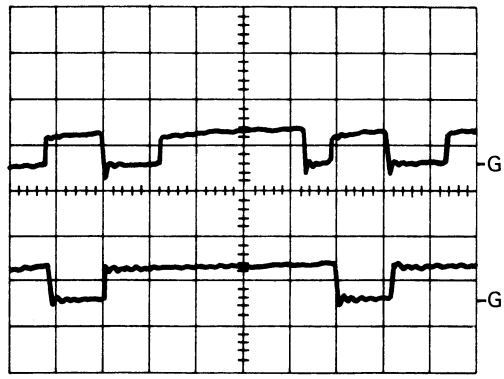
Upper: RAS
Lower: Bank not selected
Pin 13 of IC11H
(Sweep 0.2μsec. 5 v/div.)

Fig. 4-78



Upper: RAS
Lower: PRI
(Sweep 0.2 μsec 5V/div)

Fig. 4-76



Upper: RAS
Lower: Pin 12 of IC 11H
Bank not selected
(Sweep 0.2 μsec 5V/div)

Fig. 4-79

4.19.12 D-RAM $\overline{CAS}$ Signal Supply Gate Circuit

The $\overline{CAS}$ signal applied to the D RAM is supplied by AND of RAS, CAS and $\overline{RFSH}$ signals applied to the gate circuit shown in Fig. 4-80. In this case, the timing in the M1 cycle is as shown in Fig. 4-81. The D RAM is refreshed by the $\overline{RAS}$ signal. The $\overline{CAS}$ signal is set to high level during the refresh period.

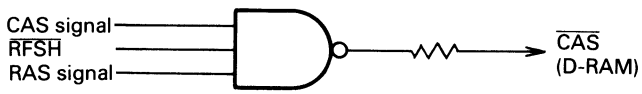


Fig. 4-80

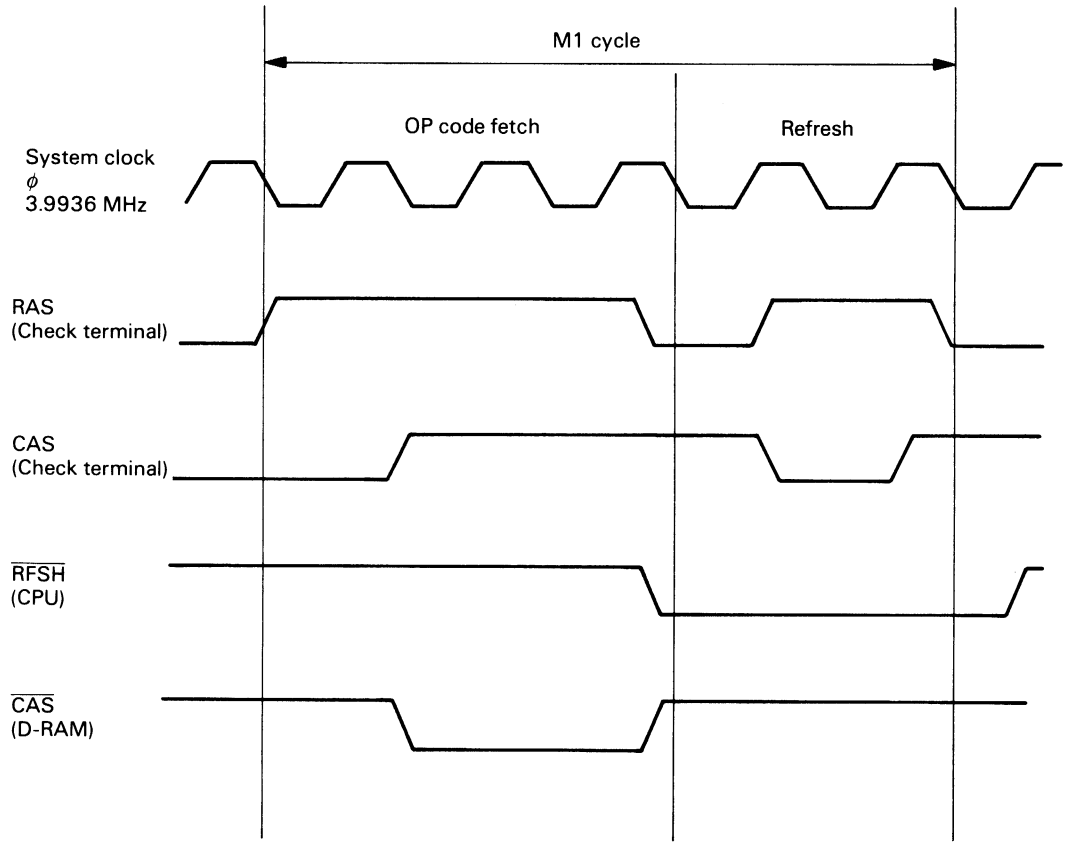
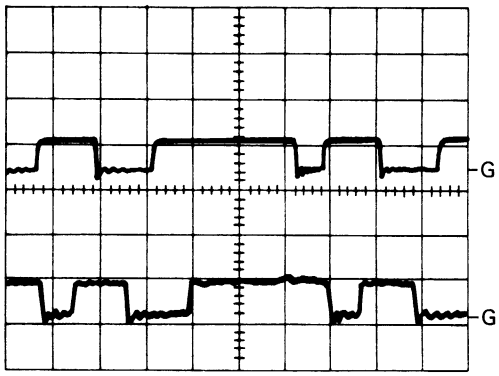
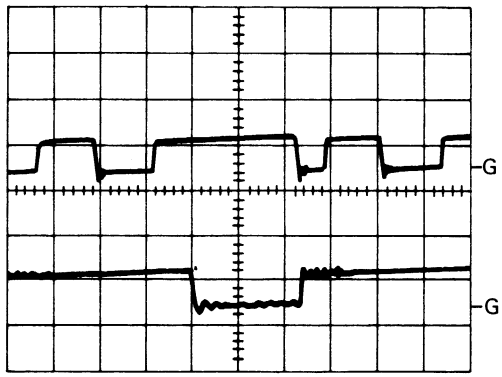


Fig. 4-81



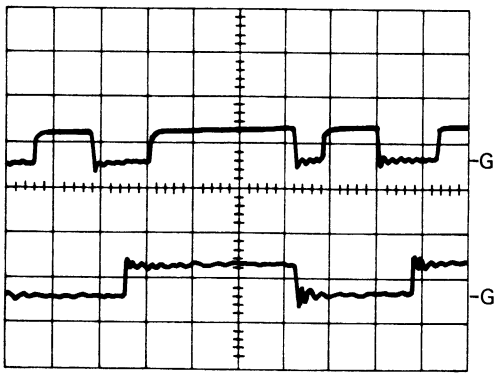
Upper: RAS
Lower: CAS
(Sweep 0.2μsec. 5 v/div.)

Fig. 4-82



Upper: $\overline{\text{RAS}}$
Lower: $\overline{\text{WE}}$ (D-RAM)
(IC12 Pin 72)
(Sweep 0.2 μsec. 5V/div.)

Fig. 4-84



Upper: $\overline{\text{RAB}}$
Lower: $\overline{\text{RFSH}}$
(IC12J Pin 12)
(Sweep 0.2μsec. 5 v/div.)

Fig. 4-83

4.19.13 Data Input/Output Control

Data input/output to the D-RAM is made through the 3-state bus buffer LS244 (7H and 6H). Input/output is controlled by 1G and 2G terminals.

The 2G terminal is connected to the ground.

Therefore, the 2G terminal is usually at low level, and the input data from the data bus is output as a data to be written into the D-RAM as it were.

AND of the D-RAM select signal and $\overline{\text{MERD}}$ signal from the CPU is applied to the 1G terminal. The signal controlled by the input signal to the 1G terminal, that is, the data to be read out from the D-RAM, is selected by the D-RAM $\overline{\text{MERD}}$ signal is active.

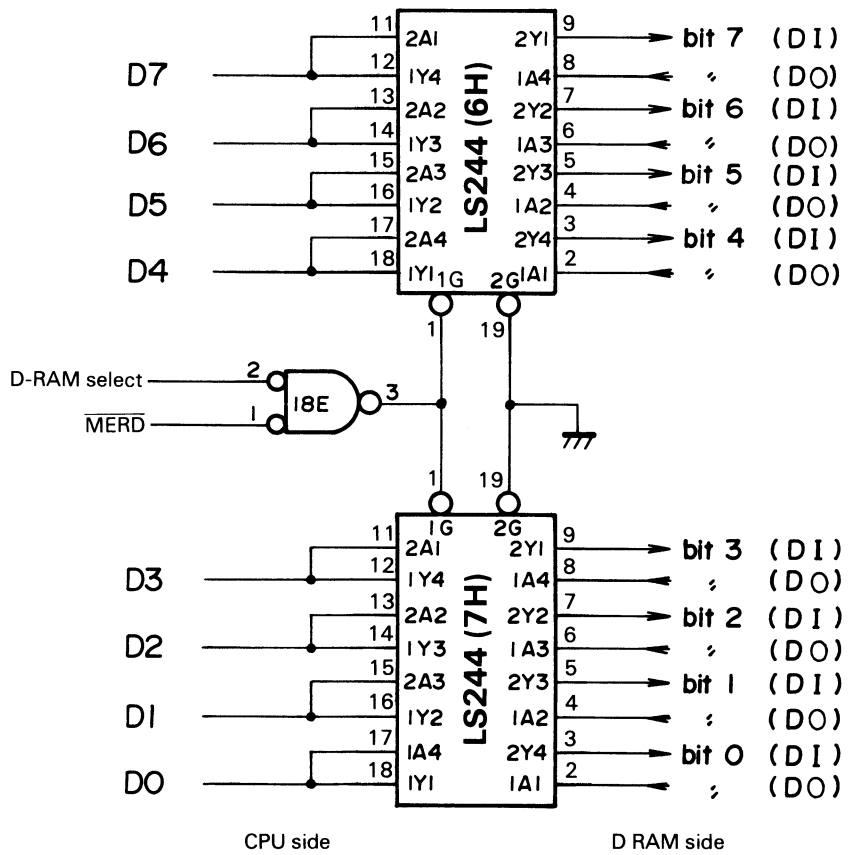


Fig. 4-85

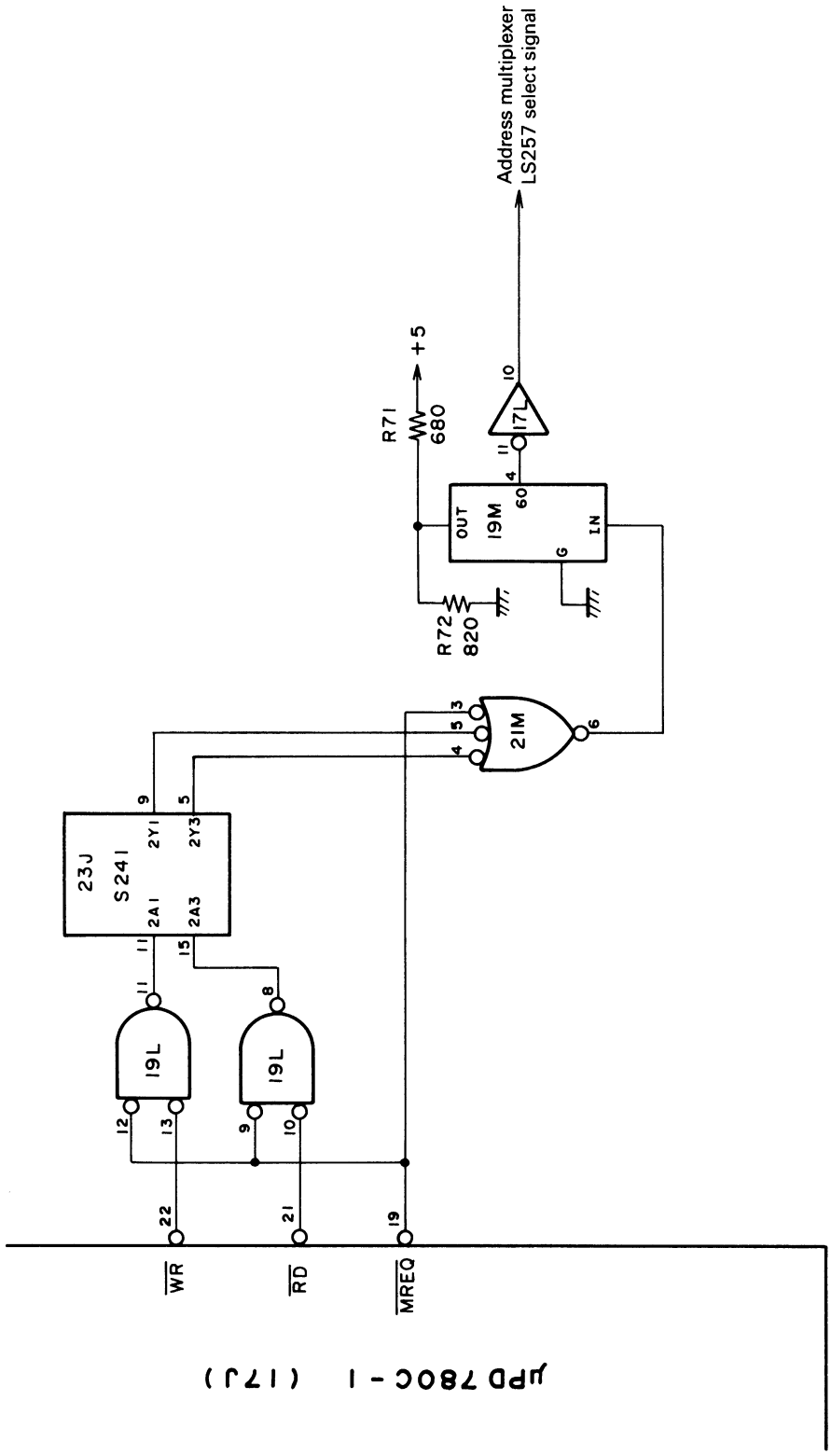


Fig. 4-86 D-RAM Address Multiplexer LS257 (7J, 8J, 9J, and 11J) Select Signal Supply Circuit

4.19.14 Refresh Circuit

The D-RAM stores one-bit information in correspondence with charge/discharge of one condenser. Therefore, the stored data will disappear in time.

Thus, a refresh operation is necessary to re-store the same data before it disappears.

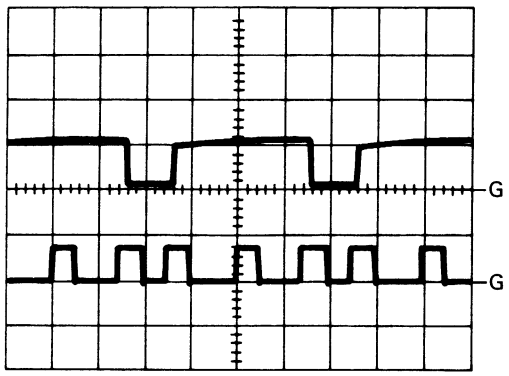
For this purpose, a refreshing address and a refresh instruct signal ($\overline{RFSH}$) are generated by utilizing the idle time during decoding inside after the CPU reads an instruction code.

In this system, by taking AND of $\overline{RFSH}$, $\overline{RAS}$ and PRI signals, the $\overline{RAS}$ signal is supplied to the D-RAM in synchronization with the $\overline{RFSH}$ signal output from the CPU, and it is used as a refresh signal.

As a refresh address, the low-order address is selected by the $\overline{RAS}$ signal.

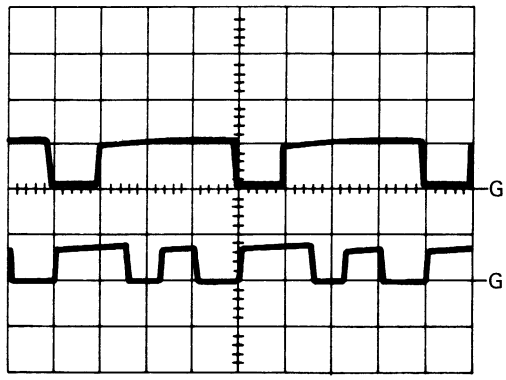
This refresh method is called RAS ONLY REFRESH.

The timing chart is shown in Figs. 4-87 and 4-88.



Upper: RFSH (CPU)
Lower: RAS (D-RAM)
Sweep 0.5 μsec.
5V/div.

Fig. 4-87



Upper: RFSH (CPU)
Lower: CAS (D-RAM)
Sweep 0.5 μsec.
5V/div.

Fig. 4-88

4.19.15 External Memory Select Signal Supply Circuit

The select signal to external optioned memory is supplied by the gate output from PIN 8 of IC 20F shown in Fig. 4-89.

When external memory is selected, memory in main unit must never be selected. For this reason, the select inhibit in signal to P-ROM, D-RAM and C-MOS RAM respectively and the select signal to the external memory are connected with the gate input of IC 20F.

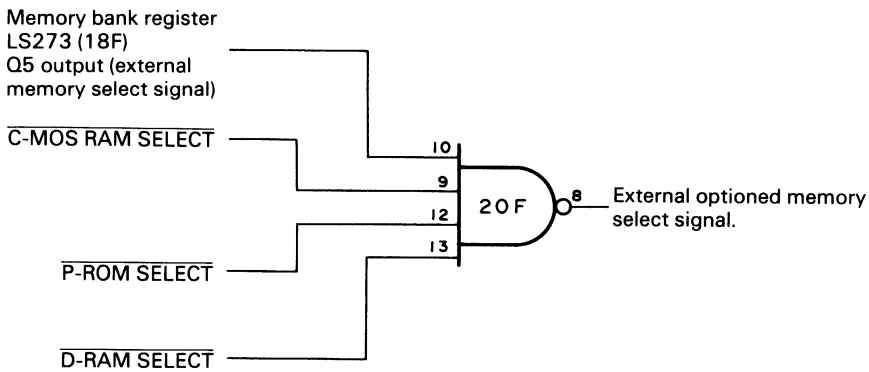
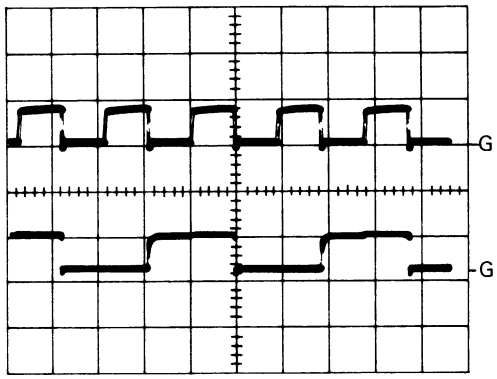
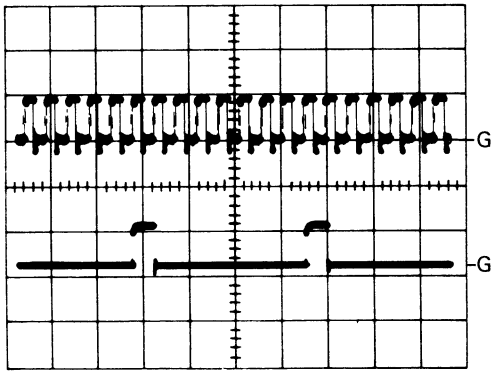


Fig. 4-89 External memory select supply circuit



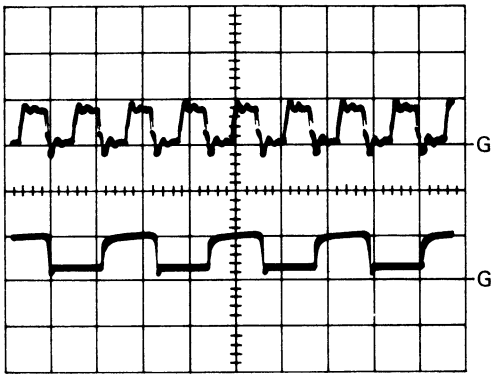
IC19H
Upper: 2QC output (pin 9)
Lower: 2QD output (pin 8)
(Sweep 0.5 μsec 5V/div)

Fig. 4-90



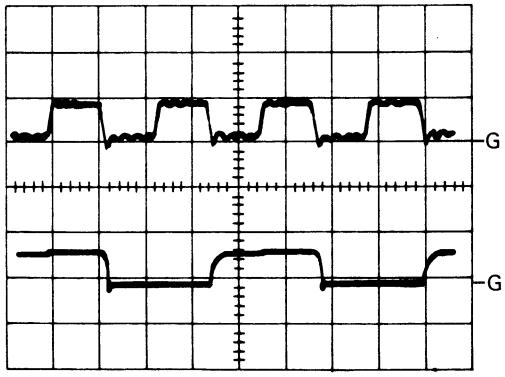
μPD765
Upper: φ (pin 19)
Lower: WCLK (pin 21)
(Sweep 0.5 μsec 5V/div)

Fig. 4-91



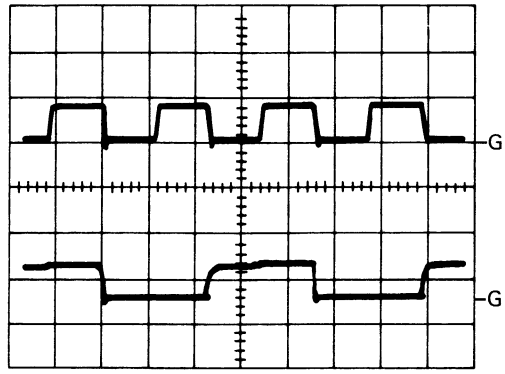
IC19H/LS393
Upper: 2A input (pin 13)
Lower: 2QA (pin 11)
(Sweep 0.1 μsec 5V/div)

Fig. 4-92



Upper: 2QA output (pin 11)
Lower: 2QB output (pin 10)
(Sweep 0.1 μsec 5V/div)

Fig. 4-93



Upper: 2QB output (pin 10)
Lower: 2QC output (pin 9)
(Sweep 0.2 μsec 5V/div)

Fig. 4-94

CHAPTER 5
G10GMS BOARD

CONTENTS

5.1 General

The CRT controller mounted on the Q10 GMS board includes the graphic display controller (μPD7220) which converts data coming from the main control circuit into a video signal and supplies it, together with horizontal and vertical sync signals, to the CRT drive unit (CDU).

The graphic display controller (GDC) controls a raster scan-type CRT according to control commands and associated parameters which the CPU (μPD780) supplies, in character mode (80 characters by 25 lines) or in graphic mode (640 by 400 dots). It permits dynamical change over character display/draw mode and graphic display/draw mode.

One of the most distinct features of the QX-10 is that the CRT controller is assigned as an I/O device for the CPU. Ordinarily, the CRT controller is, for the CPU, just like the memory which the CPU can access directly by referring to an address and, in such a system, load instructions are used to move data into V-RAM to display images.

In our system, the CPU regards the GDC (μPD7220) as an I/O device and the bus lines which the GDC controls are separate from the system bus the CPU controls. This permits the GDC and CPU to operate in parallel and, naturally, the GDC's arithmetic capabilities are used to realize high-speed graphic functions.

5.2 Block Diagram

Fig. 5-1 is a block diagram of the CRT controller. The GDC is the interface between the main circuit and the CRT controller.

Receiving data from the main circuit, the GDC generates data, which are to be written into V-RAM, along with sync and control signals.

Each word of the data written in V-RAM consist of 16 bits. In graphic mode, all the 16 bits make up a graphic data. In character mode, the most significant eight bits make up an attribute data while the least significant eight bits make up a character code.

The data held in V-RAM are converted to serial data with a shift register and sent to the CRT as a video signal combined with sync signals.

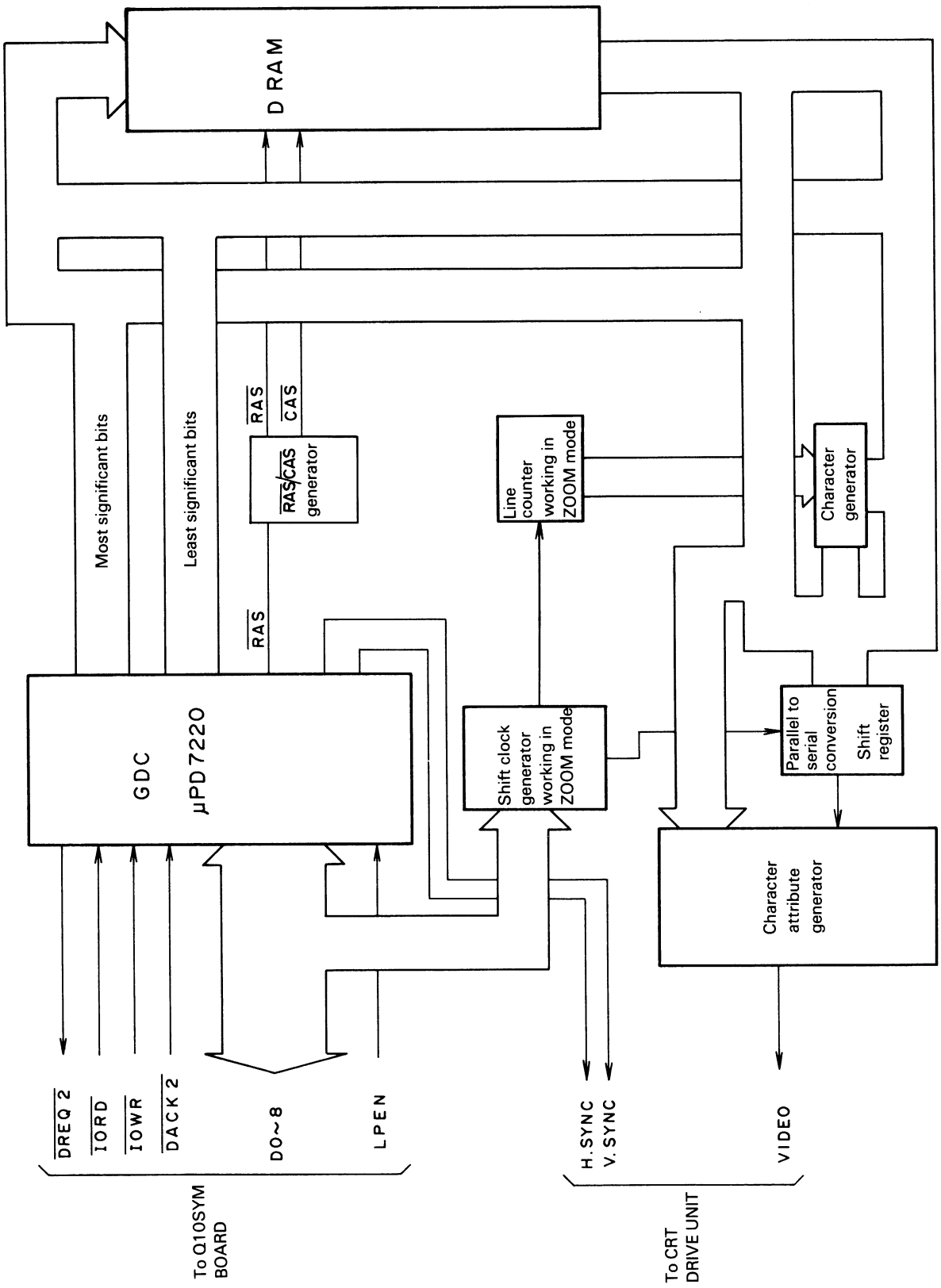


Fig. 5-1 Block Diagram of Q10 GMS Circuit

5.3 Graphic Display Controller (μPD7220)

5.3.1 General

The graphic display controller (μPD7220) is a peripheral device controller LSI which operates to display characters and graphic patterns on a raster scan-type CRT.

Its capabilities include not only generation of sync signals and control for displaying characters but also control of high-speed graphics and large-capacity video memory. So, its applications range from simple control of character displays to sophisticated graphics. Further, one of the applications which have nothing to do with display cotrol is control of large-capacity memory.

5.3.2 Features

(1) High-speed graphics capabilities

It permits drawing of line segments, quadrilaterals, arcs, circles, and other graphic figures at a speed of 960 nsec/word. During every word time of 960 nsec, it computes the address of the dot which is to be drawn next. That is, the dot time includes both the time needed to compute dot address and that to draw a dot. Figures, therefore, may be drawn continuously at high speed.

(2) Large-capacity V-RAM

V-RAM is the memory from which μPD7220 directly reads data from and into which writes data. Therefore, V-RAM may be provided separately from the main memory (RAM banks # 0 – # 3 on the Q10SYM board) which the CPU accesses directly. Actually our system incorporates a big-capacity V-RAM (ASCII type: 32 KB, HASCI type: 128 KB) by using sixteen 16-K bit or 64-K bit RAM chips.

(3) Scroll capabilities

The scroll commands of μPD7220 permit designation of SAD (display start address) and SL (number of lines of display area used) of V-RAM. This means the μPD7220's high speed scroll capabilities cover scrolling inside a page (INTRA PAGE) and over pages (INTER PAGE), paying, horizontal and vertical scrollings.

(4) Enlarging display/draw capabilities

The μPD7220 permits display of characters and drawing of graphic figures enlarged as many times as an integer multiple of 1 to 16.

5.3.3 Commands of the μPD7220

Twenty-one commands are prepared for the μPD7220 as listed below. (Table 5-1)

Operation Control

Command	Function	(MSB) Command code (LSB)
RESET	Initializes	0 0 0 0 0 0 0 0
SYNC	Defines operating mode and sync signal waveforms	0 0 0 0 1 1 1 DE
MASTER/SLAVE	Selects master or slave operation	0 1 1 0 1 1 1 M

Display Control

Command	Function	(MSB) Command code (LSB)
START	Starts displaying	0 1 1 0 1 0 1 1
		0 0 0 0 1 1 0 1
STOP	Stops displaying	0 0 0 0 1 1 0 0
ZOOM	Designates the times count of enlargement	0 1 0 0 0 1 1 0
SCROLL	Sets display start address and area	0 1 1 1 ——RA——
CSRFORM	Defines cursa of characters	0 1 0 0 1 0 1 1
PITCH	Defines horizontal length of V-RAM in words	0 1 0 0 0 1 1 1
LPEN	Reads light pen address	1 1 0 0 0 0 0 0

Graphics Control

Command	Function	(MSB) Command code (LSB)
VECTW	Sets parameters for drawing figures	0 1 0 0 0 1 1 0
VECTE	Designates line, quadrilateral, or circle to draw	0 1 1 0 1 1 0 0
TEXTW	Sets graphics text code	0 1 1 1 1 ——RA——
TEXTE	Designates graphic texts text to display	0 1 1 0 1 0 0 0
CSRW	Sets address to draw	0 1 0 0 1 0 0 1
CSRR	Reads address to draw	1 1 1 0 0 0 0 0
MASK	Sets mask register	0 1 0 0 1 0 1 0

V-RAM Control

Command	Function	(MSB) Command code (LSB)
WRITE	Prepares to write parameters in V-RAM	0 0 1 WLH 0 MOD
READ	Reads data from V-RAM	1 0 1 WLH 0 MOD
DMAW	Starts DMA data transfer to V-RAM	0 0 1 WLH 1 MOD
DMAR	Starts DMA data transfer from V-RAM	1 0 1 WLH 1 MOD

Table 5.1

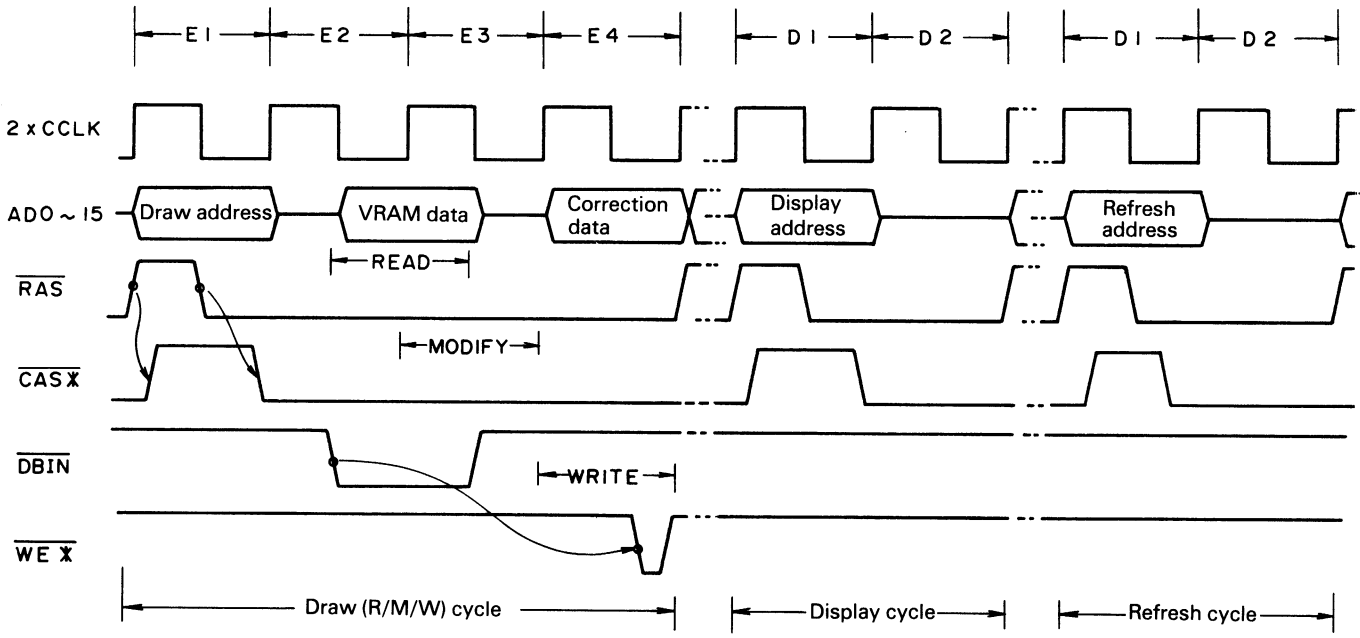
5.3.4 Timing diagrams

The GDC (μPD7220) operates through three cycles as follows.

(1) Draw cycle
(2) Display cycle
(3) Refresh cycle

During the draw cycle (1), read/modify/write is executed. During the display cycle (2), data are read from V-RAM. During the refresh cycle (1) and when H. SYNC is "1", V-RAM is refreshed.

The timing diagrams of operations performed in these cycles are given below.



Note: * Indicates a signal generated by an external circuit.

Fig. 5-2 Timing diagrams

► **Display memory RMW timing**

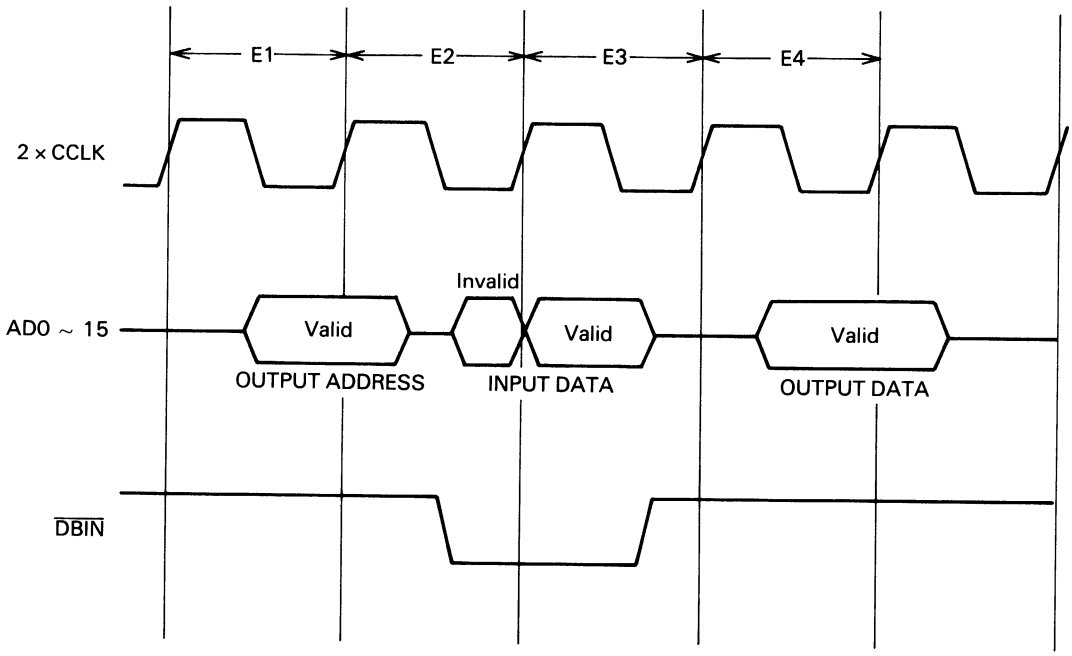


Fig. 5-3

► **Microprocessor interface write timing**

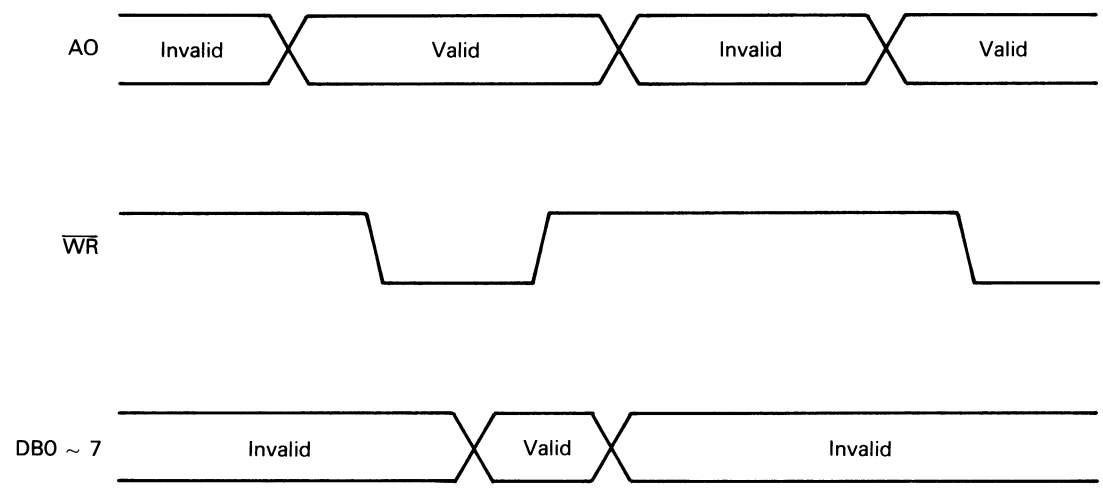


Fig. 5-4

► **Microprocessor interface read timing**

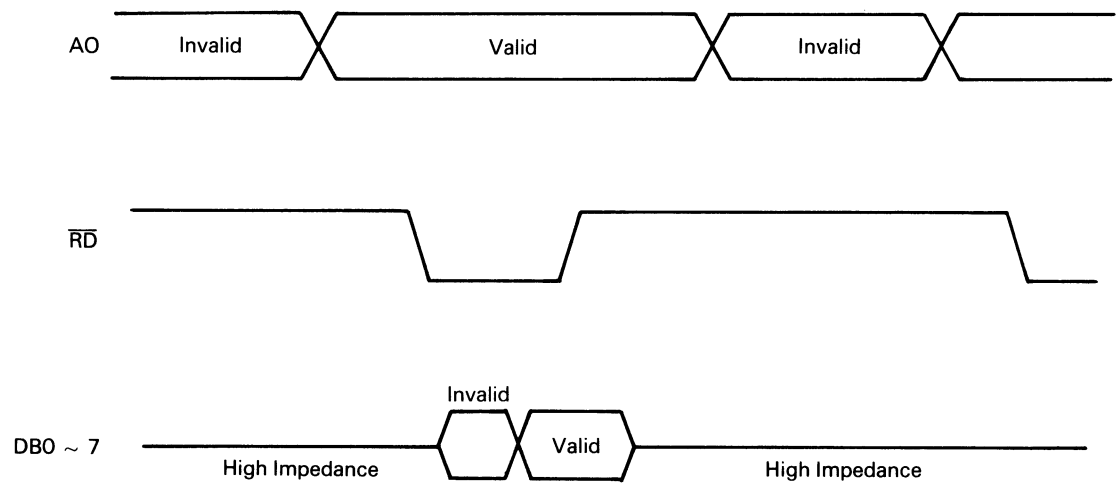


Fig. 5-5

► **Light pen input timing**

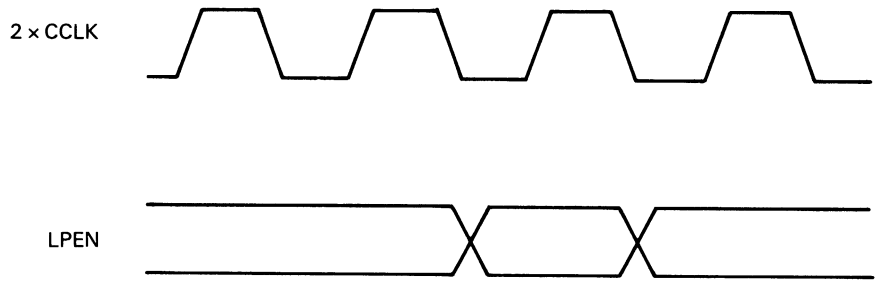


Fig. 5-6

► **Display memory Display cycle timing**

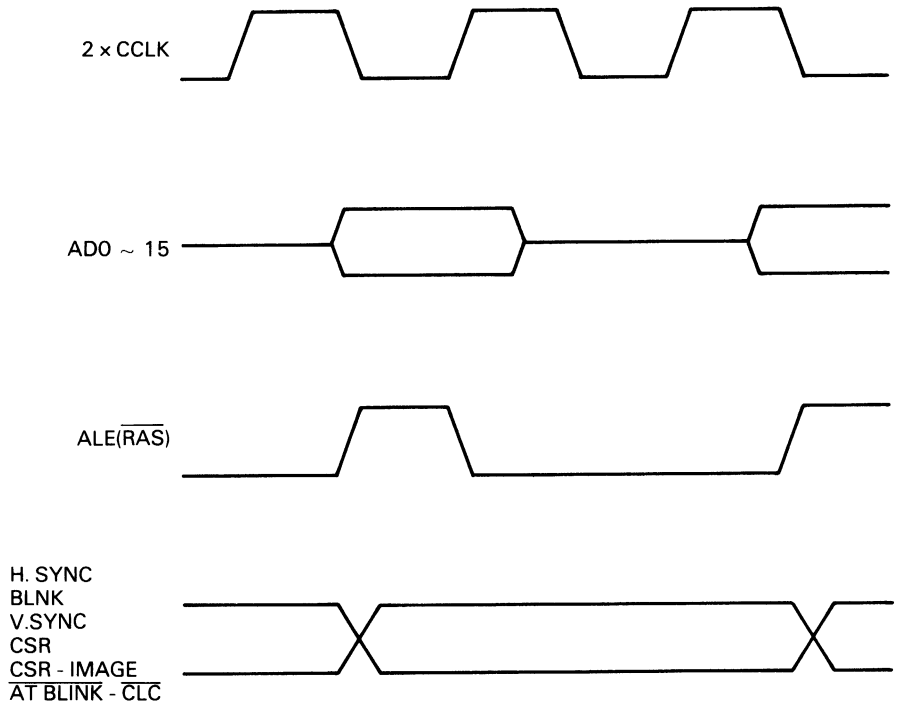


Fig. 5-7

► **Video sync signals timing**

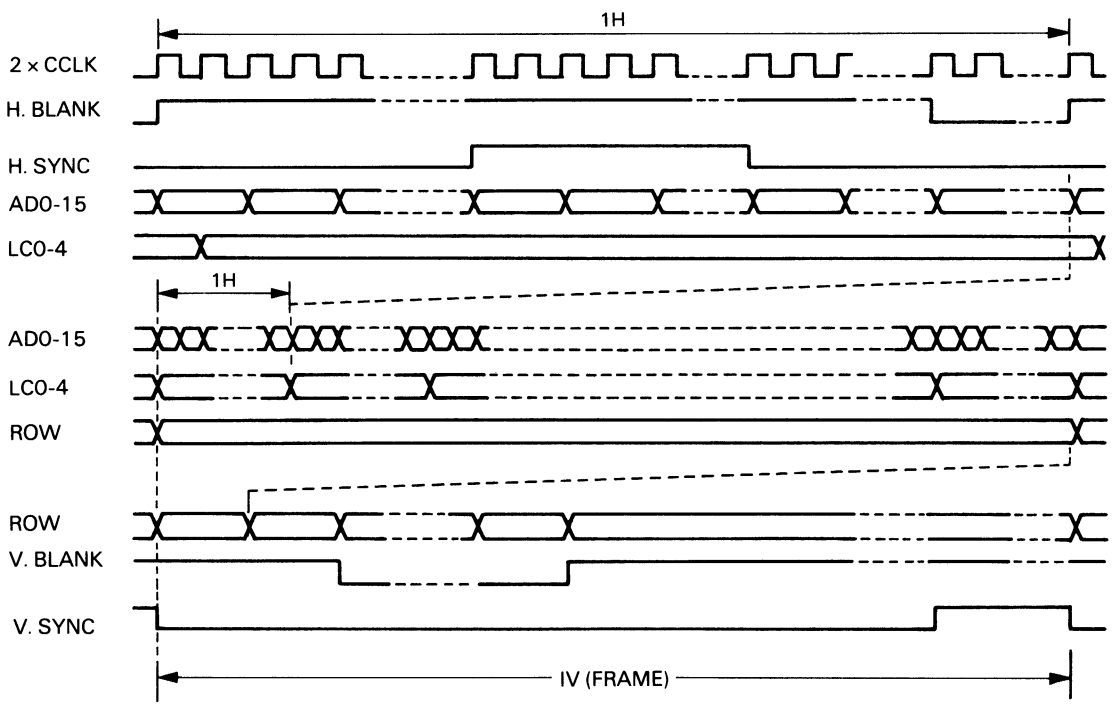


Fig. 5-8

► **Display and RMW cycles (1 x ZOOM)**

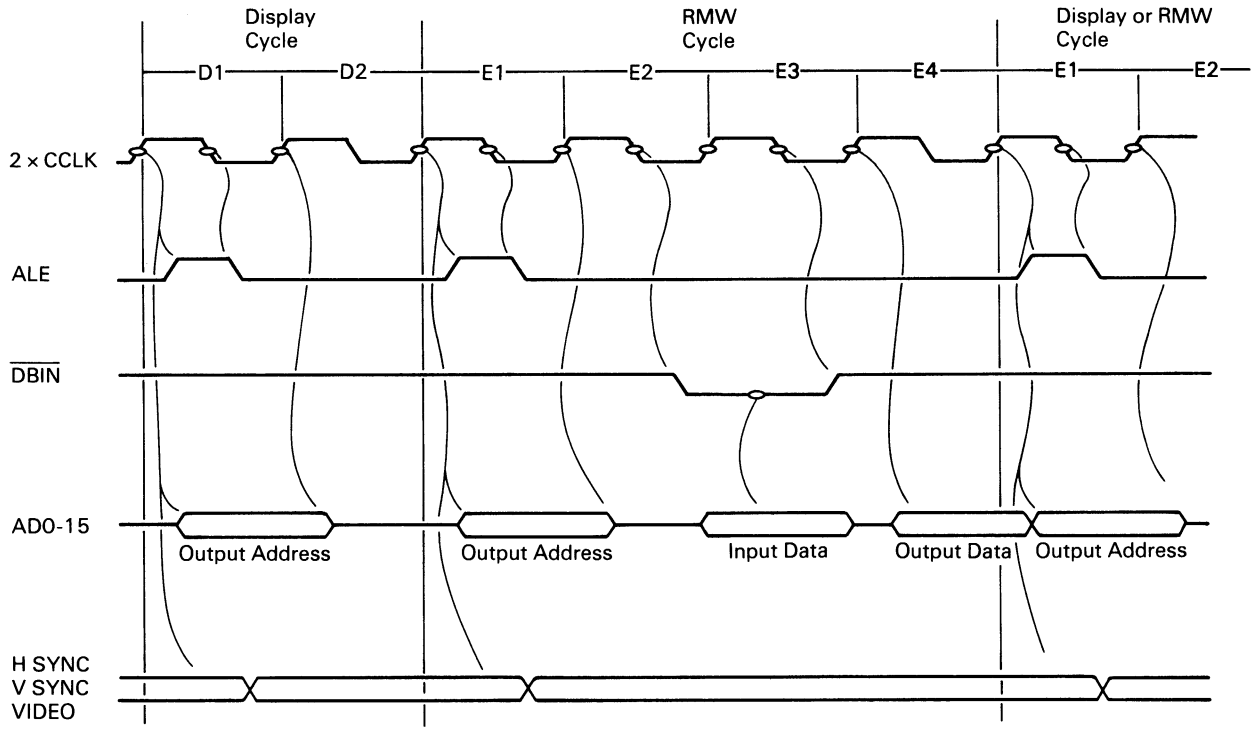


Fig. 5-9

► **Display and RMW cycles (2 x ZOOM)**

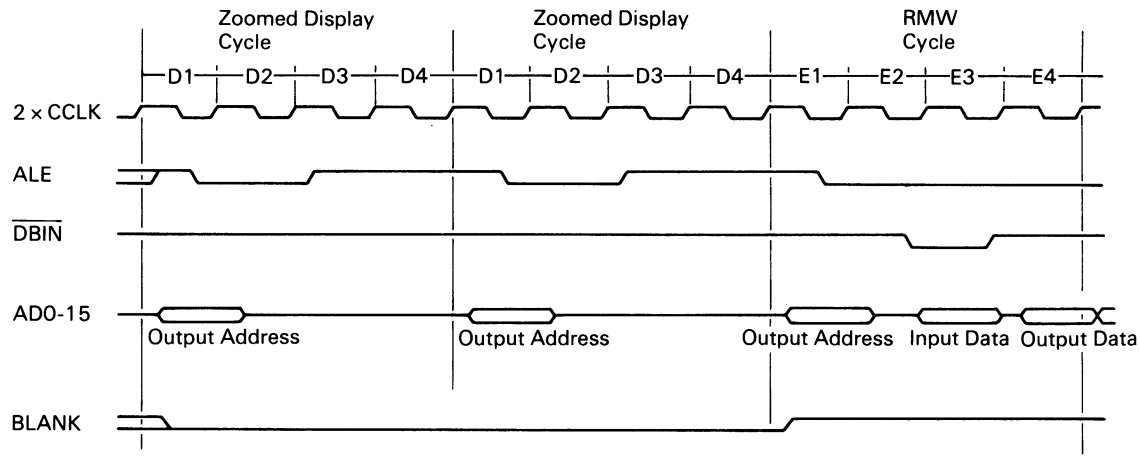


Fig. 5-10

► **Display and RMW cycles (3 x ZOOM)**

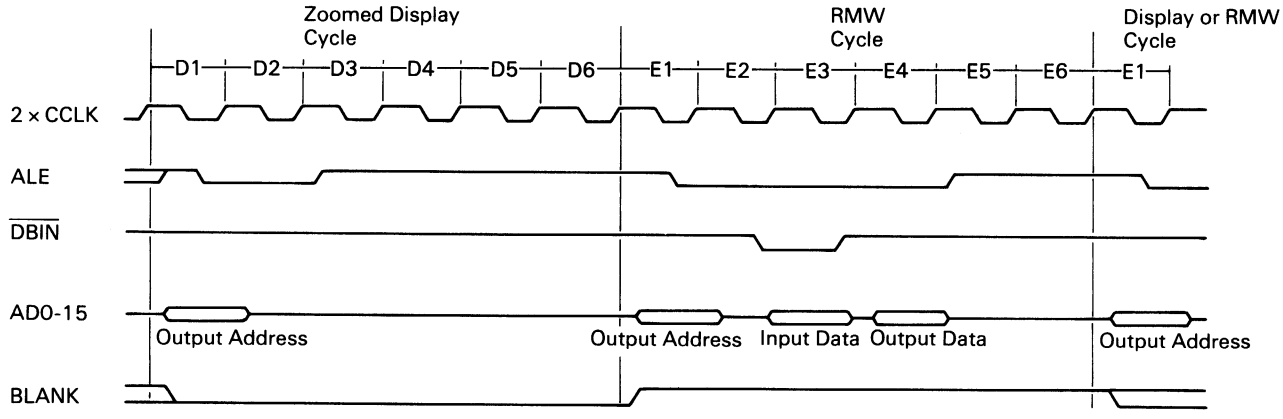


Fig. 5-11

5.4 Clock Generator

Fig. 5-12 shows the clock genrator provided for the GDC. This circuit divides the original frequency of 16.667 MHz by four into 4.16675 MHz which is delivered to terminal 2CCLK of the GDC.
The oscillator module is compensated for temperature changes so that pictures are not affected.

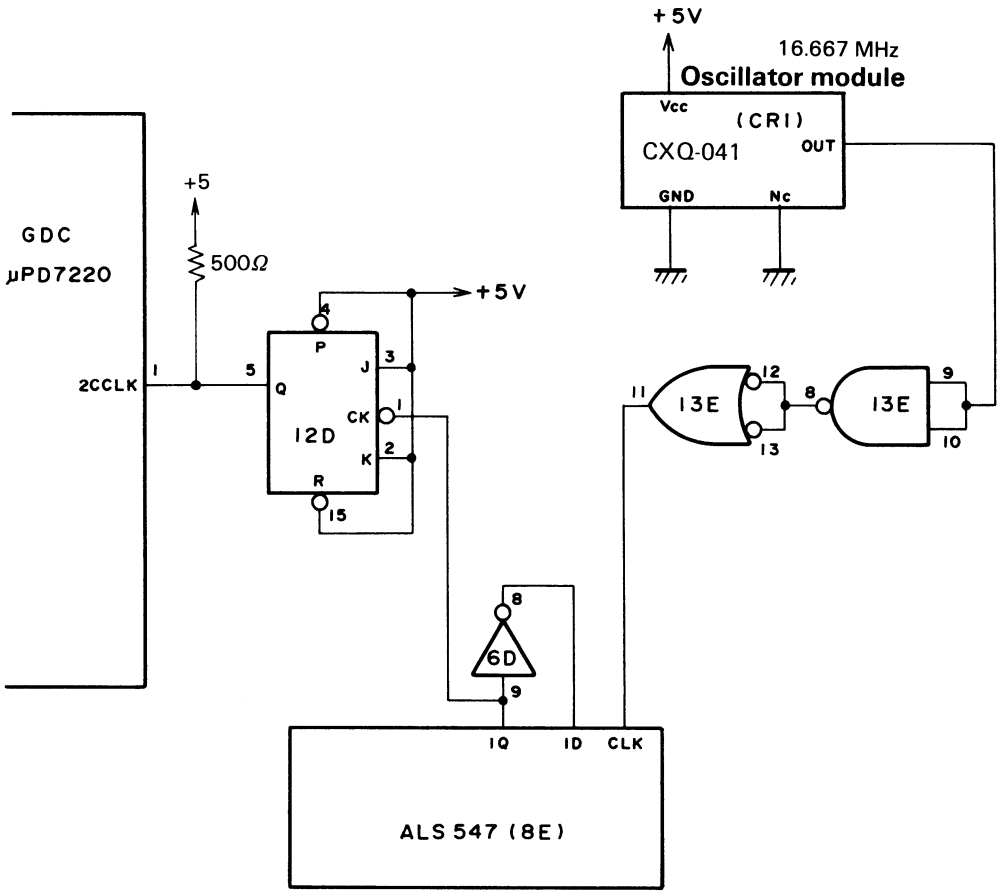


Fig. 5-12 Clock generator

5.5 Interface with the CPU

I/O addressess 38-3BH are assigned to the graphic display controller (μPD7220) and the CPU selects it with signals $\overline{\text{CSCRT}}$ and $\overline{\text{CSCCR}}$.
The μPD7220 is not provided with the input terminal of a chip select signal, and it is selected when signals $\overline{\text{RD}}$ and $\overline{\text{WR}}$, which are generated from signals $\overline{\text{IORD}}$ and $\overline{\text{IOWR}}$ coming from the main circuit, are active.
The GDC exchanges information with the CPU via the data bus, in the mode determined by the combination of A0, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ as shown below. A0 is connected to the LSB line of the system address bus.

A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	Mode
0	0	1	Reads status flag
1	0	1	Reads data (from GDC)
0	1	0	Writes parameter
1	1	0	Writes command

Table 5-2

The data bus is driven by a bidirectional bus driver LS245(12A) which not only switches the transfer direction of the bus lines according to the mode of data transfer but also drives the bus. Signal DIR used to switch the bus direction is signal $\overline{RD}$ of the μPD7220. If DIR is low level (that is, during read from the μPD7220), the data bus is directed from the μPD7220 to the CPU. If DIR is high level (during write to the μPD7220), the bus is directed from the CPU to the μPD7220.

DIR	Bus direction
Low	GDC → CPU
High	CPU → GDC

► **DMA controller**

DREQ, the DMA Request signal, enters the DREQ terminal of the DMA controller (μPD8237) mounted on the main board.

$\overline{DACK}$, the DMA Acknowledge signal which remains high during DMA transfer, comes from the $\overline{DACK}$ terminal of the DMA controller. This signal is used to count data bytes transferred and designate when to start transfer.

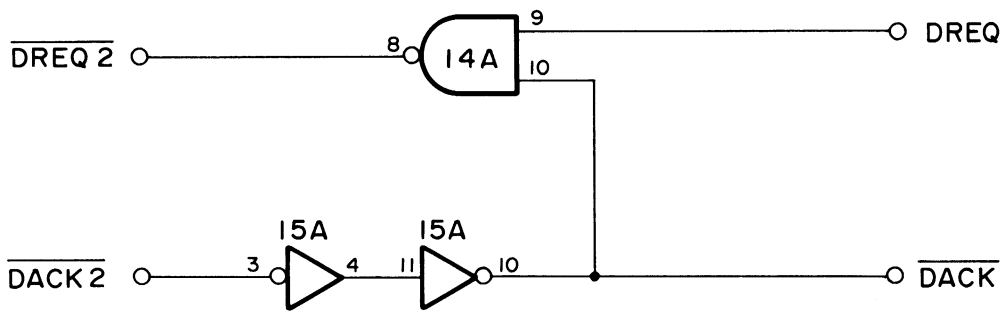


Fig. 5-13 DMA controller

The timing diagrams of $\overline{DREQ2}$ and $\overline{DACK2}$ are shown in Figs. 5-13 and 5-15.

► **Microprocessor interface DMA read timing**

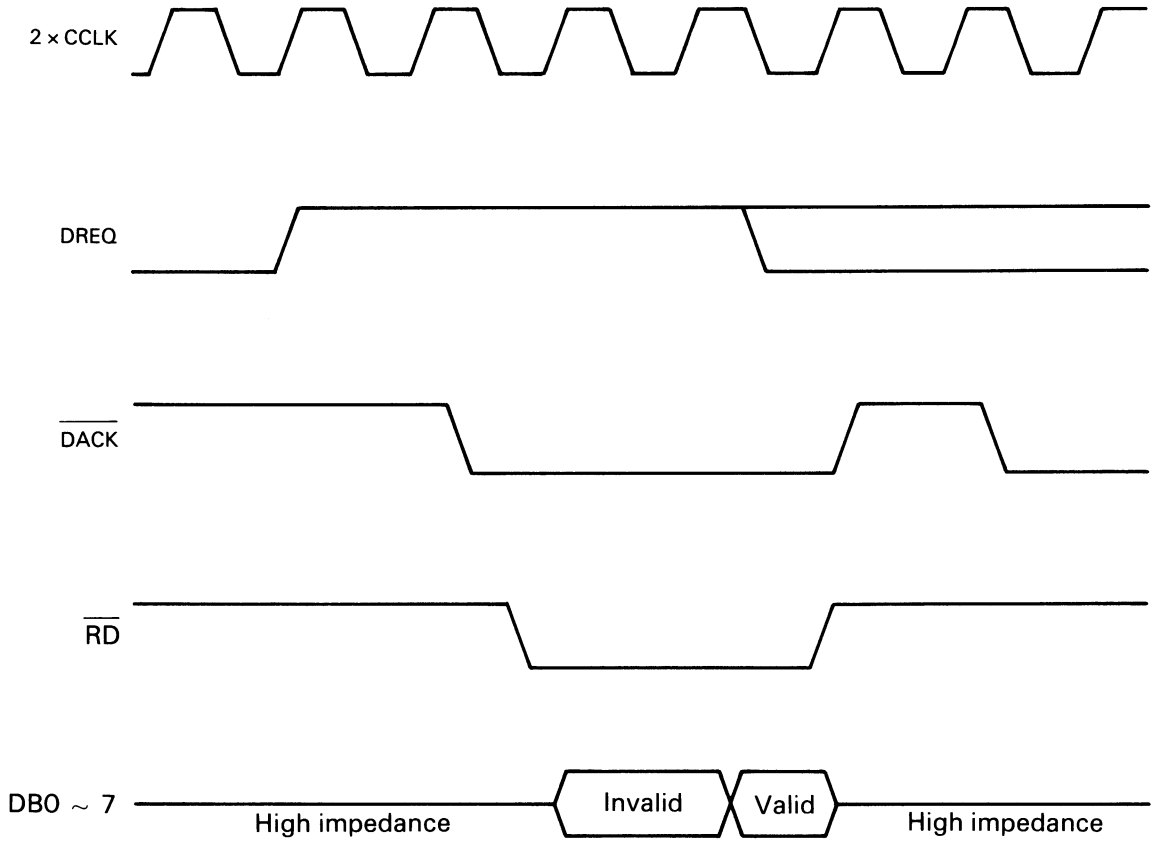


Fig. 5-14

► **Microprocessor interface DMA write timing**

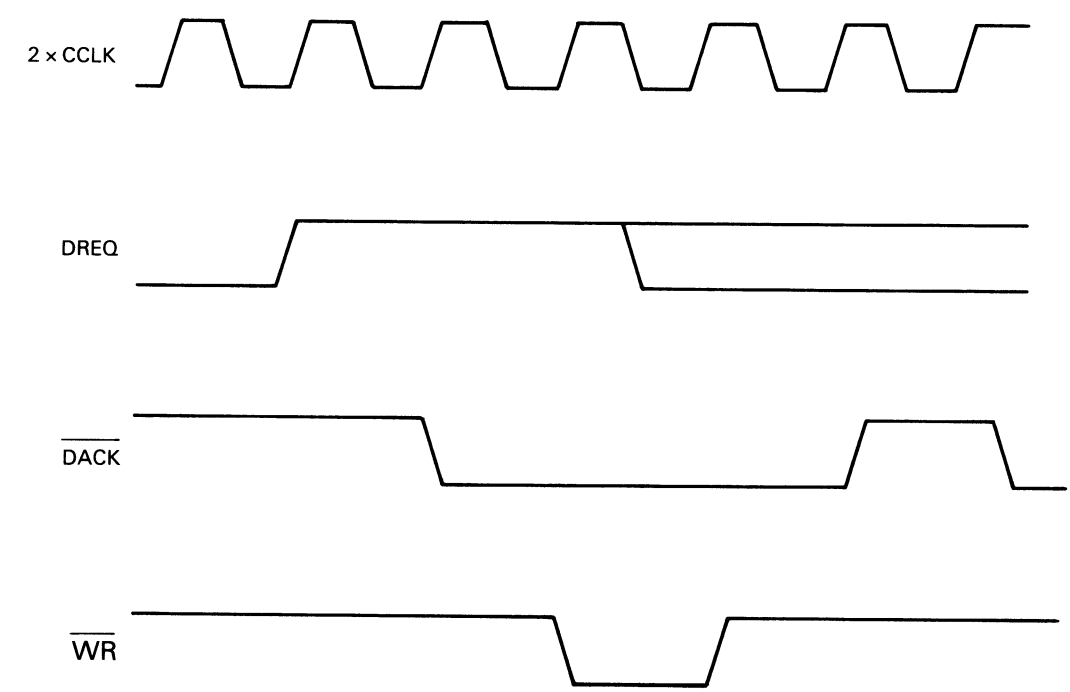


Fig. 5-15

5.6 Light Pen Interface

The μPD7220 is provided with input terminal LPEN (Light Pen) to which a signal, generated when the light pen connected detects light, maybe entered to find the location the light pen points to.

The light pen signal first enters the one-shot LS221 (1D) that converts the signal to a pulse of approximately 240 nsec wide, with the pulse width determined by the time constant of C and R externally connected. This pulse enters the GDC's LPEN terminal.

Receiving the signal, the GDC (μPD7220) computes the address of the location on the CRT and compares it with the contents of the light pen address register (LAD) of the GDC. If they are not equal, the address of the CRT location is moved to LAD. If they are equal, the light pen status flag (LPEN DETECT) is set to "1".

The CPU becomes ready to read data after it has detected that LPEN DETECT is "1".

In detection of a CRT location with the light pen, sensing is performed twice during two consecutive frame times, once per frame time. Then the coordinates detected are compared by hardware to prevent disturbance by any other light source e.g. room lighting.

Signal $\overline{\text{INTCR}}$ is the interrupt request signal which the light pen switch generates and sends to the CPU.

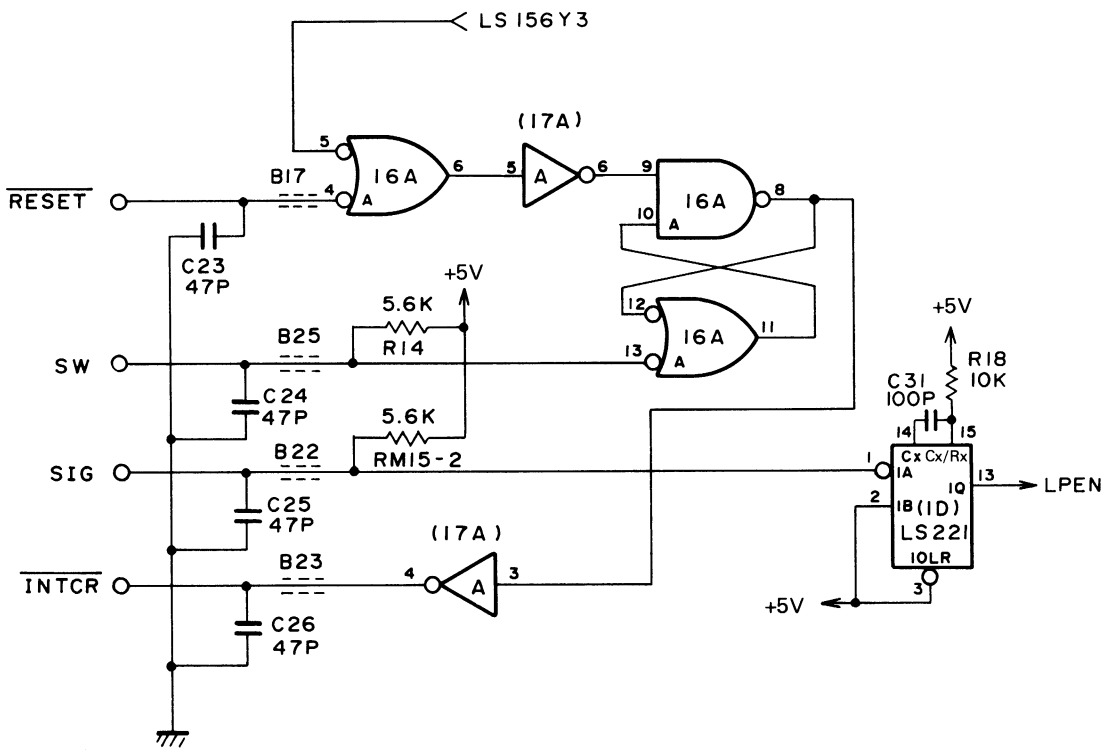


Fig. 5-16 Light pen signal input circuit

5.7 Memory Interface

5.7.1 Video RAM (V-RAM)

V-RAM consists of 16 D-RAM chips which are installed separately from the main card main memory and controlled directly by the GDC (μPD7220).

Eight address lines, A0 - A7, are connected to the D-RAM chips and addressing is performed in two cycles, with the most significant eight bits and the least significant eight bits separately. Signal $\overline{RAS}$ serves as the strobe signal for the least significant eight bits and signal $\overline{CAS}$ for the most significant eight bits.

The D-RAM capacity is 32 KB (with 16K x 1 bit Dynamic RAM used) for the ASCII type and 128 KB (with 64K x 16 bit Dynamic RAM used) for the HASCI type.

5.7.2 Basic cycles of the D-RAM

(1) Write cycle: At decay of $\overline{CAS}$ when $\overline{WE}$ is low level, the data which is currently supplied to the data input terminal DI is written into the D-RAM. The data output terminal DO remains floating at this time.

(2) Read cycle: At decay of $\overline{CAS}$ when only $\overline{WE}$ is high level, data is output to the data output terminal.

(3) Read/modify/write cycle: During this cycle, data is read out, modified, and written into the memory location where the data was stored originally. At this time, write operation is executed when $\overline{WE}$ turns to low level after data is developed at the data output terminal.

(4) Delayed write cycle: This is the same as the read/modify/write cycle but $\overline{WE}$ turns to low level earlier than in read/modify/write cycle and, therefore, write operation is executed before data develops at the data output terminal.

In this cycle, read/modify/write operation is not performed but ordinary write operation is executed. Data developing at the data output terminal is not used.

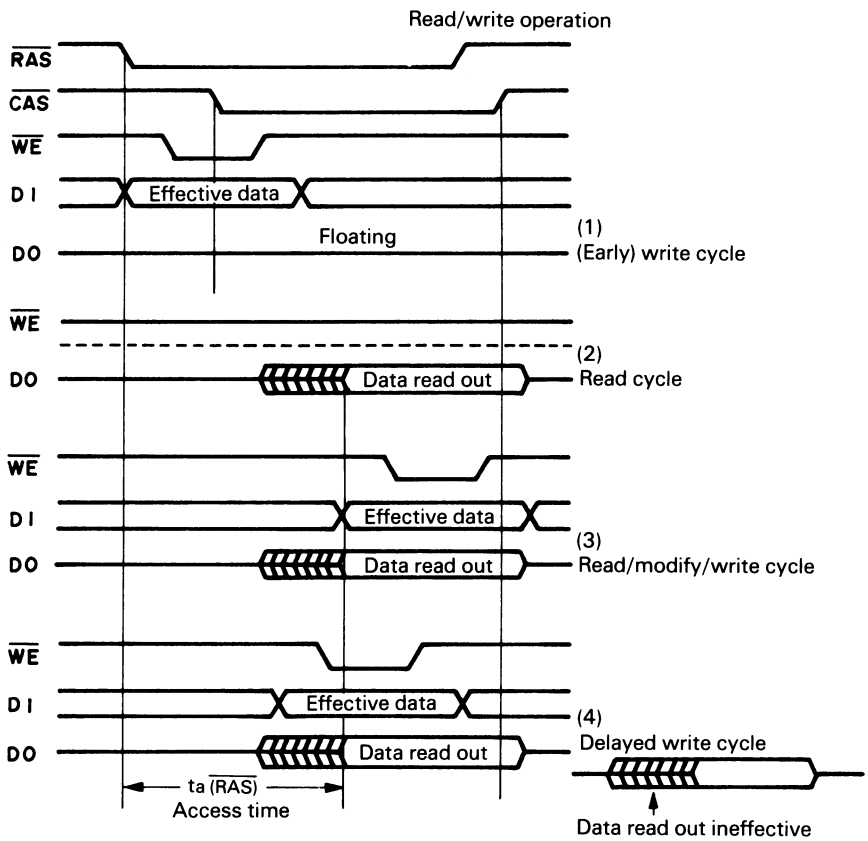


Fig. 5-17

5.7.3 Memory capacity and pages

(1) In graphic mode

In graphic mode, addresses are assigned to the locations on the CRT screen as shown in Fig. 5-18. The data associated with each location comprises 16 bits and the screen consists of 640 (vertical) by 400 (horizontal) locations called dots.

Data may be assigned to each dot in graphic mode. In full-graphic mode, the data of a screen, or of a "page", amounts to 640 x 400/16 = 16K word and, therefore, the V-RAM capacity is approximately four pages if it is 64K word.

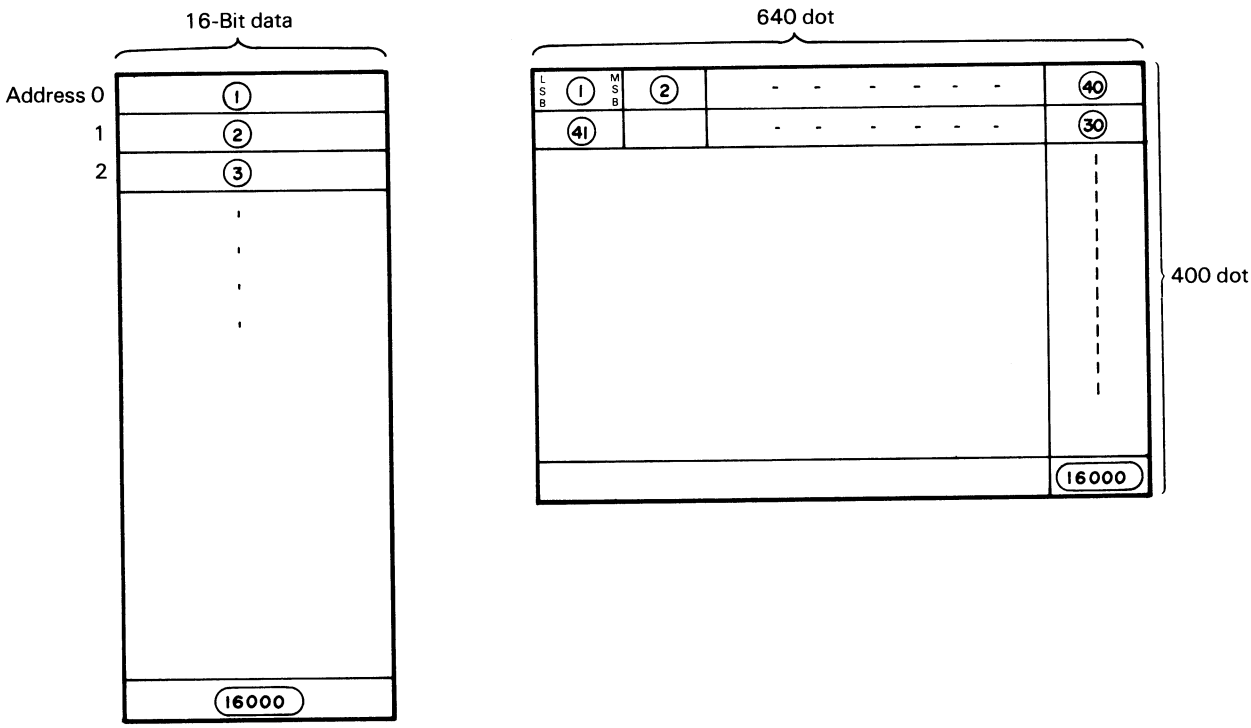


Fig. 5-18 Graphic data and memory map

(2) In character mode

In character mode, addresses are assigned to the locations on the CRT screen as shown in Fig. 5-19. Each character is composed of eight horizontal and 16 vertical dots and the whole screen may display 80 characters per line on 25 lines.

Compared with graphic mode, the number of independently addressable locations is twice as large horizontally and one-sixteenth as large vertically and, as a whole, one-eighth (2 × 1/16 = 1/8) as large. Therefore, the V-RAM capacity may be considered as 32 pages (4 pages × 8) if it is 64 KB.

Out of 16 bits of the data the GDC generates, the most significant eight bits serve as an attribute data whose function is summarized in Table 5-3.

The least significant eight bits designate an address in the character generator whose contents are to be displayed as a character.

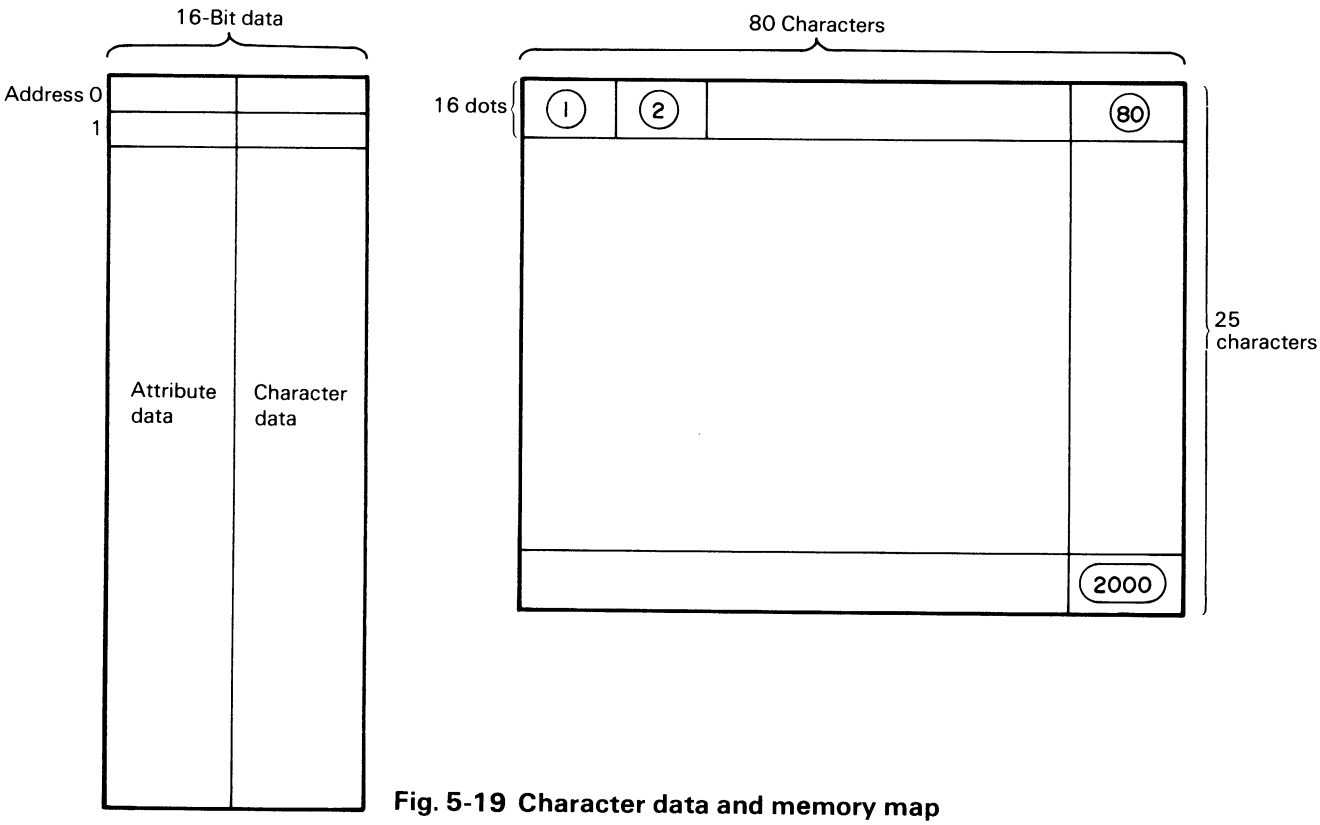


Fig. 5-19 Character data and memory map

Signal line	Signal name	Function
AD15	BLINK	BLINK
AD14	SECRET	INVISIBLE
AD11	RVS	REVERSE
AD10	HiLT	INTENSIFY

Table 5-3 Attributes

5.7.4 $\overline{RAS}$/$\overline{CAS}$ signal generator

Fig. 5-20 shows the circuit which supplies the D-RAM with signals $\overline{RAS}$ and $\overline{CAS}$. These signals are generated from the $\overline{RAS}$ (Row Address Strobe) signal of the GDC.

The J-K flip-flop ALS112 (12D) shifts $\overline{RAS}$ of the DGC to the trailing edge of 2CCLK to precharge RAS of the D-RAM.

$\overline{CAS}$ is generated by trailing $\overline{RAS}$ for 100 nsec and supplied to the D-RAM.

5.7.5 Address latch enabling/output control signal generating circuit

The $\overline{RAS}$ output by the GDC is used not only to supply the D-RAM with $\overline{RAS}$ and $\overline{CAS}$ but also to control the gates of address latches ALS573 (8C/9C).

The $\overline{RAS}$ output of the GDC is supplied directly to the ENABLE terminals of the address latches.

The input signals to the OUTPUT CONTROL terminals of ALS573 8C and 9C are basically the $\overline{RAS}$ signal supplied to the D-RAM but delayed for 40 nsec and inverted to opposite phases from each other.

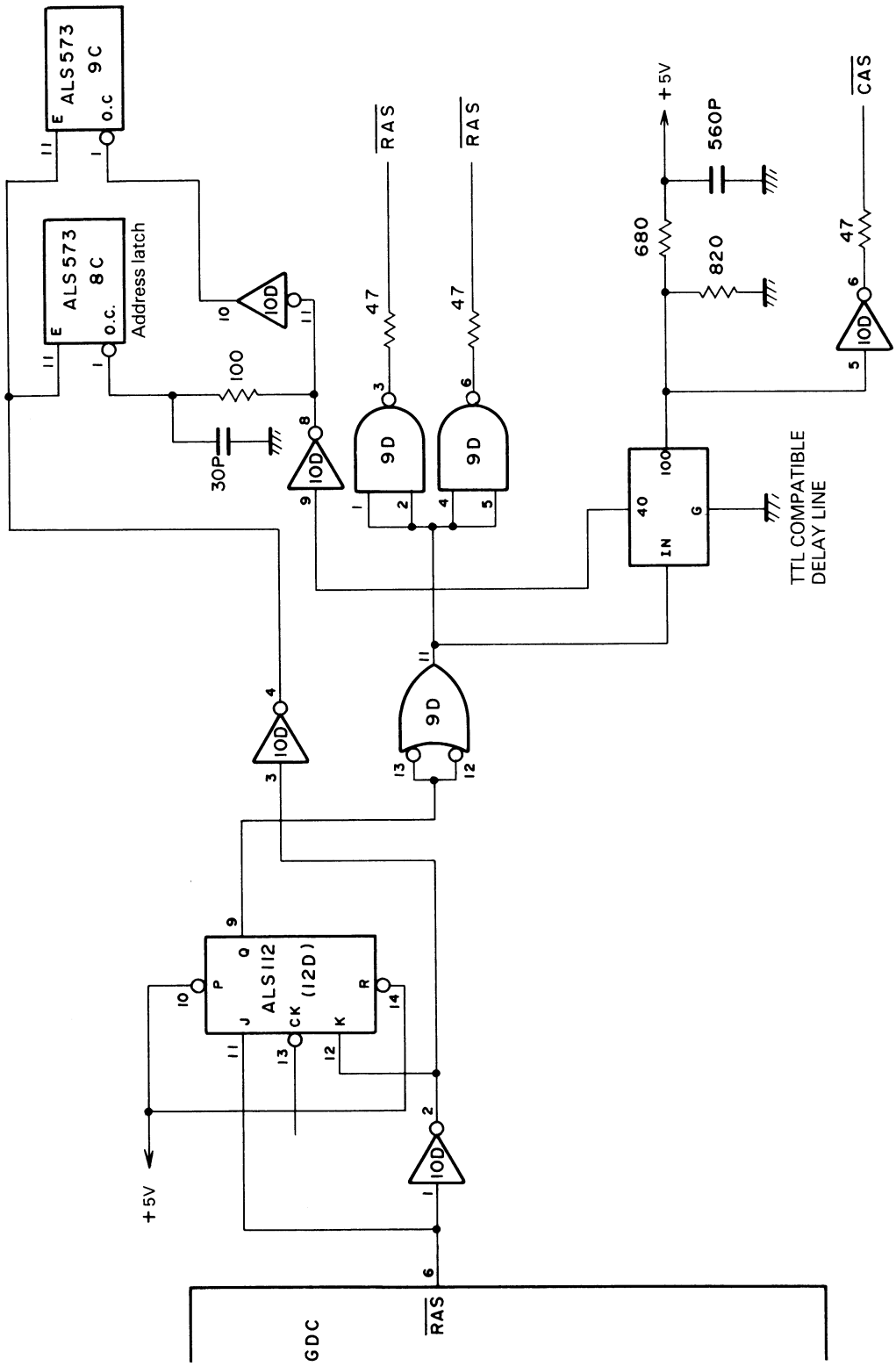


Fig. 5-20 $\overline{RAS}$/$\overline{CAS}$ signal generator and address latch enabling/output control signal genrating circuit

5.7.6 $\overline{\text{DBIN}}$ signal generator

Signal $\overline{\text{DBIN}}$ (Data Bus IN) is generated only during execution of read/modify/write (R/M/W) for V-RAM to put the V-RAM output onto its data bus.

$\overline{\text{DBIN}}$ of the GDC connects to terminals G1 and G2 of the 3-state buffers LS541 (1C and 7C).

That is the buffers output data when $\overline{\text{DBIN}}$ is active (input terminals G1 and G2 are at low level) so that the GDC can read the output data of the D-RAM.

5.7.7 $\overline{\text{WE}}$ signal generator

This circuit generates the $\overline{\text{WE}}$ (Write Enable) signal which is a trigger signal to write data in the D-RAM during draw (R/M/W) cycle.

$\overline{\text{WE}}$ is generated by the delay circuit (see Fig. 5-21) which delays $\overline{\text{DBIN}}$ coming from the GDC. $\overline{\text{DBIN}}$ is output when data are read out of V-RAM of the GDC. Two D flip-flops, LS374 (12C), timed by clock 2CCLK and LS574(7E), timed by DOT CLK, shift signal $\overline{\text{DBIN}}$ during E4 cycle when correction data are generated, generating $\overline{\text{WE}}$ which is delivered to the $\overline{\text{WE}}$ input terminals of the D-RAM.

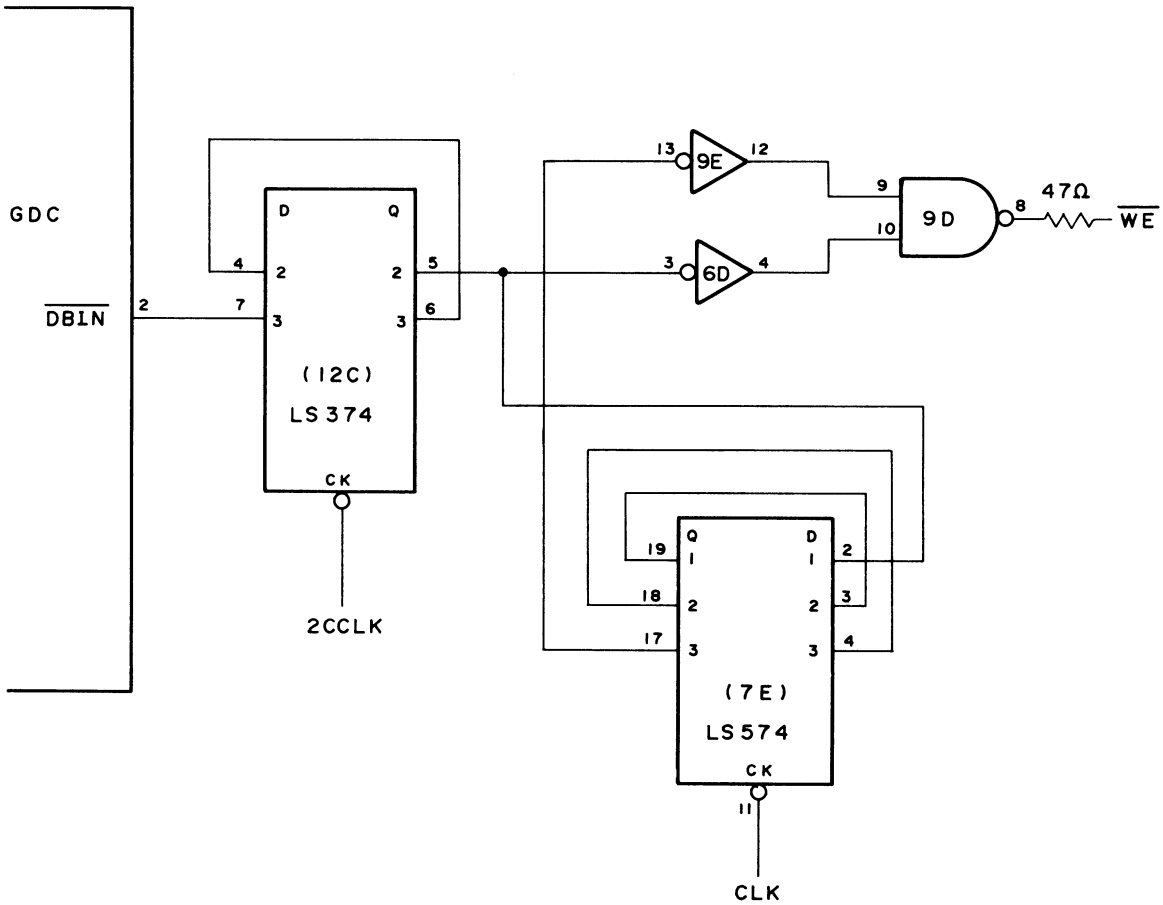


Fig. 5-21 $\overline{\text{WE}}$ signal generator

5.8 Video Signal Output Circuit

5.8.1 General

Picture data written in V-RAM are read out during the display cycle and supplied via the video signal output circuit to the CRT drive unit (CDU) as video signals.

The video signal output circuit operates as described below in a specific mode.

(1) In graphic mode

Sixteen-bit data output from V-RAM is first held in latches (D flip-flops) LS374 (2C and 6C), then enters D flip-flops LS374 (3C and 5C). Output pins 8 and 6 of NAND gate 13D are connected respectively to the OUTPUT CONTROL terminals of these flip-flops.

One input to each of the two NAND gates is the CSR-IMAGE signal which is high level during graphic mode. The other input to pin 4 is the Q output of D flip-flop LS74(14D) and that to pin 9 is the $\overline{Q}$ output.

LS74(17D) is timed by the clock signal which is the inversion of $\overline{RAS}$ supplied to V-RAM so that the data output from V-RAM are output, with its most significant eight bits and least significant eight bits separated, from latches LS374 (3C and 5C), and synchronized with addressing according to signal $\overline{RAS}$.

(2) In character mode

Signal CSR-IMAGE coming from the GDC is low level during character mode and, as a result, output of pins 6 and 8 of NAND gate 13D is high level, putting the OUTPUT CONTROL terminals of data latches LS374 (3C and 5C) to high level and inhibiting them from outputting data.

On the other hand, the OUTPUT ENABLE terminal of the character generator becomes active when CSR-IMAGE is low level. Now the data output from V-RAM enters data latches LS374 (2C and 6C) from where the least significant eight bits enter the character generator (2E). Its output, in turn enters a shift register for parallel-to-serial conversion.

The most significant eight bits of the V-RAM output data (which include a 4-bit attribute data) enters D flip-flop ALS574(6E) and then goes to an attribute logic.

(3) In graphic-character mixed mode

The μPD7220 permits mixture of graphic and character modes on the same screen. In this case, the screen is divided into upper and lower sections, and graphic and character modes work in either of the two sections. (Fig. 5-22)

In graphic-character mixed mode, graphic and character data are output as described above. That is, data latches LS374 (3C and 5C) work for graphic data and the character generator (2E) and attribute generator work for character data.

It might happen that, when the upper section of the screen is in graphic mode, characters in the lower character mode section do not appear wholly but only partly, as shown in Fig. 5-23.

However, this does not actually happen because the Q10 GMS resets the line counter with a reset signal which the one-shot LS221(1D) generates from the NAND output of the inversion of the GDC's output $\overline{AT.\ BLINK}$ - $\overline{CLC}$ with H. SYNC. Thus the line counter is reset at the end of the graphic mode section and it restarts counting line at the beginning of the character mode section.

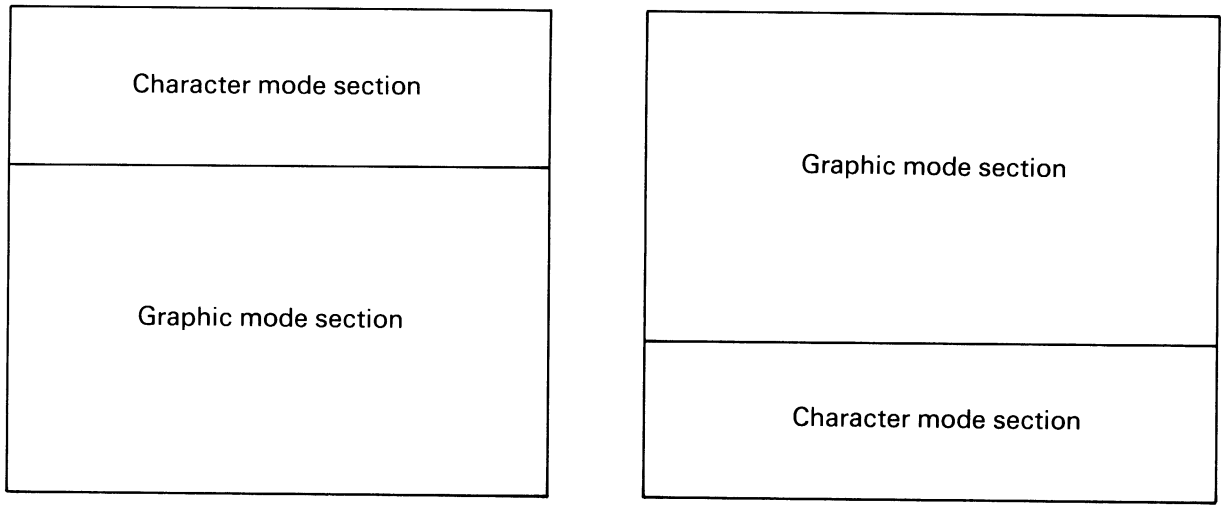
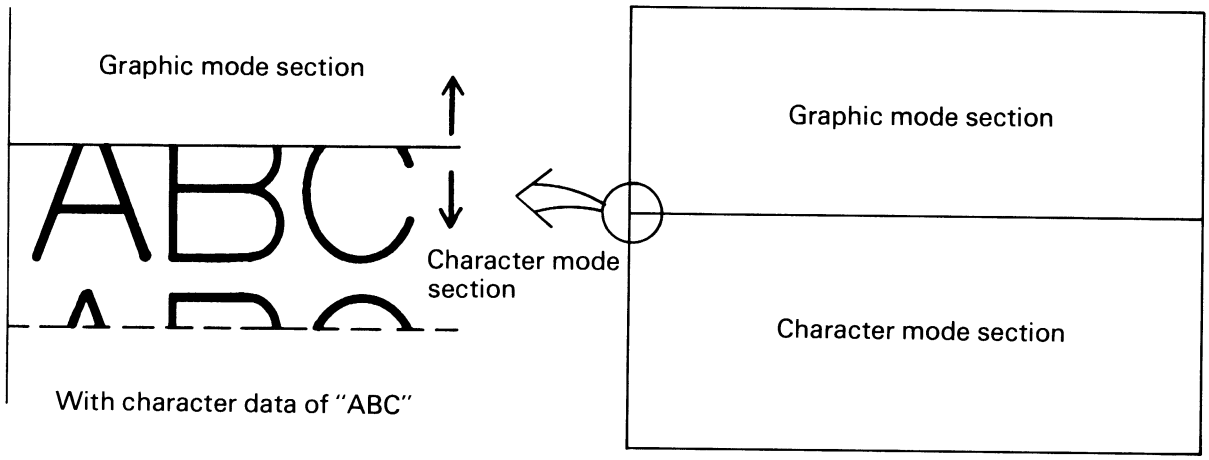


Fig. 5-22 Graphic-character mixed mode



If the first horizontal dot count where the character mode area starts is not an integer multiple of 16, characters might disintegrate unless the line counter is reset at the beginning of the character mode area.

As line counter reset is automatically done at any occation, user don't need to be bother with it.

Fig. 5-23

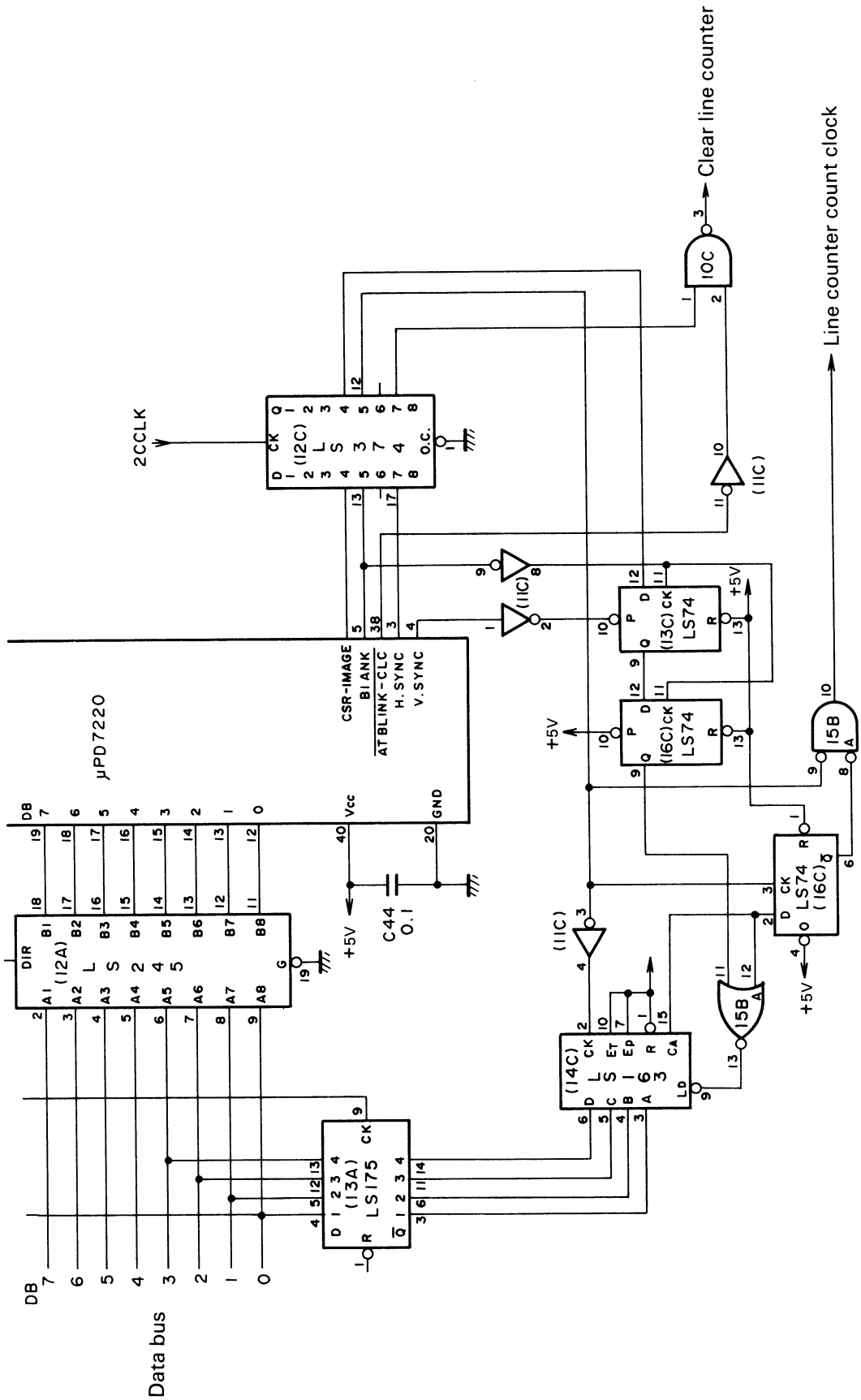


Fig. 5-24 Clock generator for the line counter operating in graphic-character mixed mode

5.8.2 Line counter

In character mode, the charachter data read out of V-RAM are actually addresses (A4 - A11) (A4 – A12, in use of 2764) of memory locations of the character generator (2E) which hold the dot pattern data of characters.

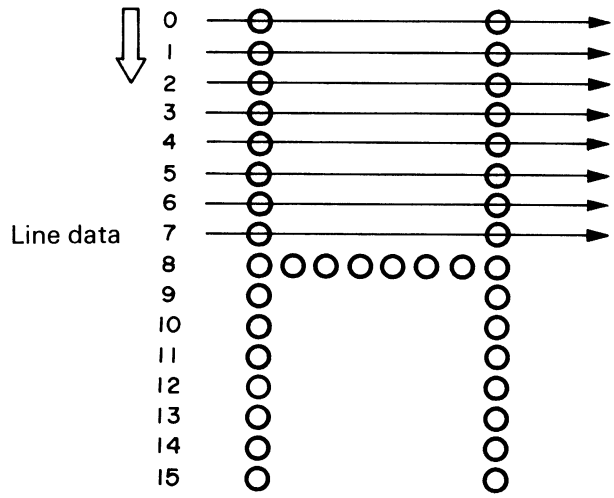
In the CRT, every horizontal scanning covers a vertical width as large as a dot and, therefore, it is necessary to count the line number of the character generator at every scanning.

The circuit shown in Fig. 5-25 performs this function. First, gate 10C NANDs H. SYNC with $\overline{\text{AT. BLINK}}$ $\overline{\text{-CLC}}$ and the output triggers the one-shot 2A to genrate a pulse, whose width is determined by external C40 and R19 at $\overline{2Q}$, so that the line counter LS161 (1E) gets reset. Next, character data are output from V-RAM.

The data giving line counter inputs are always high level because input A, B, C and D of LS161 (1E) is pulled-up to +5V.

, the line counter LS161 operates, controlled by a clock timed with the horizontal sync signal, to send line data to address A0 – A3 of the character generator from outputs QA - QD.

The character generator combines address data A0 – A3 with data of A4 – A11 and retrieves character data of line.



A 0 1 2 3	4 5 6 7 8 9 10 11
Line data	Character data
Repeats counting from 0H to FH. Dot data of characters of every line are obtained by varying this data on every scanning.	These are the codes of characters to be displayed.
Receiving address of A0 – A11, the character generator outputs the data held in the designated location.	

Fig. 5-24

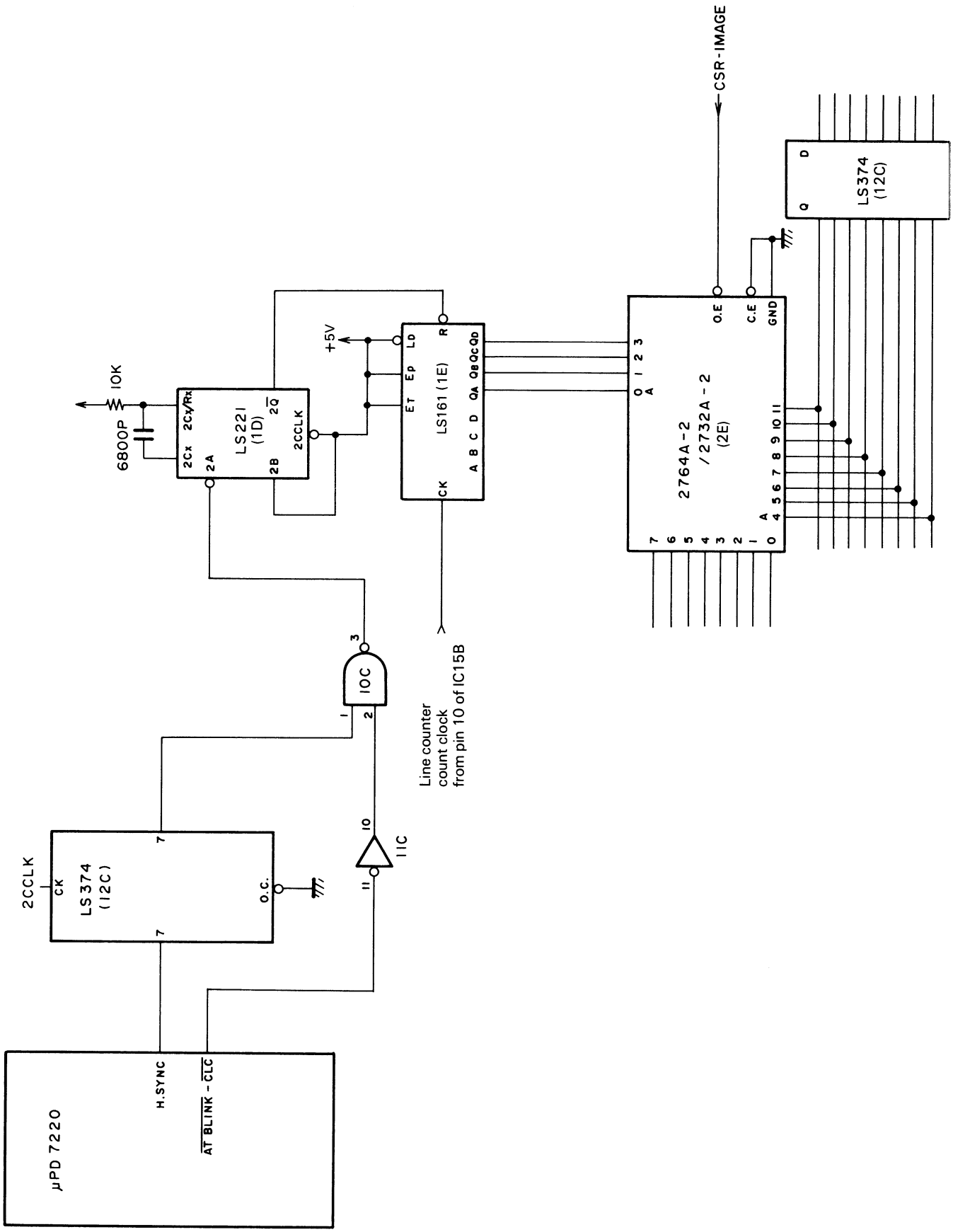


Fig. 5-25 Clear line counter generator

5.8.3 Blanking signal

The blanking signal is output from the BLANK signal terminal of the GDC to blank out retrace lines in any of the following conditions.

(1) During horizontal or vertical retrace time

(2) From execution of a display stop command such as RESET and STOP until execution of a START command

(3) During execution of R/M/W for V-RAM

Fig. 5-26 shows the circuits to which signal BLANK is supplied from the GDC. The BLANK signal is output from the BLANK signal terminal of the GDC and passes D flip-flop LS374(12C) over to terminal 2D of another D flip-flop LS175(15D). Output $2\overline{Q}$ of LS175(15D) is further delayed by two dot clocks by LS175(8D), and is output from 2Q of LS875(8D). This goes into ALS40(10E) of the last ladder of attribute logic. Also the video signal which has passed attribute logic is input to another input terminal of ALS40(10E). Thus, AND of these signals is ultimately made, and provided to the CDU. According to the situation of BLANK signal, the video signal will be output or stopped.

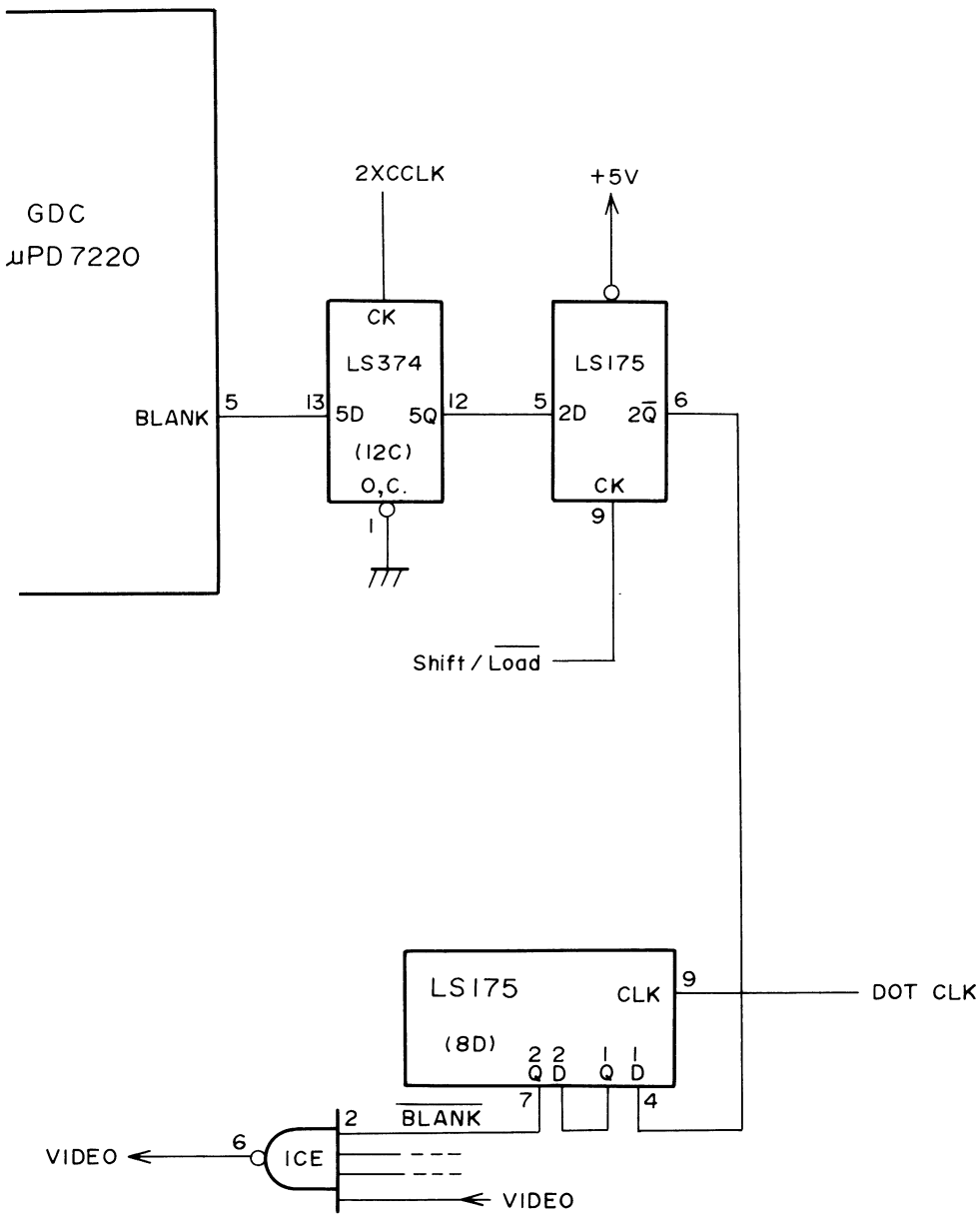


Fig. 5-26 Circuits of the BLANK signal

5.8.4 CSR-IMAGE signal

CSR means cursor and IMAGE graphic mode. These signals which are active at high level are output by time division.

The CSR signal remains output during the horizontal scanning time (one raster time). The IMAGE signal is output when the BLANK signal is output (during retrace blanking time).

If signal IMAGE is high level at the beginning of horizontal scanning when signal BLANK is output together, graphic mode is selected during the horizontal scanning time and the OE (Output Enable) terminal of the character generator does not become active.

At this time, the IMAGE signal turns the OUTPUT CONTROL signal of another D flip-flop LS374 (3C or 5C) to active, so that graphic mode is entered.

If the IMAGE signal is low level while the BLANK signal is output, character mode is selected during the horizontal scanning time and the signal turns terminal OE of the character generator 2732(2E) to active and, at the same time, the OUTPUT CONTROL terminals of D flip-flops LS374 (3C and 5C) to high level As a result, video data enters the shift register via the character generator.

5.9 Attribute Data Generator

The attribute data generator genrates VIDEO signal of the CRT by adding attribute data to VIDEO signal of character data.

First, the VIDEO signal enters pin 1 of NAND gate IC7D. The other input to the gate is the $\overline{\text{SECRET}}$ signal and, when it is low and active, the VIDEO signal is not output to the CRT. So, the character become invisible.

The $\overline{\text{SECRET}}$ signal is normally high level and, therefore, the output at pin 3 of IC7D is low level. This signal then enters pin 5 of OR gate IC7D. The other input to the gate is the CSR signal output through pin 11 of IC7D. This signal is low level when CSR appears and high level otherwise. The OR gate ORs the VIDEO and CSR signals to determine whether or not to display the cursor.

The output at pin 6 of IC7D is high level when there are display data and, therefore, the input to pin 13 of the subsequent EX-OR gate IC16B is also high level. The other input to this gate is the $\overline{\text{RVS}}$ signal, which is EX-ORed with the VIDEO signal to determine whether or not to reverse the image. The BLINK signal which designates image blinking is supplied from pin 8 of IC7D.

The $\overline{\text{BLINK}}$ signal coming to pin 9 of IC9E is an attribute data associated with a character data, but the $\overline{\text{AT-BLINK}}$ signal alternates between high and low levels for every screens to make the image appear as if it were blinking. The blinking signal is generated by NANDing these signals.

The BLANK signal further enters pin 2 of IC10E. This signal is low level and the screen becomes blank The VIDEO signal passes through the gates as explained above and enters the CDU (CRT drive unit) as the VIDEO signal of the CRT.

The HILT (High Light) signal which intensified characters is generated by varying the voltage level which resistors R5 and R6 generate by dividing the level of the VIDEO signal obtained above.

The level of the VIDEO signal is 0 – 4V in normal mode and 0 – 5V in highlight mode.

All attribute data pass through a certain number of gates and synchronization is obtained at the time of output.

RVS	Reverse
CSR	Cusor
SECRET	Secret (Invisible)
BLINK	Blink
AT-BLINK	Attribute blink
BLANK	Blank
HILT	High light (Intensify)

Table 5-4 Attribute data

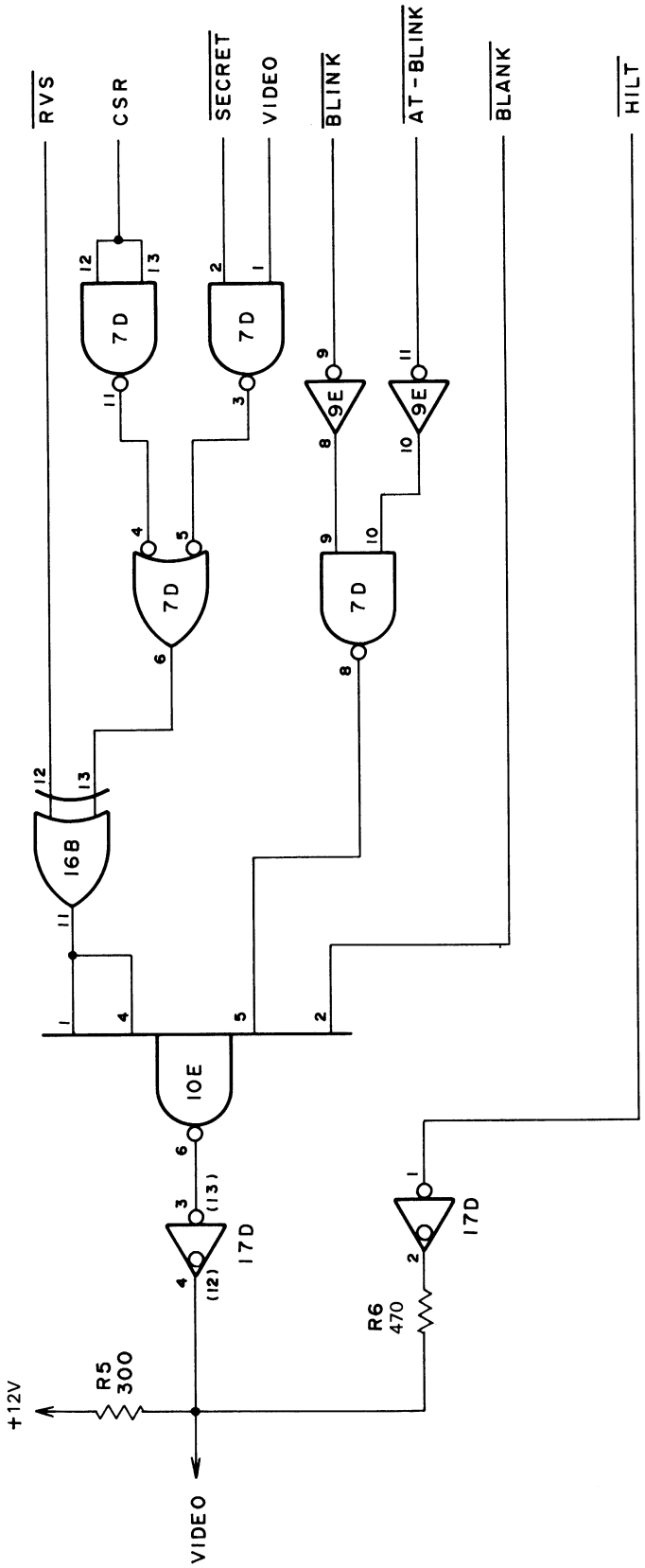


Fig. 5-27 ATTRIBUTE LOGIC CIRCUIT

5.10 Magnified Display (draw) Circuit

5.10.1 Timing diagram

It is possible to display characters and graphic figures which are magnified as many times as an integer multiple of 1 to 16. In this mode, display addresses are generated as shown in Fig. 5-5.

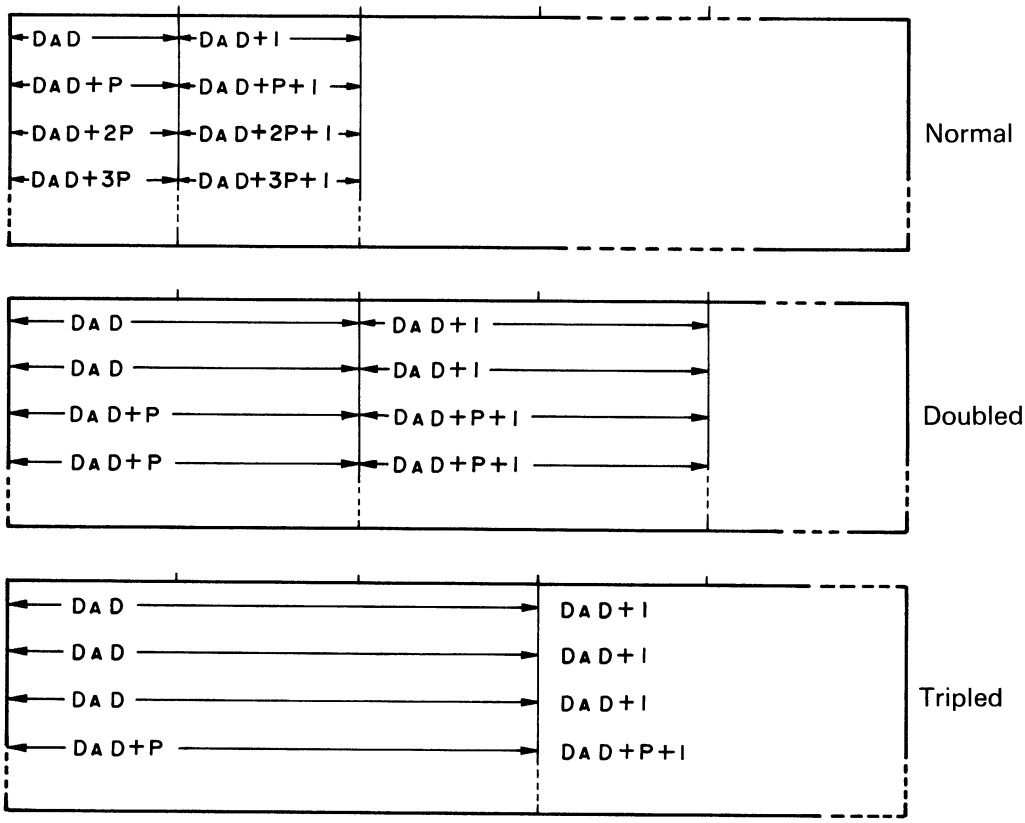


Table 5-5

Horizontal display address cycle is changed according to the magnification factor designated.

As shown in Fig. 5-28, the cycle of two clock signals (2CCLK) normally becomes four clock signals (2 × 2CCLK) during double-magnification time and six clock signals (3 × 2CCLK) during triple-magnification time.

At this time, output $\overline{RAS}$ rises to high level in magnified areas as shown in Fig. 5-28 to help the shift register, which generates serial video signals from V-RAM outputs, select timing of load clock generation.

In the vertical direction, line count is changed to display the same data.

Thus the GDC controls display address in units of word during magnified mode.

The circuit (see Fig. 5-29) working in magnified mode generates load and shift clocks and supplies the shift register with them.

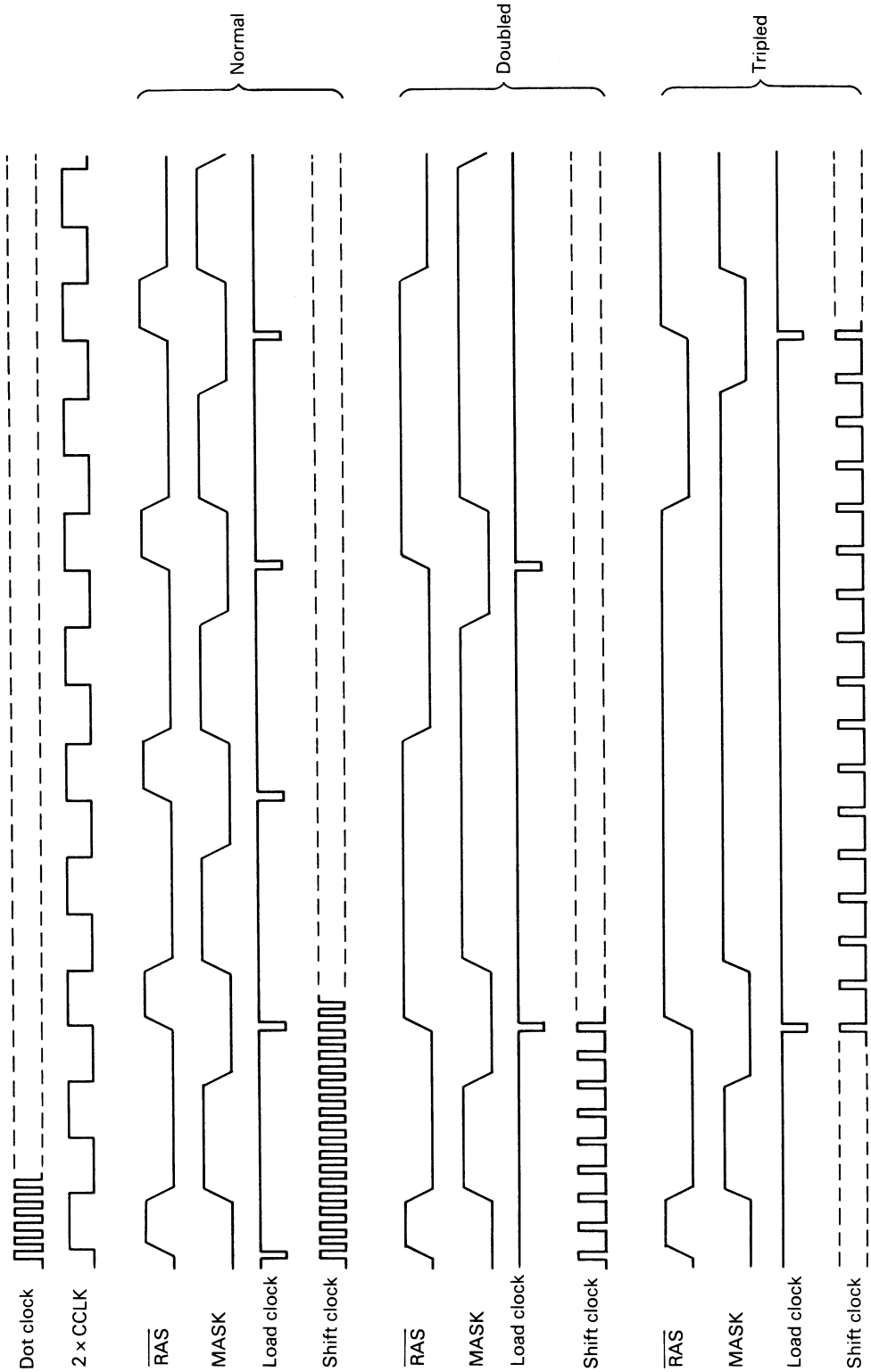

Normal
Doubled
Tripled
Dot clock
2 x CCLK
RAS
MASK
Load clock
Shift clock
RAS
MASK
Load clock
Shift clock
RAS
MASK
Load clock
Shift clock

Fig. 5-28

5.10.2 Magnified Display Circuit

To display magnified data, it is necessary to vary the periods of the load and shift clock signals, which are supplied to the shift register, according to the magnification factor.

Display address is controlled by the GDC according to the magnification factor.

When a ZOOM command (46H) comes from the CPU, the GDC enters magnified display (draw) mode. Then the magnification factor is set as a parameter in the least significant four bits of the data bus. (See Table 5-6)

Data	Magnification factor
0000	1
0001	2
0010	3
.	.
.	.
.	.
.	.
1101	14
1110	15
1111	16

Table 5-6 Magnification parameter

The data bus lines of the least significant four bits are connected to D flip-flop LS175(13A) and its $\overline{Q}$ outputs enter counter S161(13B) and LS163(14C).

When the magnification factor is two, for example, the parameter set in the data bus lines of the least significant four bits is "0001" and, therefore, the data entering the data input terminals of the counter S161(13B) and LS163(14C) is Q_D Q_C Q_B Q_A = 1110. S161(13B) operates, timed by dot clock of the GDC. Since the input data is now "1110", the subsequent clock signal triggers a pulse to develop at the RIPPLE-CARRY OUTPUT terminal and this pulse enters pin 3 of the subsequent NOR gate IC 15B.

The other input to the NOR gate (15B) is the inversion of the shift load signal of the shift register of the video signal. The ORed output of these signals returns to the LOAD terminal of S161(13B).

This signal is routed via inverter 14E to pin 1 of IC13E and, after NANDed with the dot clock supplied to pin 2, exits through pin 3 to shift register (5D and 5E) as shift clock.

Thus, when the magnification factor is two, the shift clock frequency is halved so that image size is doubled.

LS163(14C) generates clock signal for the line counter of the character generator during character ZOOM mode. Like S161(13B), it generates RIPPLE CARRY OUTPUT signal according to the magnification factor. To the LOAD input terminal of LS163(14C), the NANDed result of output C_A of LS163 and output Q of LS74(16C) generated according to CSR-IMAGE is supplied. This signal resets the LS163(14C) when its own C_A output is present or graphic mode is changed to character mode on the same screen, and counts up for every horizontal scanning. Signal C_A enters D flip-flop LS74(16C), whose output $\overline{Q}$ in turn enters pin 8 of IC15B. On the other hand, NANDed with BLANK signal, the output at pin 10 of IC15B becomes the clock signal of line counter LS161(1E). Thus, clock frequency controlled according to the magnification factor is supplied to LS161(1E) so that characters appear magnified in magnified display mode.

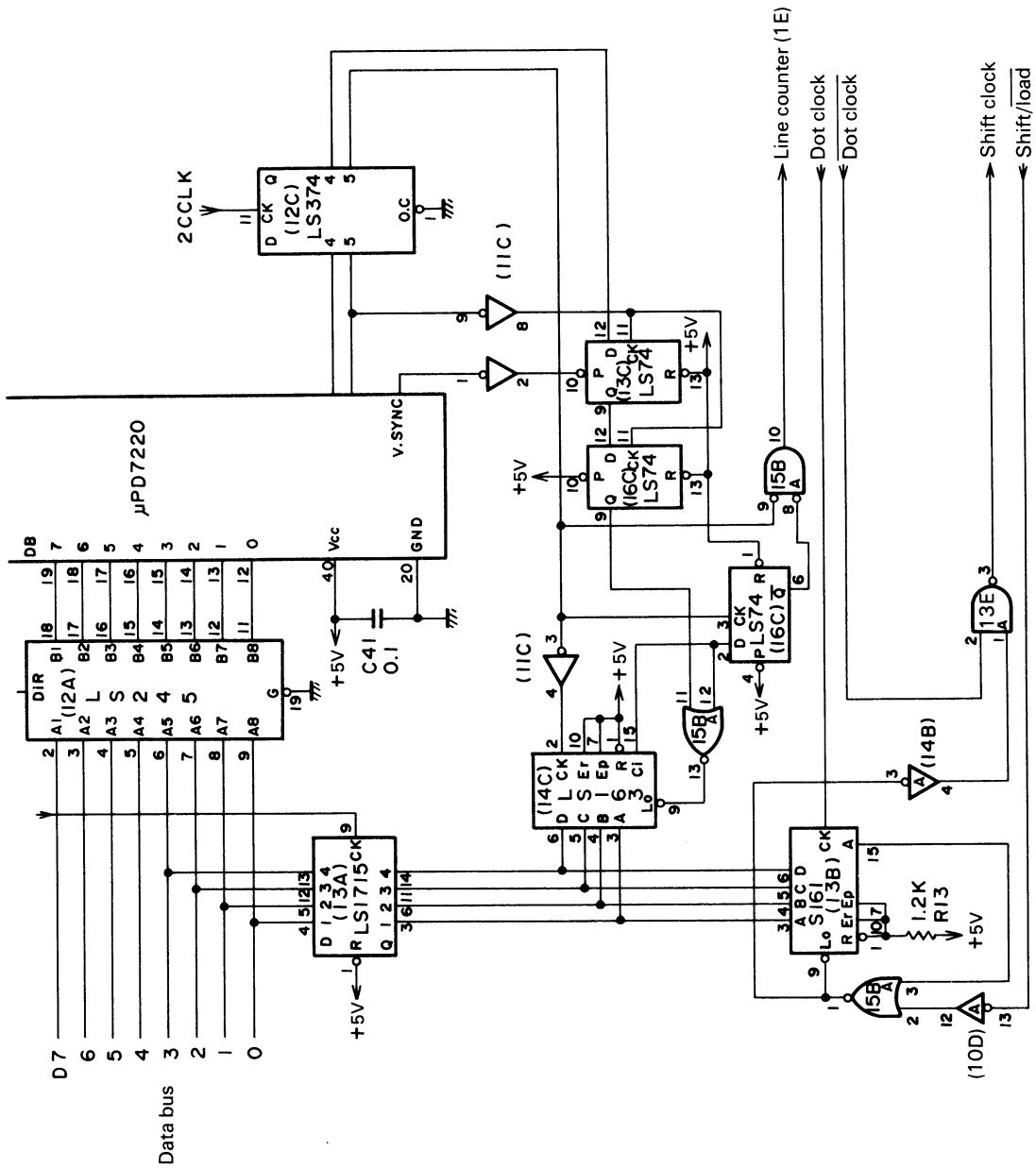


Fig. 5-29 Magnified display circuit

5.11 Sync Signal Generator

The μPD7220 generates the vertical and horizontal sync signals for the CRT.

Fig. 5-30 shows the circuit through which the sync signals are supplied to the CRT. These signals are output at the same timing as the address and cursor signals of V-RAM and routed through a latch circuit (D flip-flop) to normalize the jitter at the output to the CRT.

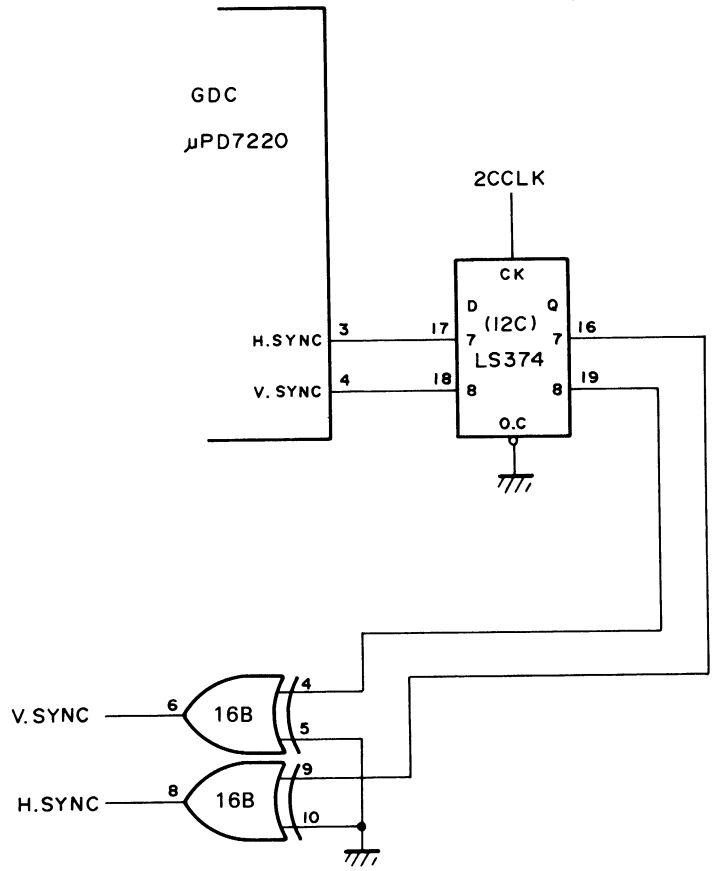
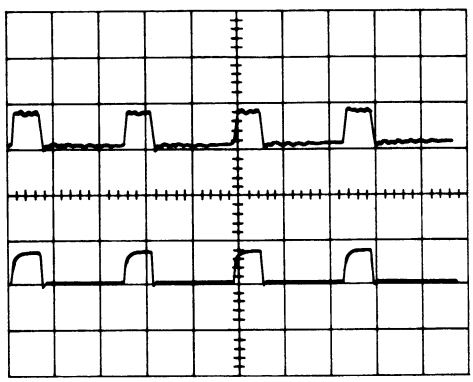
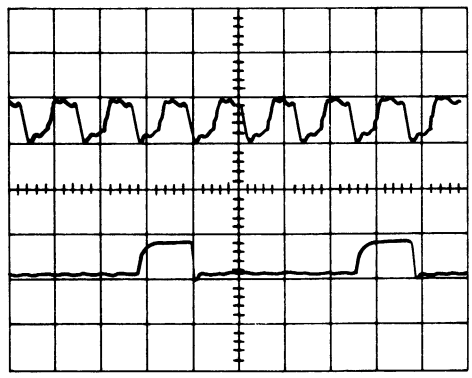


Fig.5-30 Circuit of sync signal



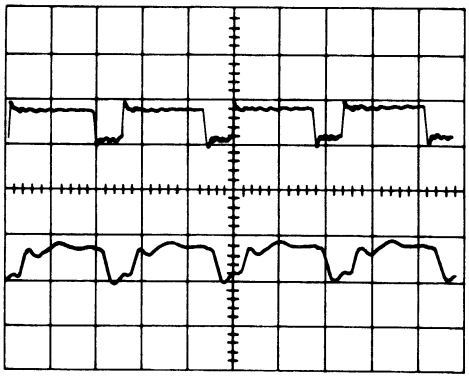
Upper: $\overline{RAS}$
Lower: IC12D (pin 9)
(Sweep 0.2 μsec 5V/div)

Fig. 5-31



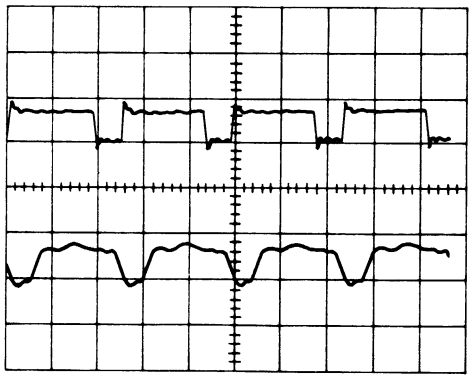
Upper: IC12D (pin 13)
Lower: IC12D (pin 9)
(Sweep 0.1 μsec 5V/div)

Fig. 5-32



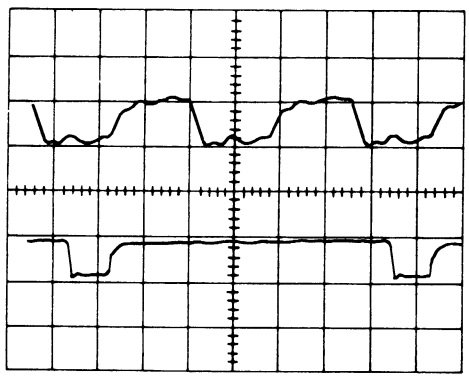
Upper: IC9D (pin 11)
Lower: IC10D (pin 9)
(Sweep 0.2 μsec 5V/div)

Fig. 5-33



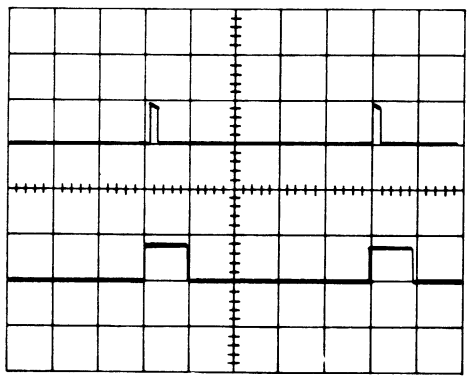
Upper: IC9D (pin 11)
Lower: IC10D (pin 5)
(Sweep 0.2 μsec 5V/div)

Fig. 5-34



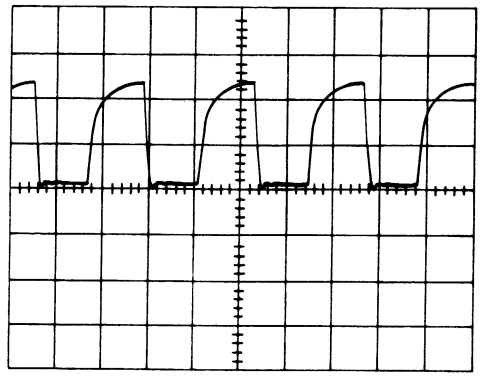
Normal
Upper: 2CCLK
Lower: S/L
Sweep 0.2 μsec 5V/div

Fig. 5-35



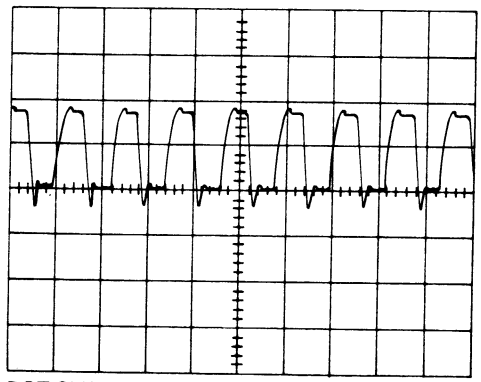
Upper: H.SYNC
Lower: BLANK
(Sweep 10 μsec 5V/div)

Fig. 5-36



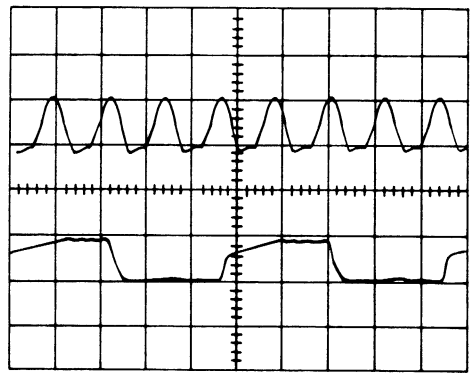
2CCLK
(Sweep 0.1 μsec 5V/div)

Fig. 5-37



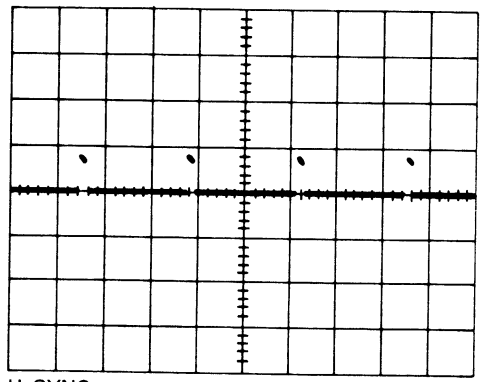
DOT CLK
(Sweep 50 nsec 2V/div)

Fig. 5-38



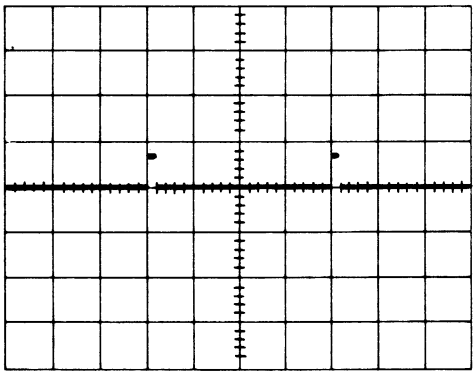
Upper: DOT CLK
Lower: 2CCLK
(Sweep 50 nsec 5V/div)

Fig. 5-39



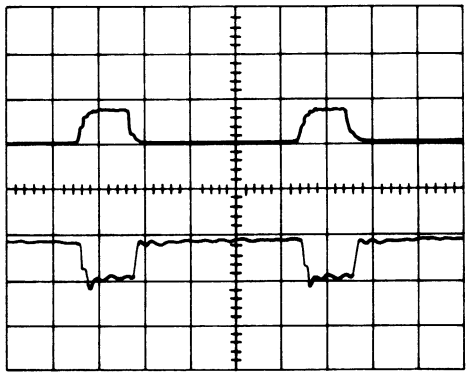
H. SYNC
(Sweep 20 μsec 5V/div)

Fig. 5-40



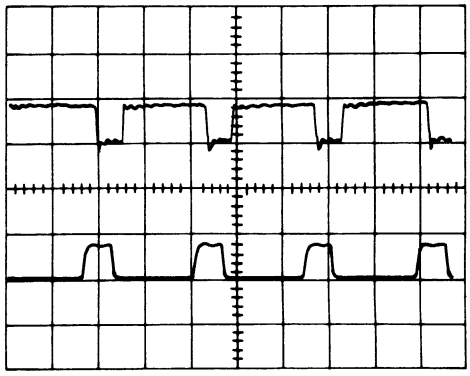
V. SYNC
(Sweep 2 nsec 5V/div)

Fig. 5-41



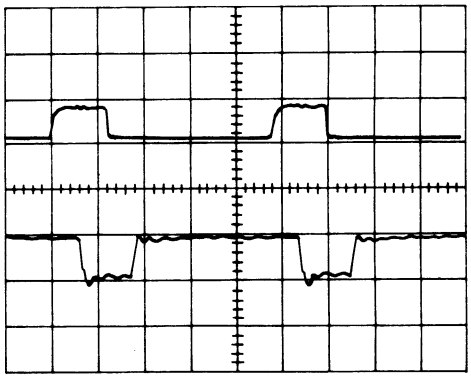
Upper: IC8C (pin 1)
Lower: IC9C (pin 1)
(Sweep 0.1 μsec 5V/div)

Fig. 5-42



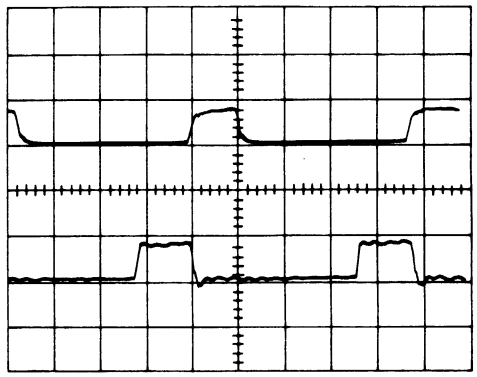
Upper: IC9C (pin 1) O.C
Lower : RAS
(Sweep 0.2 μsec 5V/div)

Fig. 5-43



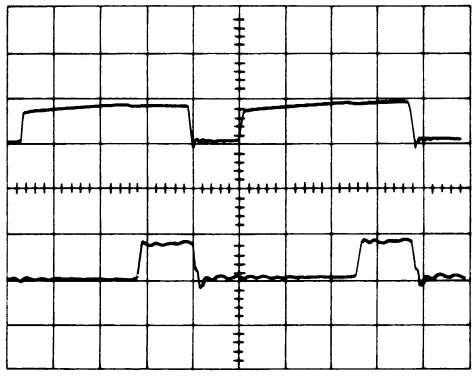
Upper: RAS
Lower: IC9C (pin 1) O.C
(Sweep 0.1 μsec 5V/div)

Fig. 5-44



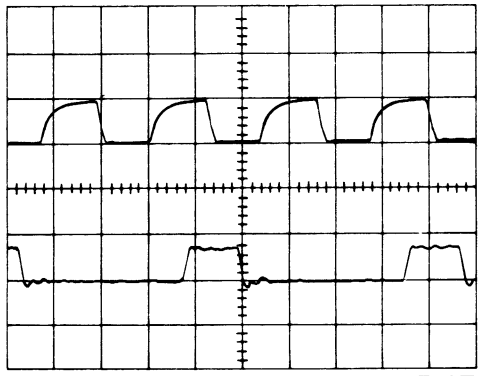
Upper: IC8C (pin 1) O.C
Lower: IC8C (pin 11) ENABLE
(Sweep 0.1 μsec 5V/div)

Fig. 5-45



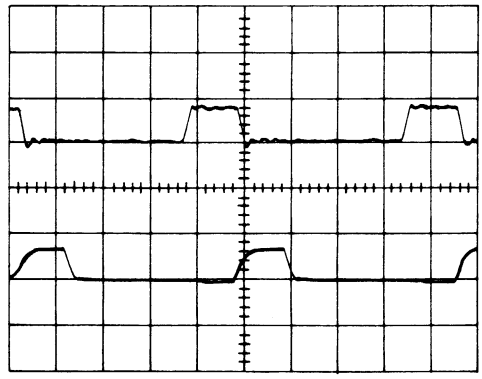
Upper: IC9C (pin 1) O.C
Lower: IC9C (pin 11) ENABLE
(Sweep 0.1 μsec 5V/div)

Fig. 5-46



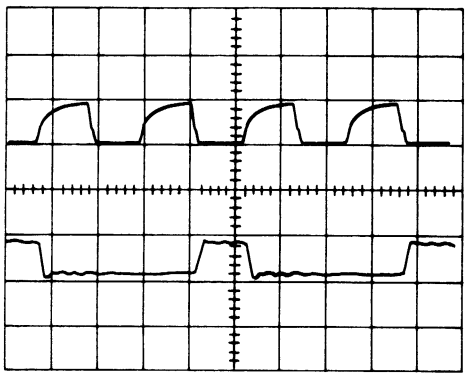
Upper: 2CCLK
Lower: RAS
(Sweep 0.1 nssec 5V/div)

Fig. 5-47



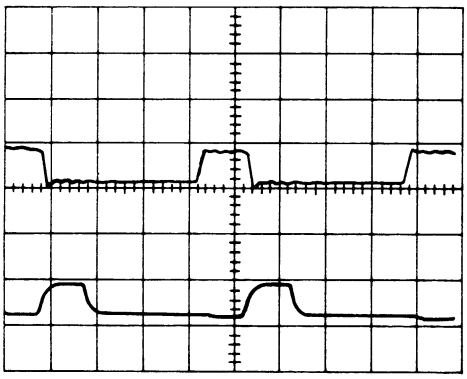
Upper: RAS
Lower: CAS
(Sweep 0.1 μsec 5V/div)

Fig. 5-48



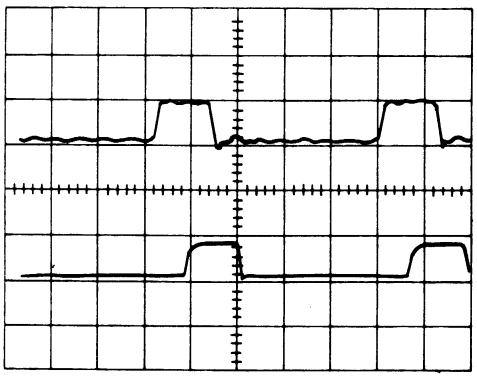
Upper: 2CCLK
Lower: RAS
(Sweep 0.1 μsec 5V/div)

Fig. 5-49



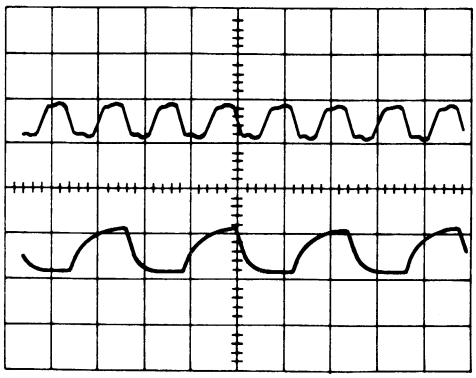
Upper: RAS
Lower: CAS
(Sweep 0.1 μsec 5V/div)

Fig. 5-50



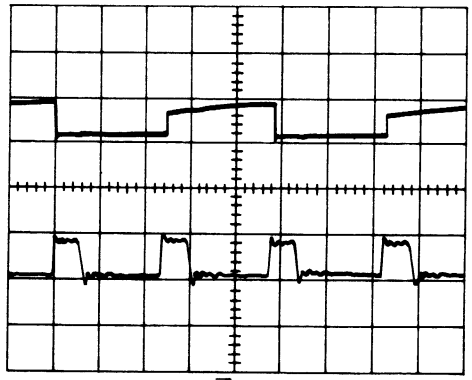
Upper: IC12D (pin 11) J
Lower: IC12D (pin 9) Q
(Sweep 0.1 μsec 5V/div)

Fig. 5-51



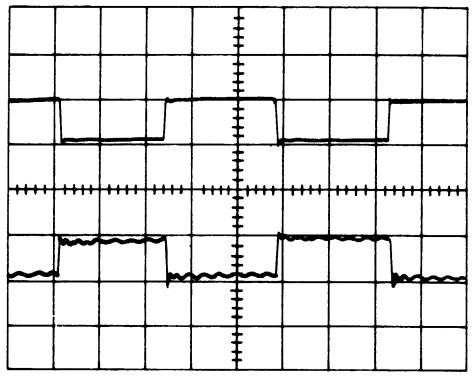
Upper: IC12D (pin 1) CK
Lower: IC12D (pin 5) 2CCLK
(Sweep 0.1 μsec 5V/div)

Fig. 5-52



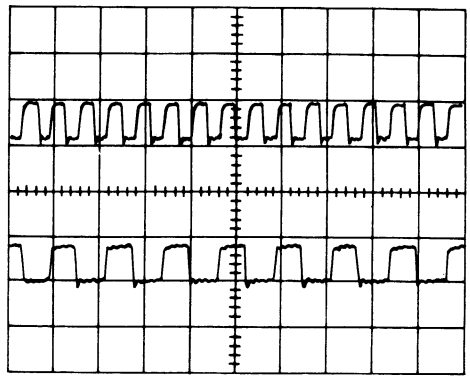
Lower: IC14D (pin 8) $\overline{Q}$
Lower: IC14D (pin 11) CK
(Sweep 0.2 μsec 5V/div)

Fig. 5-53



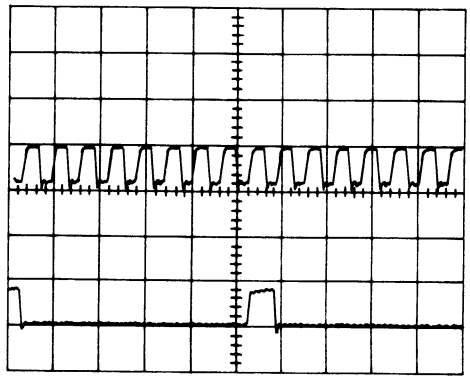
OUTPUT CONTROL
Upper: IC3C (pin 1)
Lower: IC5C (pin 1)
(Sweep 0.2 μsec 5V/div)

Fig. 5-54



ZOOM (× 2)
Upper: IC13E (pin 2)
Lower: IC13E (pin 1)
(Sweep 0.1 μsec 5V/div)

Fig. 5-55



ZOOM (×8)
Upper: IC13E (pin 2)
Lower: IC13E (pin 1)
(Sweep 0.1 μsec 5V/div)

Fig. 5-56