PRINCIPLES OF OPERATION

2

CHAPTER

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2.1 SYSTEM OVERVIEW (Figure 2-1)

The interconnection of the main CPU unit, floppy disk drives, keyboard, and monitor is diagrammed below and summarized in Table 2-1. Pin assignment for each connector is detailed in Tables 2-2 through 2-16.

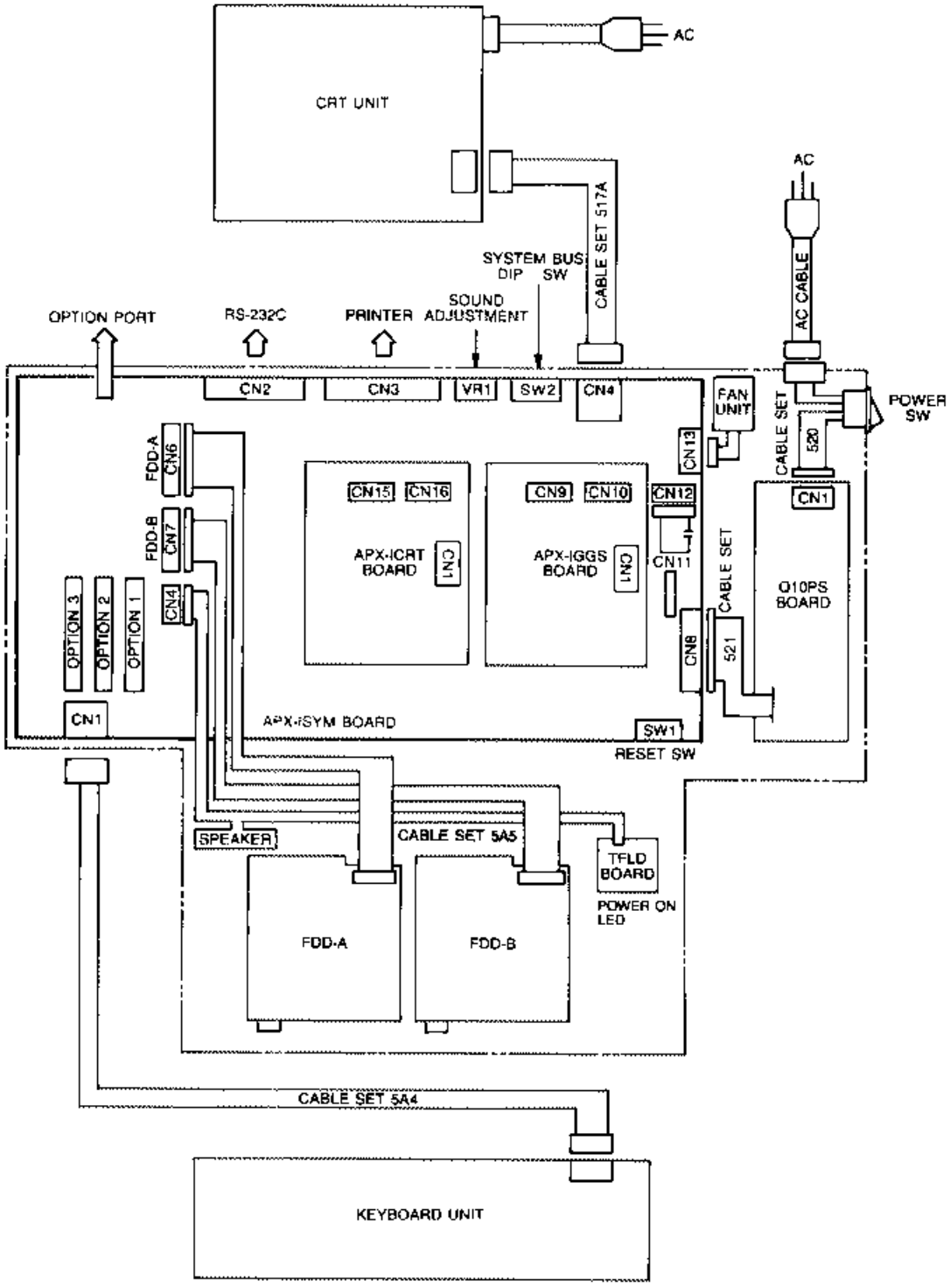

FIGURE 2-1. SYSTEM CONFIGURATION BLOCK DIAGRAM

TABLE 2-1. CONNECTOR SUMMARY

CONNECTOR	TYPE	DESCRIPTION	REFERENCE
CN1	DIN, 8-pin, TC4480	Keyboard port	Table 2-1
CN2	Cannon, 25-pin, GMM-25HUFDA	RS-232C port	Table 2-2
CN3	Honda, 36-pin, ADS-36BLFD	Parallel printer port	Table 2-3
CN4	DIN, 8-pin, TC4480	CRT unit	Table 2-4
CN5	————	NC (unused)	————
CN6	3M, 34-pin, 3463-0001	FDD-A (left drive)	Table 2-5
CN7	3M, 34-pin, 3464-0001	FDD-B (right drive)	Table 2-5
CN8	13-pin, 5271-6A	Power supply to APX-ISYM	Table 2-6
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Option slots #1 - #3	60 pin DDK225D-10030C2-23	Option card connectors	Table 2-15

TABLE 2-2. CN1 PIN ASSIGNMENT (Main unit to keyboard)

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	RXD	OUT	Received data
2	CLK	OUT	Clock
3	+12	OUT	+12V
4	TXD	IN	Transmitted data
5	GL	—	Ground

NOTE: Signal is viewed from the APX-ISYM board.

TABLE 2-3. CN2 PIN ASSIGNMENT (RS-232C)

PIN. NO.	SIGNAL	DIRECTION	DESCRIPTION
1	FG	—	Frame ground
2	TXD	OUT	Transmitted data
3	RXD	IN	Received data
4	RTS	OUT	Request to send
5	CTS	IN	Clear to send
6	DSR	IN	Data set ready
7	GL	—	Signal ground
8	DCD	IN	Carrier detect
9-10	—	—	NC (unused)
11	REV	OUT	Reverse channel
12-14	—	—	NC (unused)
15	DB	IN	Transmitter clock input
16, 21-23	—	—	NC (unused)
17	RXC	IN	Receiver clock
20	DTR	OUT	Data terminal ready
24	TXC	OUT	Transmitter clock output

NOTE: Signal direction is viewed from the APX-ISYM board.

TABLE 2-4. CN3 PIN ASSIGNMENT (Parallel printer)

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	$\overline{STB}$	OUT	Strobe
2	DB0	OUT	Data line 0
3	DB1	OUT	Data line 1
4	DB2	OUT	Data line 2
5	DB3	OUT	Data line 3
6	DB4	OUT	Data line 4
7	DB5	OUT	Data line 5
8	DB6	OUT	Data line 6
9	DB7	OUT	Data line 7
10	$\overline{ACK}$	IN	Acknowledge
11	RDY	IN	Ready
12	$\overline{NPA}$	IN	No paper
13	$\overline{SLO}$	IN	Select out
14	$\overline{ALF}$	OUT	Auto line feed
15	—	—	NC (unused)
16	GL	—	Signal ground
17	FG	—	Frame ground
18	—	—	NC (unused)
19-30	GL	—	Signal ground
31	$\overline{RST}$	OUT	Reset
32	$\overline{ERR}$	IN	Error
33	GL	—	Signal ground
34	—	—	NC (unused)
35	$\overline{PWF}$	IN	Power failure
36	—	—	NC (unused)

NOTE: Signal direction is viewed from the APX-ISYM board.

TABLE 2-5. CN4 PIN ASSIGNMENT (CRT)

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	I	—	Intensity signal
2	GP	—	Ground
3	—	—	NC (unused)
4	H.SYNC	OUT	Horizontal sync
5	V.SYNC	OUT	Vertical sync
6	VIDEO (R)	OUT	Video signal (red)
7	VIDEO (G)	OUT	Video signal (green)
8	VIDEO (B)	OUT	Video signal (blue)
E	FD	—	Frame ground

NOTE: Signal direction is viewed from the APX-ISYM board.

TABLE 2-6. CN6/CN7 PIN ASSIGNMENT (FDD interface)

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	Ø3	OUT	Stepper motor phase signal
2	Ø1	OUT	Stepper motor phase signal
3	Ø4	OUT	Stepper motor phase signal
4	Ø2	OUT	Stepper motor phase signal
5	WPRT	IN	Write protect
6	$\overline{\text{MON}}$	OUT	Motor on signal
7	TR0	IN	Track 00 indicator
8	LED5V	OUT	+5V for LED
9	WD2	OUT	Write data
10	ERS	OUT	Erase timing signal
11	$\overline{\text{WG}}$	OUT	Write gate
12	WD1	OUT	Write data (complement of WD2)
13	+12V	—	+12V
14	$\overline{\text{SWFL}}$	OUT	Read amplifier control signal
15	GND	—	Ground
16	GND	—	Ground
17	RD	IN	Read data
18	+5V	OUT	+5V
19	$\overline{\text{INDX}}$	IN	Index
20	$\overline{\text{SSL1}}$	OUT	Side select
21-24	—	—	NC (unused)
25	HD5V	OUT	+5V for R/W circuitry
26	$\overline{\text{STP}}$	OUT	Stepper motor hold signal

NOTE: Signal direction is viewed from the APX-ISYM board. The above pinout is used for each connector.

TABLE 2-7. CN8 PIN ASSIGNMENT (Power to APX-ISYM board)

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	PWD	—	Power failure detection
2	GND	—	Ground of +5V
3	GND	—	Ground of −12V
4	GND		Ground of +12L
5	GP	—	Ground of +12V
6	GP	—	Ground of +12V
7	+5V	—	+5V for logic
8	+5V	—	+5V for logic
9	+5V		+5V for logic
10	−12V	—	−12V
11	+12L	—	+12V for logic
12	+12F	—	+12V for FDD
13	+12C	—	+12V for CRT

TABLE 2-8. CN9 PIN ASSIGNMENT (APX-ISYM to APX-IGGS board)

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	−12V	—	−12V
2	−12V	—	−12V
3-4	—	—	NC (unused)
5	+12L	—	+12V
6	+12L	—	+12V
7	+5V	—	+5V
8	+12L	—	+12V
9	+5	—	+5V
10	+5V	—	+5V
11	D0	IN/OUT	Data line 0
12	D1	IN/OUT	Data line 1
13	D2	IN/OUT	Data line 2
14	D3	IN/OUT	Data line 3
15	D4	IN/OUT	Data line 4
16	D5	IN/OUT	Data line 5
17	D6	IN/OUT	Data line 6
18	D7	IN/OUT	Data line 7
19	GL	—	GND
20	GL	—	GND
21	GL	—	GND
22	GL	—	GND

NOTE: Signal direction is viewed from the APX-ISYM board.

TABLE 2-9. CN10 PIN ASSIGNMENT (APX-ISYM to APX-IGGS)

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	GL	—	Ground
2	VIDEO (R)	IN	Video signal (red)
3	$\overline{\text{DACK2}}$	OUT	DMA acknowledge
4	VIDEO (G)	IN	Video signal (green)
5	I	IN	Video signal (intensity)
6	VIDEO (B)	IN	Video signal (blue)
7	V.SYNC	IN	Vertical sync
8	DCLK		NC (unused)
9	$\overline{\text{IORD}}$	OUT	Read data control signal
10	A0	OUT	Address line 0
11	—	—	NC (unused)
12	$\overline{\text{IOWR}}$	OUT	Write data control signal
13	$\overline{\text{CSCCR}}$	OUT	APX-iGGS I/O select
14	$\overline{\text{DREQ2}}$	IN	DMA transfer request
15	$\overline{\text{RESET}}$	OUT	Reset
16	—	—	NC (unused)
17	—	—	NC (unused)
18	H.SYNC	IN	Horizontal sync
19		—	NC (unused)
20	—	—	NC (unused)
21	A1	OUT	Address line 1
22	$\overline{\text{CSCRT}}$	OUT	APX-IGGS I/O select

NOTE: Signal direction is viewed from the APX-ISYM board.

TABLE 2-10. CN11 PIN ASSIGNMENT (Power test terminals)

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	GP	—	Ground for +12V
2	+12C	—	+12V for CRT
3	+12L	—	+12V for logic
4	+12F	—	+12V for FDD
5	−12V	—	−12V
6	GND	—	GND
7	+5	—	+5V for logic

TABLE 2-11. CN12 PIN ASSIGNMENT (NiCd battery)

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
A	-	—	Ground
B	—	—	Voltage for charging NiCd battery
C	—	—	+3.6V

TABLE 2-12. CN13 PIN ASSIGNMENT (Fan motor)

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	G	—	Ground
2	+12	—	+12V
3	+12R	—	+12V

TABLE 2-13. CN14 PIN ASSIGNMENT (Speaker)

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	LED	OUT	Power indicator
2	GL	—	Ground for power indicator
3	SPG	—	Ground for speaker
4	SP	OUT	Speaker signal

NOTE: Signal direction is viewed from the APX-ISYM board.

TABLE 2-14. CN15 PIN ASSIGNMENT (APX-ICRT board)

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	DA2	IN/OUT	Multiplexed data address line 2
2	VRAM	IN	Video RAM range signal
3	—	—	NC (unused)
4			NC (unused)
5	+5	—	+5V
6	+5	—	+5V
7	A10	OUT	Address line 10
8	RES	OUT	Reset
9	A13	OUT	Address line 13
10	I/M	OUT	I/O memory select line
11	HLDA	OUT	Hold acknowledge line
12	A9	OUT	Address line 9
13	DA1	IN/OUT	Multiplexed data/address line 1
14	A8	OUT	Address line 8
15	A14	OUT	Address line 14
16	A11	OUT	Address line 11
17	ALE	OUT	Address latch enable
18	DA6	IN/OUT	Multiplexed data/address line 6
19	A12	OUT	Address line 12
20	DMA	OUT	DMA address enable
21	GND	—	Ground
22	GND	—	Ground

NOTE: Signal direction is viewed from the APX-ISYM board.

TABLE 2-15. CN16 PIN ASSIGNMENT (APX-ICRT board)

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	CLK	OUT	5.3MHz clock signal
2	—	—	NC (unused)
3	DT/R	OUT	Transmit/receive bus control line
4	$\overline{\text{WAIT}}$	IN	ICRT wait request line
5	DA3	IN/OUT	Multiplexed data/address line 3
6	DA7	IN/OUT	Multiplexed data/address line 7
7	DA4	IN/OUT	Multiplexed data/address line 4
8	DA5	IN/OUT	Multiplexed data/address line 5
9	A16	OUT	Address line 16
10	$\overline{\text{WR}}$	OUT	8088 write control line
11	SSO	OUT	8088 bus status line
12	A15	OUT	Address line 15
13	DEN	OUT	8088 data enable line
14	$\overline{\text{RD}}$	OUT	8088 read control line
15	A17	OUT	Address line 17
16	—	—	NC (unused)
17	A19	OUT	Address line 19
18	—	—	NC (unused)
19	—	—	NC (unused)
20		—	NC (unused)
21	A18	OUT	Address line 18
22	DA0	—	Multiplexed data/address line 0

NOTE Signal direction is viewed from the APX-ISYM board.

TABLE 2-16. OPTION CARD PIN ASSIGNMENT

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1-2	GND	—	Ground
3-10	DTB0—7	IN/OUT	Data bus
11-12	-12V	—	-12V
13-20	ADR0-7	OUT	Address bus lines 0—7
21-28	—	—	NC (unused)
29-30	GND	—	Ground
31	CLK	OUT	System clock
32	GND	—	Ground
33	BSAK	OUT	Bus acknowledge
34	—	—	NC (unused)
35	$\overline{IRD}$	OUT	I/O read control line
36	$\overline{IWR}$	OUT	I/O write control line
37-38	-	—	NC (unused)
39	$\overline{RSIN}$	IN	Reset input
40	INT(H)1	IN	High-priority interrupt #1
41	INT(H)2	IN	High-priority interrupt #2
42	INT(_)	IN	Low-priority interrupt
43	+5V	—	+5V
44	$\overline{RSET}$	OUT	Reset output
45-46	+5V	—	+5V
47	$\overline{DRQ(F)}$	IN	DMA request (master)
48	$\overline{DRQ(S)}$	IN	DMA request (slave)
49-51	—	--	NC (unused)
52	$\overline{IWS}$	OUT	I/O write control line
53	$\overline{DAK(F)}$	OUT	DMA acknowledge (master)
54	$\overline{DAK(S)}$	OUT	DMA acknowledge (slave)
55	$\overline{EOP(F)}$	OUT	End of process (master)
56	$\overline{EOP(S)}$	OUT	End of process (slave)
57-58	+12V	—	+12V
59-60	GL	--	Ground

NOTE: Signal direction is viewed from the APX-ISYM board.

2.2 POWER SUPPLY OPERATION (Figure 2-2)

The Q10PS power supply board converts AC input to the voltages used by the CPU unit, FDDs, and keyboard. The power supply board is available in two versions: in the 110VAC model jumper J1 is installed; in the 220VAC model J1 is removed. (Refer to the Q10PS schematic in Chapter 6.)

The primary control circuits are simplified using hybrid ICs, and amplify oscillation pulses of approximately 30 KHz to drive the transformer primary. The secondary voltages are rectified, smoothed, and regulated to produce system voltages of +5 and ± 12VDC. The +5V is monitored by IC2 and stablized by varying the duty of the oscillation frequency.

Protective circuitry in the power supply includes excess voltage and current prevention circuits, which protect the components on the load side from overvoltage/current, and the power down circuit, which monitors AC and initiates a protective interrupt to the main CPUs in instances of sudden voltage drop.

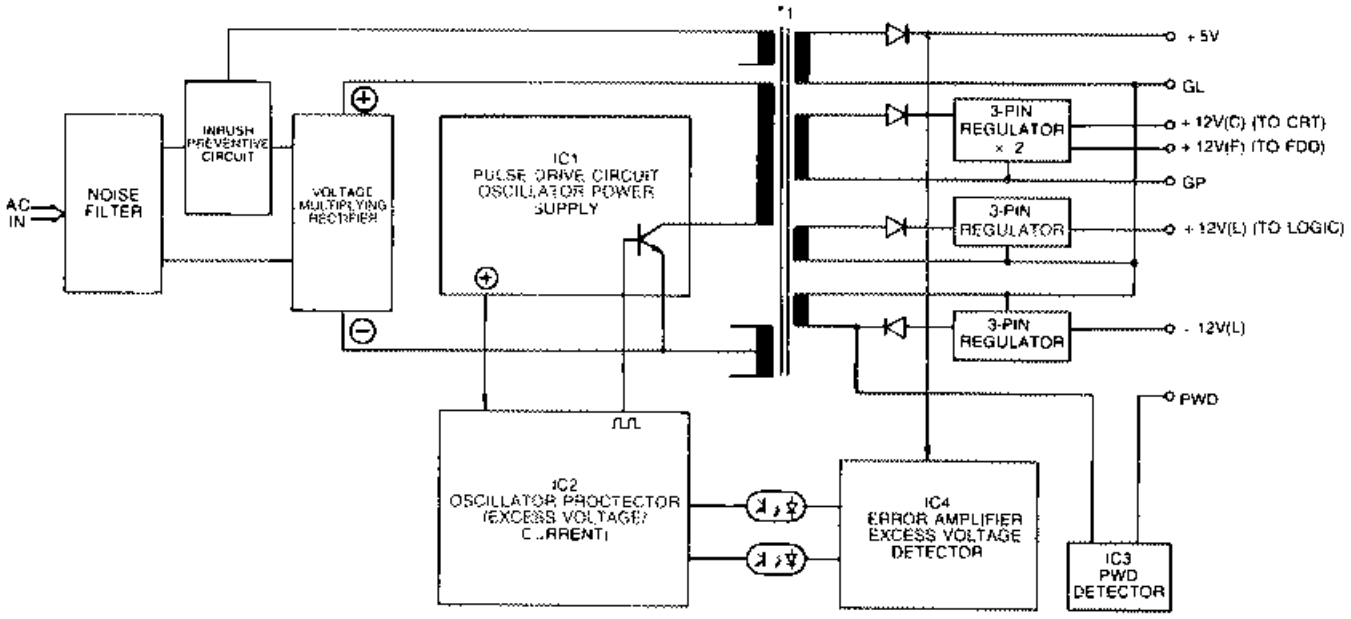


FIGURE 2-2. POWER SUPPLY BLOCK DIAGRAM.

2.2.1 **Noise Filter** (Figure 2-3)

The noise filter prevents system malfunction due to input surge, and inhibits electronic noise to the AC line.

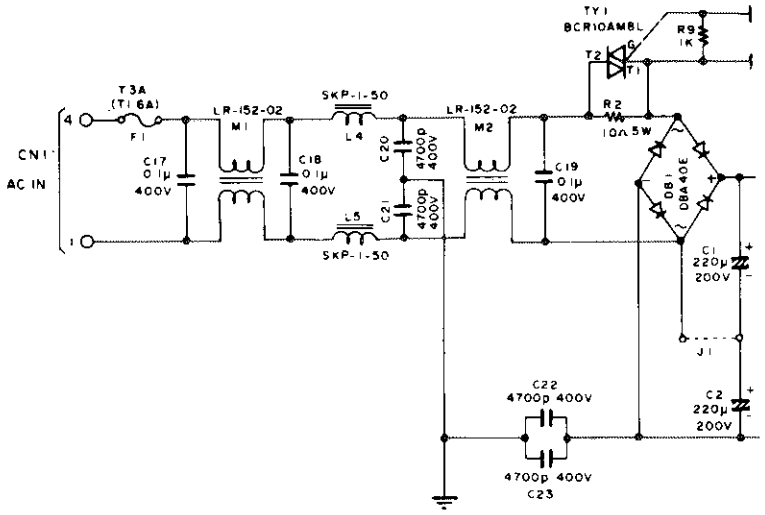


FIGURE 2-3. NOISE FILTER AND INRUSH PREVENTION CIRCUIT

2.2.2 **Inrush Prevention Circuit** (Figure 2-3)

The inrush prevention circuit protects diode bridge DB1 and subsequent components from being damaged by excessive current flow in C1 and C2 at power-up. R2 limits the current to DB1 when power is applied; when the switching oscillator operates normally, voltage from T1 activates triode TY1, permitting increased current flow to DB1.

2.2.3 **Voltage Multiplying Rectifier** (Figure 2-4)

The voltage multiplying rectifier (DB1, C1, C2, and J1) doubles and rectifies the 110VAC input when J1 is connected; when J1 is disconnected,the circuit is bypassed and the 220VAC is rectified directly. When DB1-1 conducts, C1 is charged with the maximum AC voltage, Vin. In the next half-cycle DB1-2 conducts, the C1 charging voltage and supply voltage are applied in the same direction, and voltage doubling occurs on the output side of the circuit.

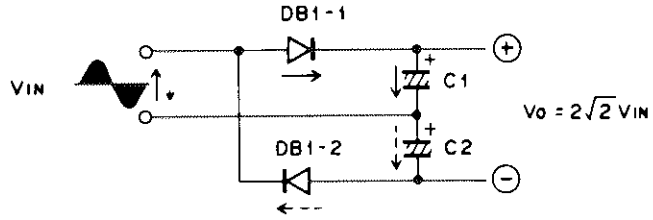


FIGURE 2-4. VOLTAGE MULTIPLYING RECTIFIER

2.2.4 Oscillator/Pulse Driver (Figures 2-5 through 2-8)

The oscillator and pulse driver circuit includes IC2 (STK752), which generates the high frequency switching signal, and IC1 (STK711), the pulse driver used to drive T1. The following is a description of the internal circuits of these two devices.

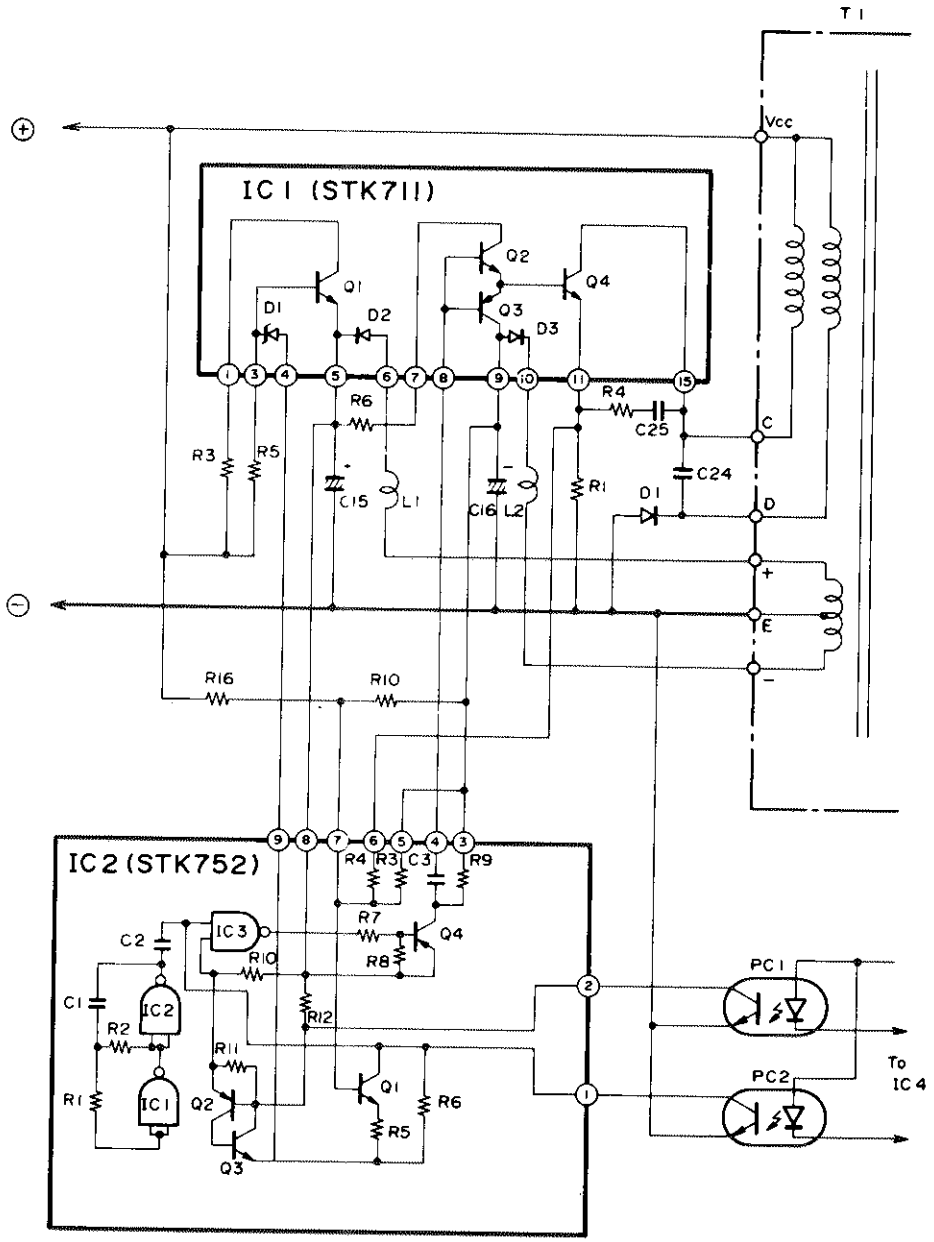


FIGURE 2-5. OSCILLATOR / PULSE DRIVER CIRCUIT

At power-up approximately 8V from the series pass regulator (Figure 2-6) is applied to pin 8 of IC2, initiating 30KHz oscillation. Pulses from IC2 are applied to IC1 to drive the primary of transformer T1.

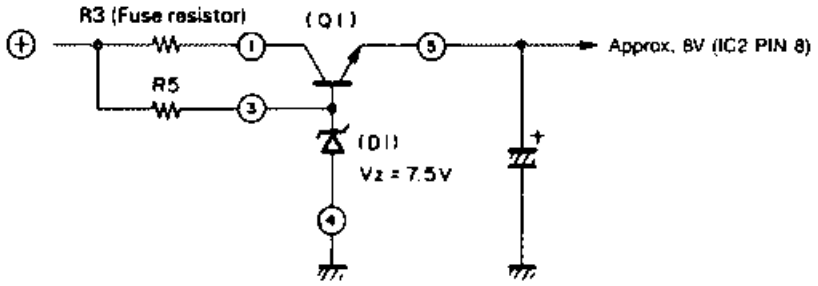


FIGURE 2-6. SERIES PASS REGULATOR

The voltage generated at T1 by switching of Q1 (IC1) is stabilized by L1 and an internal diode of IC1, and approximately 9V is returned to pin 8 of IC2 to maintain oscillation. If oscillation stops for any reason, excessive current is drawn through the series pass regulator, and fuse resistor R3 opens after approximately 2 minutes to halt power supply operation.

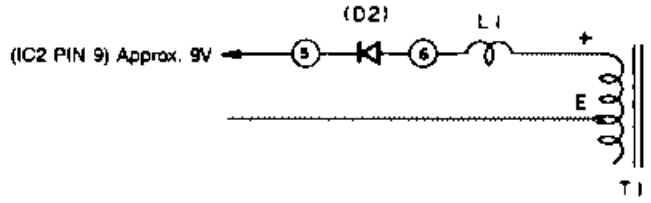


FIGURE 2-7. OSCILLATOR POWER CIRCUIT

The drive pulse from the oscillator is amplified by transistors within IC1 (Q2 and Q3, which switch Q4) driving T1. The approximately -9V power supply is derived from the voltage of T1 through L2, D3 (in IC1), and C16, and +9V is supplied from the oscillator power circuit. A counterelectromotive force protection circuit is formed by R4, C25, C24, and D1, connected to pins 10 and 12 of T1.

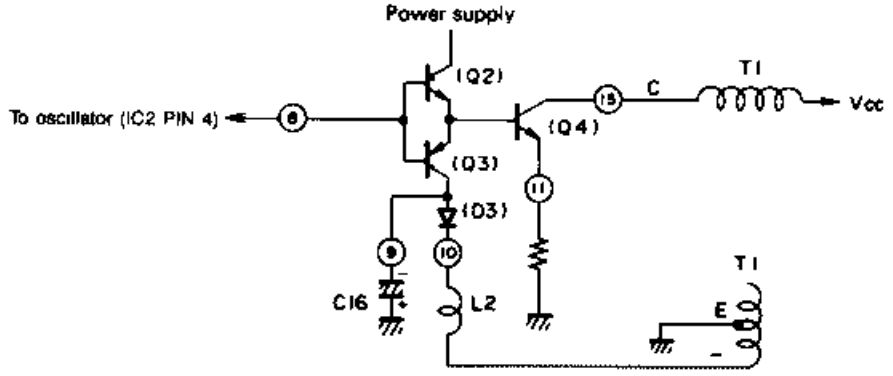


FIGURE 2-8. PULSE DRIVER CIRCUIT

2.2.5 Protection Circuitry (Figures 2-9 through 2-11)

When the output voltage on the +5V line rises above 8V, IC4 activates the opto isolator, PC1, which triggers the internal protection circuit of IC2 (Q2 and Q3), disabling oscillator output until the system power is turned off, then on again.

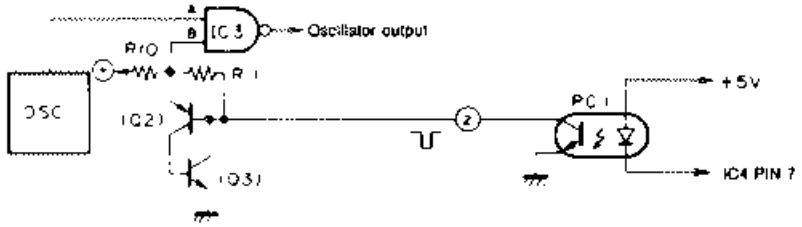


FIGURE 2-9. EXCESS VOLTAGE PROTECTOR

The voltage on the +5V line is monitored by the error amplifier in IC4. When the voltage exceeds the reference value, PC2 operates to alter the duty cycle of the internal oscillator of IC2. By varying the duty cycle of the oscillator output of pin 4 of IC2, a constant voltage is maintained on the +5V output.

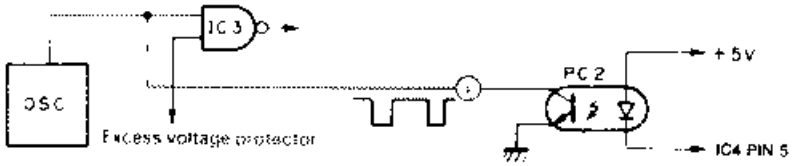


FIGURE 2-10. VOLTAGE STABILIZER

The voltage at each end of R1 in the pulse drive circuit is monitored by IC2. Excess current causes Q1 in IC2 to disable the IC2 internal oscillator; when all components in the power supply secondary are drawing maximum current, excessive current at the primary of T1 is detected by IC2, and oscillation stops. This circuit does not operate when only the +5V line is overloaded.

MAX CURRENT

+ 5V	7A
+ 12C	2A
+ 12F	2A
+ 12L	0.5A
− 12	0.5A

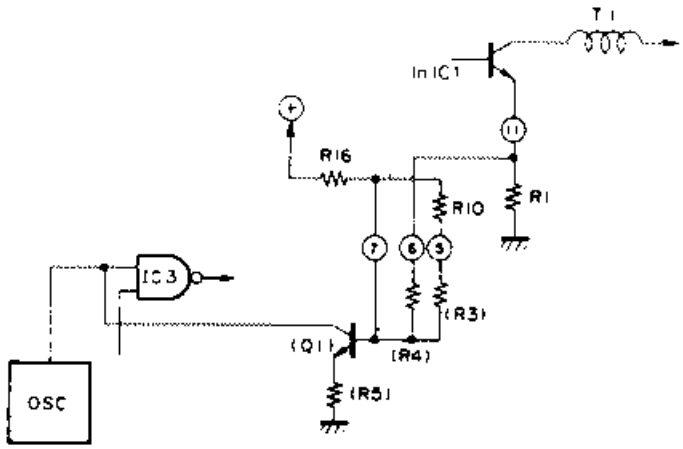


FIGURE 2-11. EXCESS CURRENT PROTECTION CIRCUIT

2.2.6 Error Amplifier and Excess Voltage Detector (Figure 2-12)

IC4 is used to monitor the + 5V line, operating in conjunction with PC2 as an error amplifier, and with PC1 as an excess voltage detector. In the error amplifier circuit, voltage lower than the reference value activates PC2 to set pin 1 of IC2 to low, and IC2 modifies the oscillation duty cycle to stabilize the voltage. VR1 is used to adjust the reference voltage under full load. In the excess voltage detector circuit, the + 5V line is monitored by Z1 in IC4 (Vz = 7.5V); when over 8V is detected PC1 is activated and oscillation stops until the system power is turned off, then on.

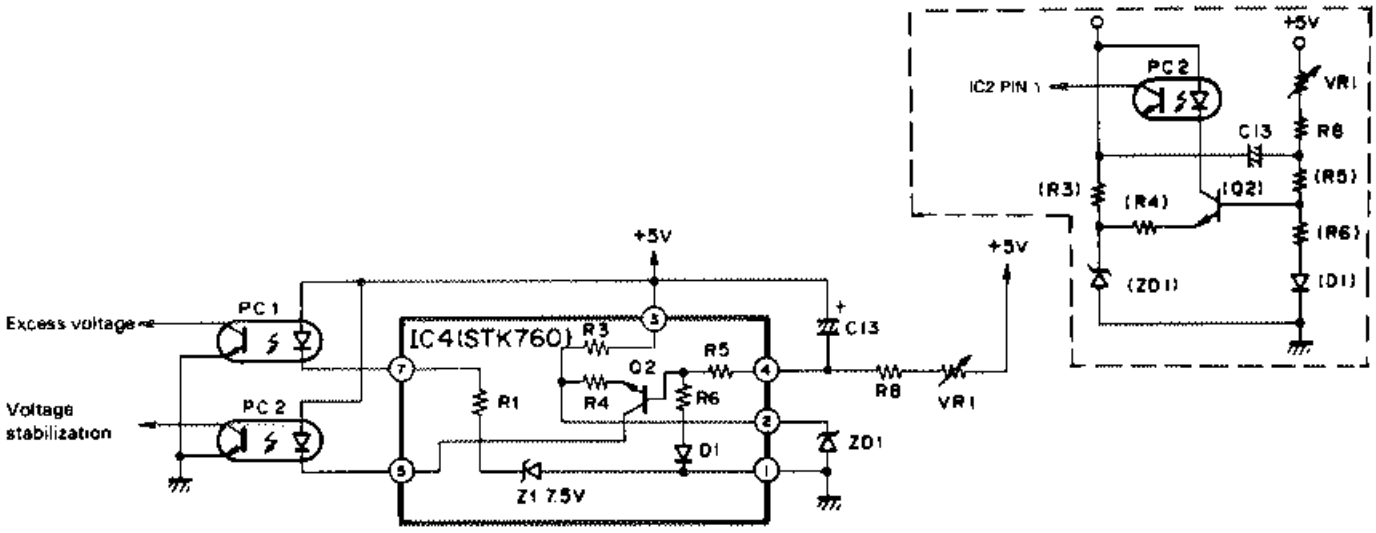


FIGURE 2-12. ERROR AMP AND EXCESS VOLTAGE DETECTOR (IC4)

2.2.7 Power Down Detector (PWD) (Figure 2-13)

In the power down detection circuit, rectified and filtered signals from pin 5 of T1 are input to IC3, which monitors the voltage on the AC line. If power drops below 80VAC in the 110V models or 160VAC in the 220V models, the PWD signal is output to the APX-ISYM board, causing an interrupt of the highest priority before the power instability is detected by the remainder of the system.

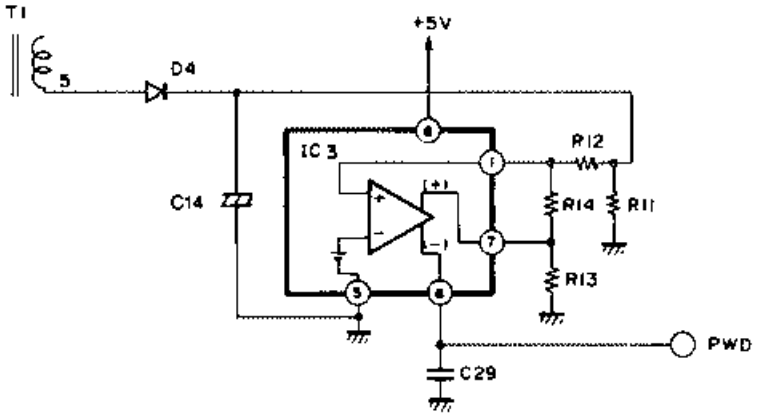


FIGURE 2-13. POWER DOWN DETECTOR (IC3)

2.2.8 Voltage Output Circuit

The + 5V output from T1 is rectified by DB2 and filtered by C3, C4, C5, and L3. The + 12C, + 12F, + 12V, and − 12V outputs from T1 are rectified by diodes DB3, D2, and D3, and the respective circuits are regulated by one of four three-pin regulators, SR3, SR4, SR1, and SR2, which provide internal protection against overvoltage/overcurrent on their outputs.

2.2.9 CMOS Battery Backup Circuit (Figure 2-14)

The CMOS ICs on the APX-ISYM board require a minimum 3.0VDC to retain memory; when power is turned off, this voltage is supplied by the battery backup circuit.

During normal operation, + 5V is supplied to CMOS via the 78M05 series regulator (D4 raises the regulator potential by approximately 0.6V to compensate for the drop at D5), and the battery is charged through D3 and R99. When power is turned off, approximately 3.5V is supplied to the IC from the battery, with D5 eliminating reverse current. C8 filters glitches from the CMOS supply during power on or off conditions.

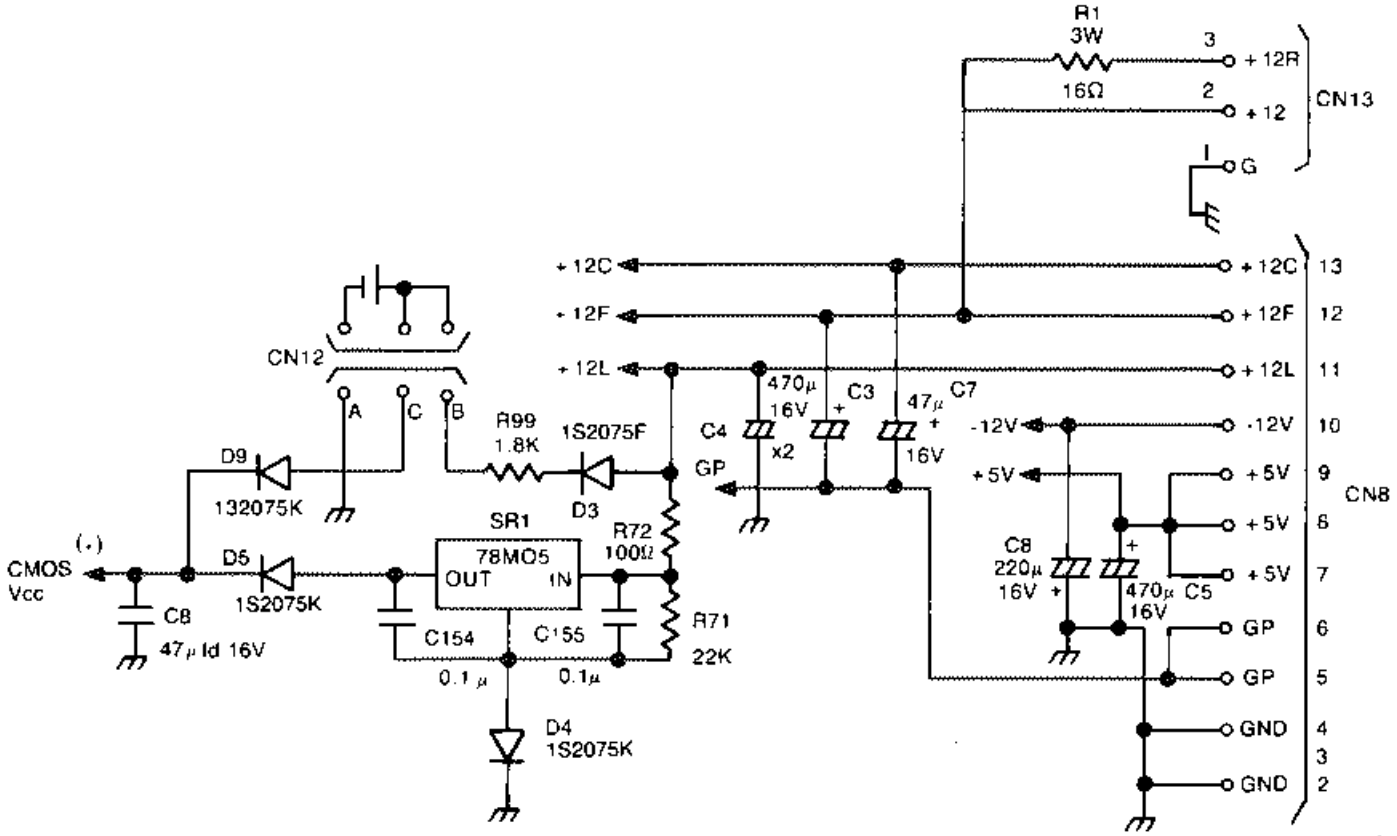


FIGURE 2-14. CMOS BATTERY BACKUP CIRCUIT

2.3 APX-ISYM BOARD OPERATION

A logic block diagram of the APX-ISYM board is provided in Figure 6-69, at the end of this manual. The board is functionally divided into CPU control, memory control, and input/output (I/O) control circuits, and the additional circuitry required to incorporate the programmable devices. In some circuits, the Z-80A and 8088 interact differently with the related components, as noted throughout the text.

2.3.1 CPU Control Circuits

This section describes the dual-processor configuration of the QX-16 and discusses the CPU control circuits in their descending order of importance to system operation.

2.3.1.1 8088/Z-80A CPU Circuit (Figure 2-15)

An 8088-2 and a Z-80A compatible chip, the 780C-1, are used in the QX-16. These processors share the address and data bus circuits, but are driven at different rates (5.3 MHz for 8088 and 3.99 MHz for Z-80A) and only one CPU can be active at a time.

The Z-80A is selected at each system reset: the IPL is enabled, and the Z-80A executes code from within the IPL. After initializing the programmable devices, a short diagnostic test is performed on the first four (0-3) memory banks and the Z-80A CPU. If no errors are detected, the Z-80A attempts loading the 8-bit operating system from the left floppy disk. If this step fails, the Z-80A attempts loading a 16-bit operating system, and repeats the loading process until a valid operating system is found on the left drive. If a 16-bit system is loaded, the Z-80A switches control to the 8088, which begins execution from the BIOS ROM at location 0FFFF0H.

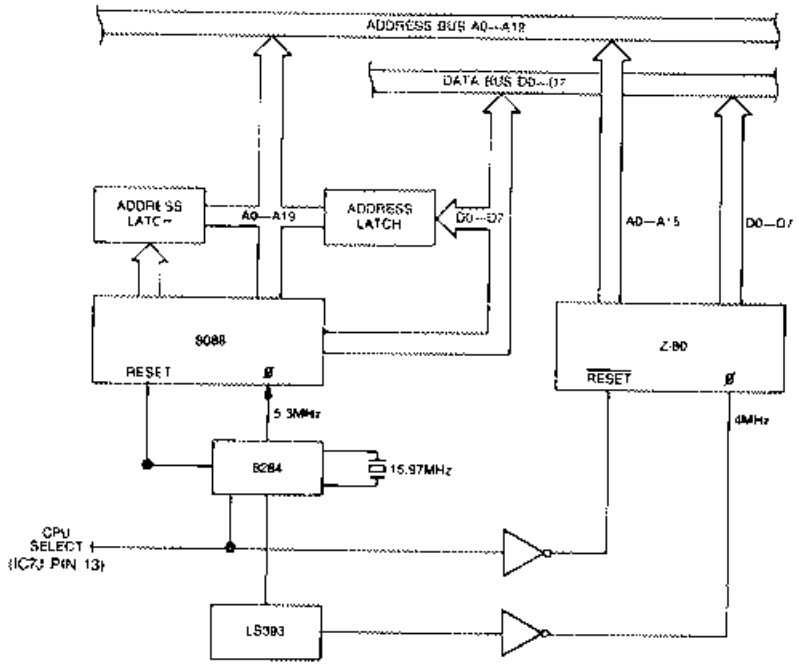


FIGURE 2-15. QX-16 CPU CIRCUIT DIAGRAM

NOTE: *If an error message is displayed, press RESET to retry, or refer to the troubleshooting procedures in Chapter 3.*

2.3.1.2 System Reset Circuit (Figure 2-16)

A 500 millisecond system reset is generated under the following conditions :

1. Manual reset is accomplished by closing switch SW1, located under the right hand floppy disk drive, which turns on CY1 and pulls the input on pin 11 of IC 25H low.
2. Power-on reset occurs when power is applied.
3. Power-down reset occurs when the Q10PS board detects low voltage on the AC line and supplies a postive pulse to pins 8 and 9 of IC 24F. R77 and C199 act as a filter to prevent reset from occuring for inputs of less that 10 milliseconds duration. The output of the power-down reset circuit causes the same action as closing SW1 during manual reset.
4. Option slot reset occurs when an option card pulls low the RSIN signal on pin 39 of the option connector. The option card hardware determines the exact period of the reset pulse, but it must be a minimum of 500 milliseconds to guarantee proper initialization of all devices.

The output of the reset circuit is supplied to the Z-80A memory bank latch, the CPU selector circuit, and most of the programmable devices. The 146818 real time clock, however, is reset and disabled by the power-down circuit, preventing any spurious read or write operations to the RTC during power-down conditions.

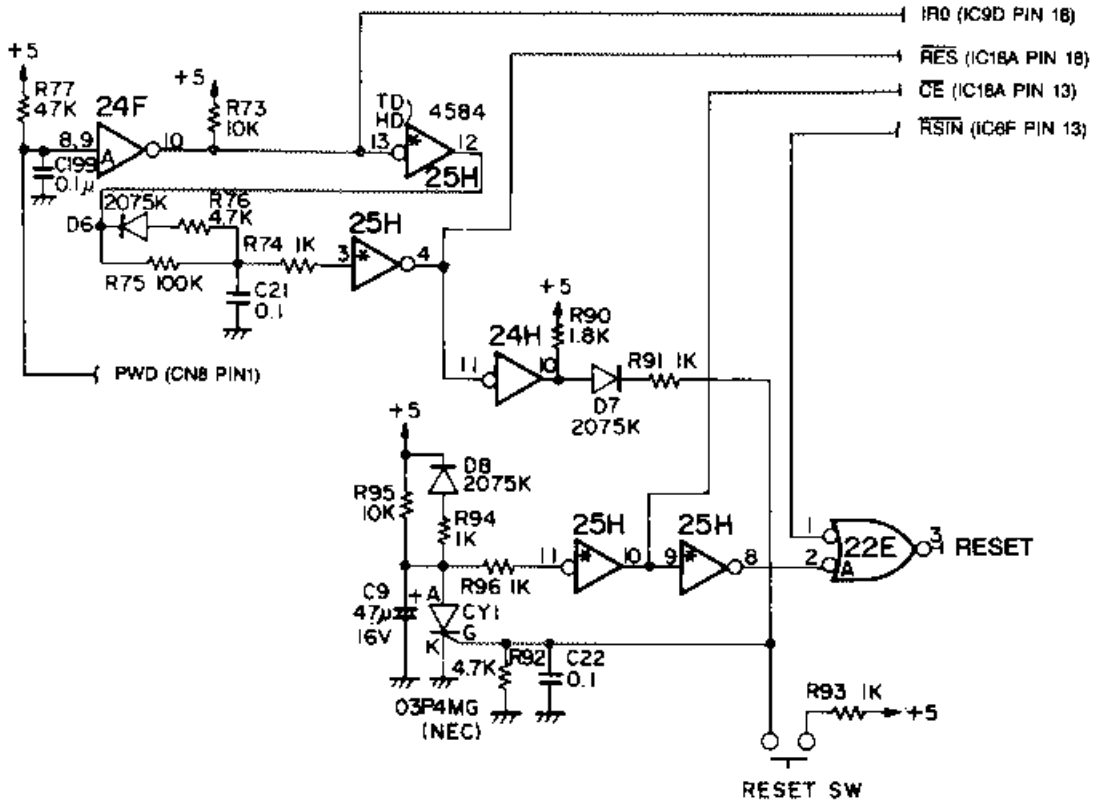


FIGURE 2-16. SYSTEM RESET CIRCUIT

2.3.1.3 CPU Select Circuit (Figures 2-17 and 2-18)

The CPU select circuit determines which CPU has active control of the system bus. The LS259 system configuration latch (15F) selects the active CPU by its Q1 output (pin 5); the output is controlled by bit 0 when either CPU writes to port 24H.

When one CPU writes to port 24H, the value of data bit 0 determines which CPU is active. When this bit is low, as in power-on default, the Z-80A is selected; if high, the 8088 is enabled. The output from the latch (15F) is input to IC 7J, which updates the CPU select signal two clock cycles later.

The output of IC 7J pin 13 controls the activity of the CPU reset inputs, and a processor switch command is used to start the selected CPU at the reset vector (0000H for the Z-80A and 0FFFF0H for the 8088). Note that switching the CPU does not cause the IPL to be selected nor is the Z-80A memory bank switch reset for bank 0.

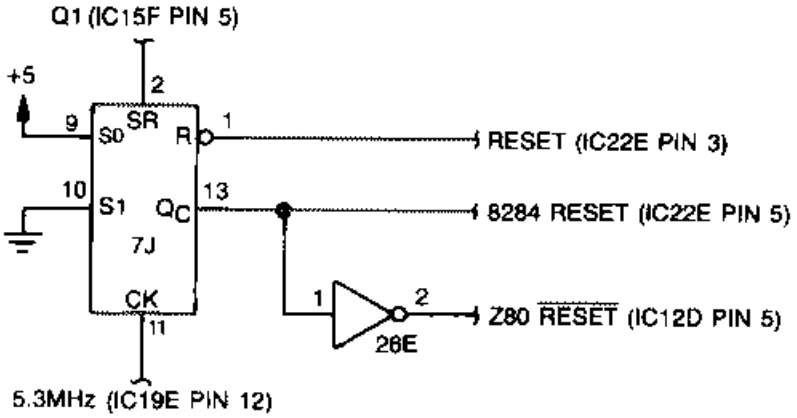
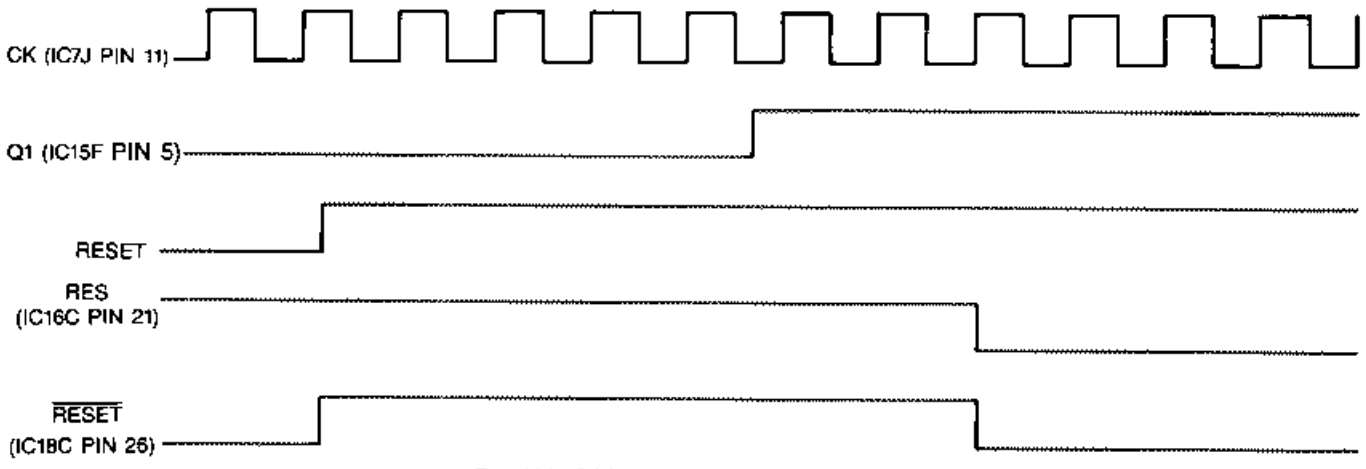


FIGURE 2-17. CPU SELECT CIRCUIT



*The 8088 RESET signal is active high.

FIGURE 2-18. CPU SELECT TIMING DIAGRAM

2.3.1.4 System Clock and Timing Generator Circuits (Figures 2-19 through 2-22)

The clock and timing generator circuits include the 8088/Z-80A CPU clock generator circuit, composed of ICs 16E and 17E, which initiates system operation, and the system timing generator, composed of ICs 26D and 20E, which provides timing signals to the I/O and memory devices.

8088/Z-80A CPU Clock Generator Circuit

The 8284A clock generator (IC 17E) contains an oscillator and additional circuitry to generate the main control signals for the CPUs (Table 2-17). A 15.97 MHz crystal, CR3, is connected across pins 16 and 17 of 17E. For 8088 clocking, a 5.3 MHz square wave with a 33% duty cycle from the CLK output (pin 8) is used. The 8284A also receives the reset ($\overline{RES}$) and ready (RDY1 and RDY2) control signals, which it synchronizes with the 8088 CPU clock. $\overline{RES}$ is used to reset the processor during system reset and to control the 8088 from the CPU select circuit. RDY1 is used to provide wait state timing for system memory, and RDY2 to implement wait state timing during an I/O access to the APX-ICRT board.

To begin Z-80A clocking, the square wave from CR3, present on the OSC output (pin 12) of 17E, is supplied to the LS93 divider circuit (16E), which outputs a 3.99 MHz clock to the Z-80A from pin 9, and a 1.99 MHz clock to the 8253 timer/counters from pin 8.

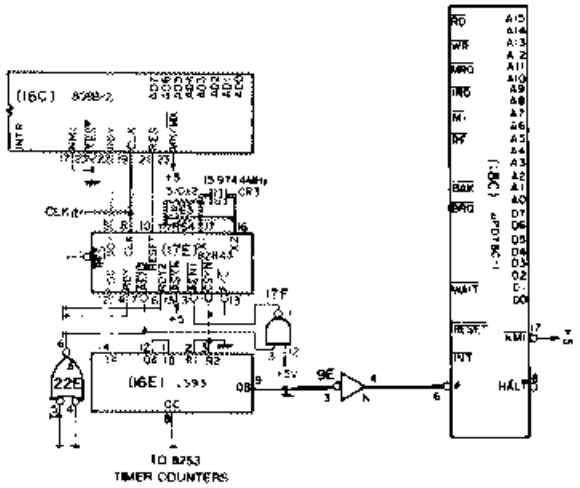


FIGURE 2-19. CPU CLOCK GENERATOR CIRCUIT

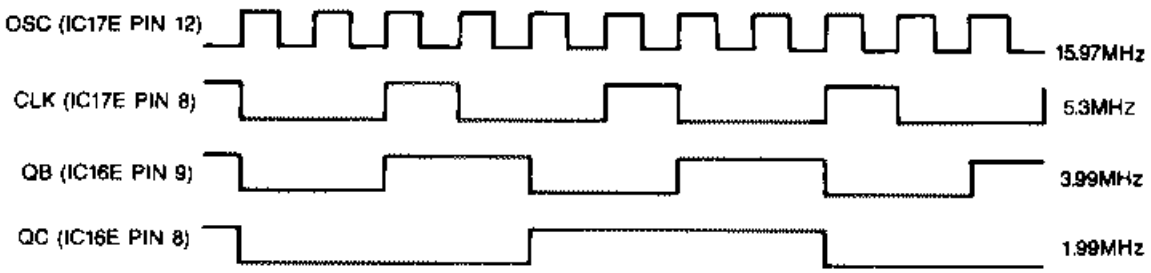


FIGURE 2-20. CPU CLOCK GENERATOR TIMING DIAGRAM

System Timing Generator Circuit

The LS175 4-bit shift register (20E) in the system timing generator circuit produces timing signals used by the I/O and memory devices. All outputs of IC 20E are low when the reset input, pin 1 of 20E, is low. During a write operation, or a DMA memory read or write initiated by the 8237, IC 26D outputs a high and the data and reset inputs of 20E are driven high. On each positive transition of the clock input, pin 9 of 20E, the level on the data input is transferred by one bit.

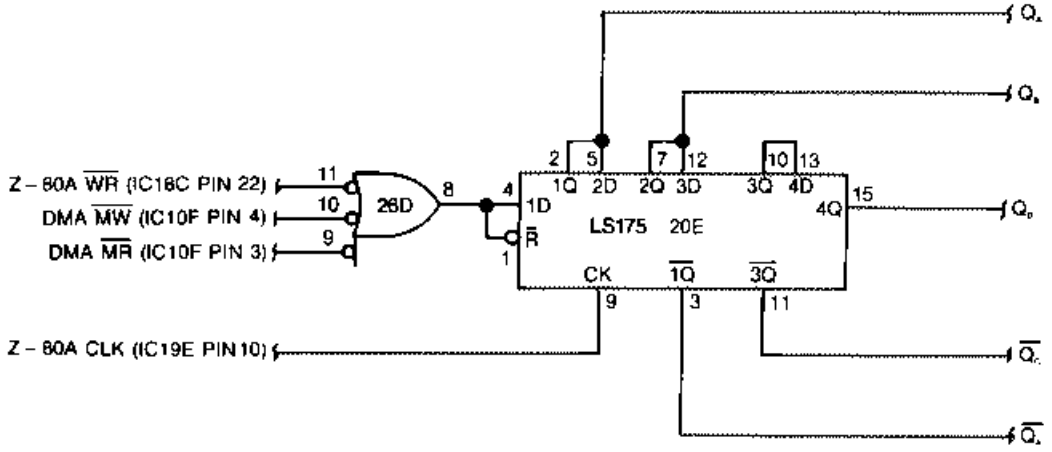


FIGURE 2-21. SYSTEM TIMING GENERATOR CIRCUIT

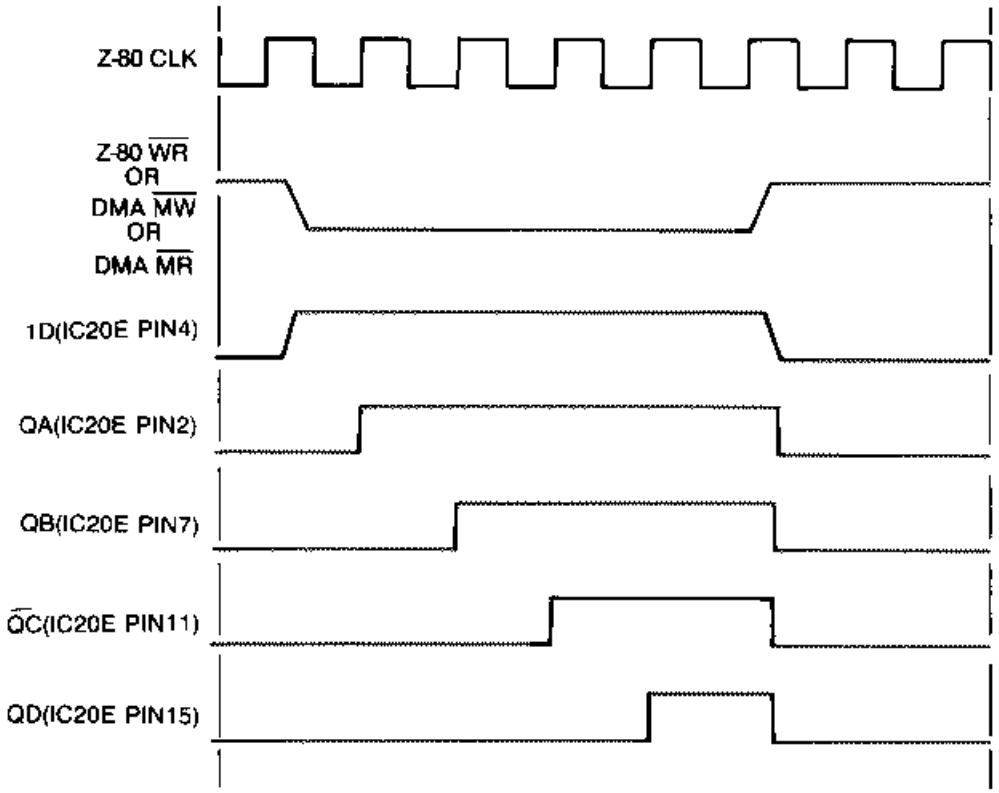


FIGURE 2-22. SYSTEM TIMING GENERATOR TIMING DIAGRAM

TABLE 2-17. 8284A CLOCK GENERATOR PIN DESCRIPTION

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
3 7	$\overline{AEN1}$, $\overline{AEN2}$	IN	Address enable. AEN is an active low signal which serves to qualify its respective bus ready signal (RDY1 or RDY2).
4 6	RDY1 RDY2	IN	Bus ready (transfer complete). RDY is an active high which is an indication from a device located on the system data bus that data has been received, or is available.
5	READY	OUT	Ready is an active high signal which is the synchronized RDY signal input to the 8088 CPU.
17 16	X1, X2	IN	Crystal in. X1 and X2 are the pins to which a crystal of 3 times the processor clock frequency is attached.
13	F/C	IN	Frequency/crystal select. When strapped low, F/C permits the processor clock to be generated by the crystal.
14	EFI	IN	External frequency in. When F/C is strapped high, CLK is generated from the input frequency appearing on this pin.
8	CLK	OUT	Processor clock. CLK is the clock output used by the processor. CLK has an output frequency which is 1/3 of the crystal or EFI input frequency and a 1/3 duty cycle
2	PCLK	OUT	Peripheral clock. PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.
15	$\overline{ASYNC}$	IN	Synchronization select input. Synchronizes READY input when tied high.
12	OSC	OUT	Oscillator output. OSC is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal
11	RES	IN	Reset in. RES is an active low signal which is used to generate RESET.
10	RESET	OUT	Reset is an active high signal which is used to reset the 8088.
1	$\overline{CSYNC}$	IN	Clock Synchronization. When using the internal oscillator, CSYNC should be hard-wired to ground.
9	GND		Ground
18	Vcc		+5V supply

2.3.1.5 Z-80A $\overline{\text{WAIT}}$ Signal Generator Circuit (Figures 2-23 and 2-24)

To allow an adequate timing margin for all memory devices, the $\overline{\text{WAIT}}$ signal generator circuit provides one additional clock cycle for every instruction fetch cycle of the Z-80A.

The Z-80A machine cycle lasts 3 or 4 clock cycles (T states), depending on the instruction being executed. The first part of the instruction fetch is the same for all instructions: the CPU outputs the address specified by the program counter onto the address bus during the T1 cycle and reads the memory data at the end of the T2 cycle. The $\overline{\text{WAIT}}$ signal generator uses the CPU $\overline{\text{M1}}$ line and the Z-80A clock to generate an active low signal on the $\overline{\text{WAIT}}$ input (pin 24) of the CPU, which adds one T state (Tw) at the end of the T2 cycle and provides adequate timing margin to ensure accurate reading of data from memory.

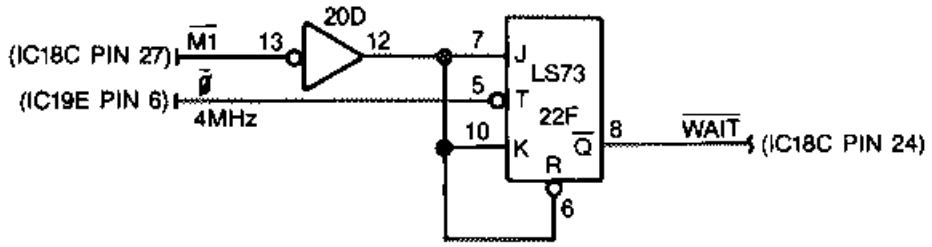


FIGURE 2-23. Z-80A $\overline{\text{WAIT}}$ SIGNAL GENERATOR CIRCUIT

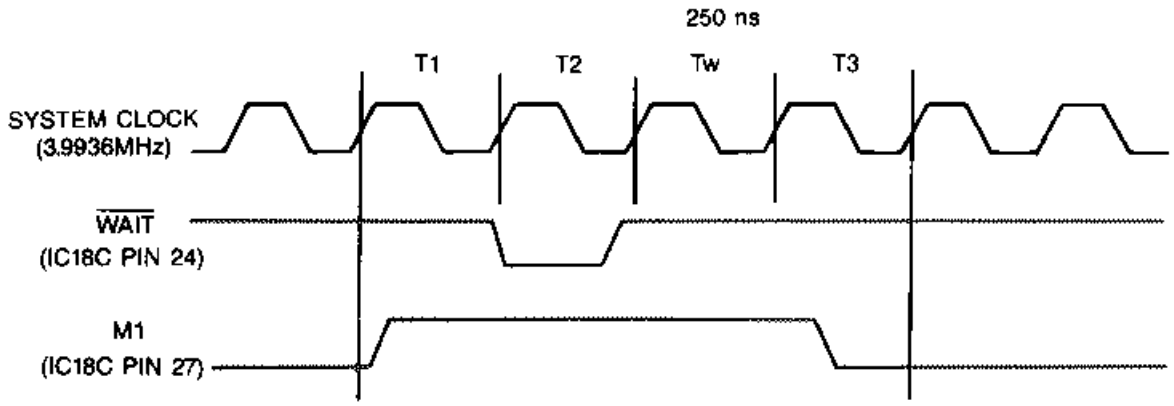


FIGURE 2-24. M1 TIMING CYCLE WITH WAIT STATE

2.3.1.6 8088 RDY Signal Generator Circuit (Figures 2-25 and 2-26)

The 8088 outputs the address specified by the bus interface unit (BIU) onto the address bus during the T1 cycle and reads the memory data into the instruction queue during the T3 cycle. It is necessary to add one clock cycle to every bus cycle of the 8088 CPU to allow adequate timing margin for all memory and I/O devices.

The RDY signal generator circuit uses the CPU $\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$ lines and the 8088 clock to generate an active low on the RDY1 input (pin 4) of the 8284A clock generator. The 8284A synchronizes the RDY1 input with the 8088 clock and supplies this signal to the RDY input (pin 22) of the 8088 CPU, which adds one T state (Tw) at the end of the T3 cycle, providing an adequate timing margin to ensure accurate reading of data from memory.

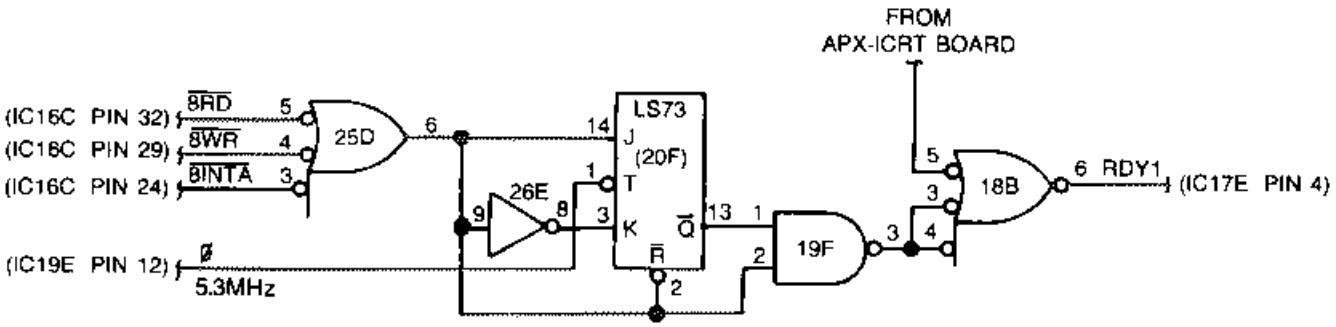


FIGURE 2-25. 8088 RDY SIGNAL GENERATOR CIRCUIT

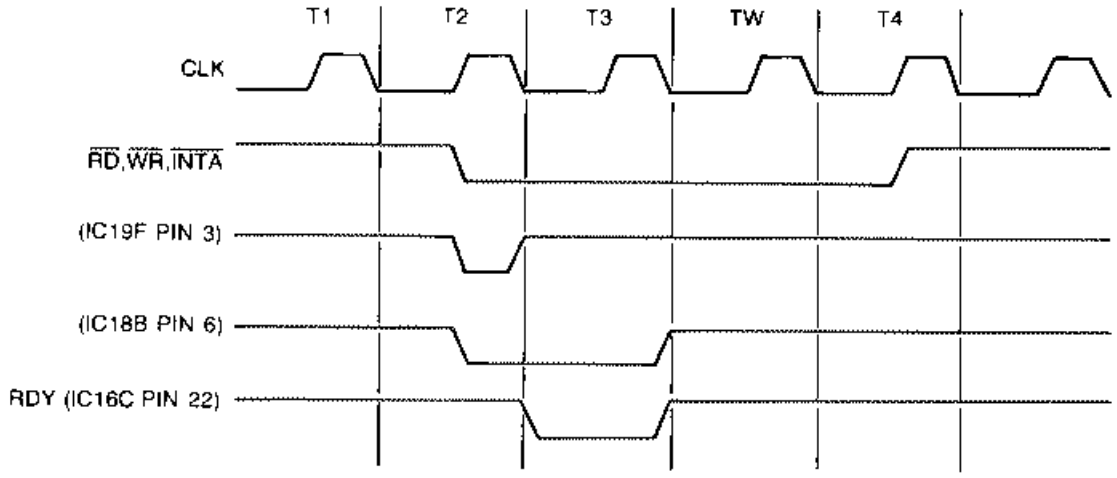


FIGURE 2-26. 8088 BUS CYCLE WITH WAIT STATE

2.3.1.7 Data Bus Direction Control Circuit (Figure 2-27)

The data bus consists of 8 lines which are used to read and write information into the memory and I/O devices. The LS245 bidirectional bus driver (14E) is used as the direction control gate to switch the data bus, depending on the CPU or DMA operation taking place. Two inputs on IC 14E ($\overline{G}$ and DIR) control the direction of transfer between the I/O and CPU side of the bus.

The $\overline{G}$ input is an active low gating signal which enables communication between the I/O and CPU busses, and disables communication when it is high. The $\overline{G}$ input goes low when a valid I/O write ($\overline{IOWR}$), I/O read ($\overline{IORD}$), or interrupt acknowledge ($\overline{INTA}$) signal is generated by the respective circuit.

The DIR input is the direction control line. When a valid $\overline{IORD}$ or $\overline{INTA}$ signal is generated, the DIR input is brought high by the output of IC 17F pin 8 allowing the I/O side to drive the CPU side of the bus. When an $\overline{IOWR}$ occurs, the DIR signal goes low, allowing the CPU to drive the I/O side of the bus.

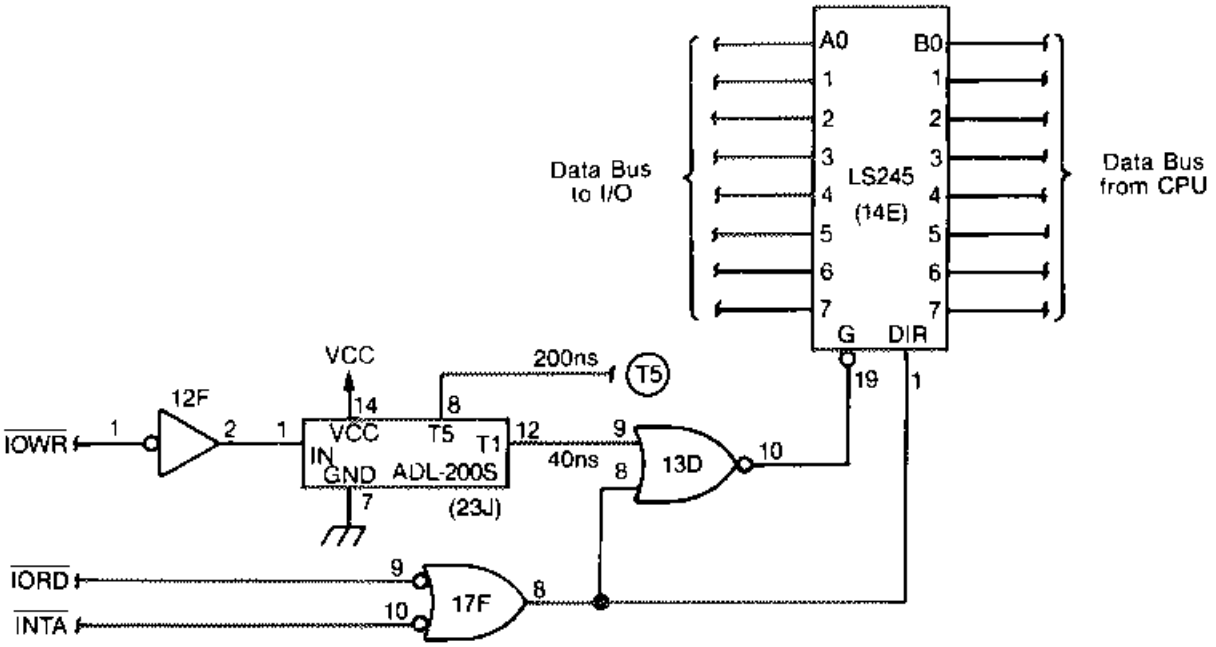


FIGURE 2-27. DATA BUS DIRECTION CONTROL CIRCUIT

2.3.1.8 CPU Bus Request Circuit (Figures 2-28 and 2-29)

The bus request circuit performs two functions: 1) it provides the bus request and acknowledge functions for both CPUs, and 2) it acts as the refresh timing generator. (Refer to Section 2.3.2.8 for description of refresh timing operation.)

The CPU bus request circuit causes the active CPU to relinquish the data bus so that DMA and DRAM refresh operations can be performed. The device needing access to the system bus initiates the bus request. To acknowledge this request, the CPU switches its output controls and busses to high-impedance and outputs a bus acknowledge signal while waiting for the bus request to finish.

When the active CPU is executing object code, the system bus acknowledge signal at IC 23J is low and pins 5 and 2 of 21D are high, making the DMA or refesh request valid. When either of these inputs (pins 3 and 4 of IC 21D) goes high, the output on pin 6 goes low to start the bus request cycle. This signal is delayed by two clock cycles through IC 21F to allow for synchronization. When the active CPU acknowledges the bus request, pin 8 of 23J goes high.

If the request is from the DMA controller, pin 12 of 25F is high, indicating that the request is not for a refresh operation, and the output on pin 11 of 25F is low, which sends the hold acknowledge (HAK) signal to the DMA controller.

If the bus request is from the refresh circuit, pin 1 of 25F is high, indicating that the request was not for a DMA operation, and the output on pin 3 of 25F is low, which disables the DMA request input and causes a low hold acknowledge (HAK) signal to be sent to the DMA controller.

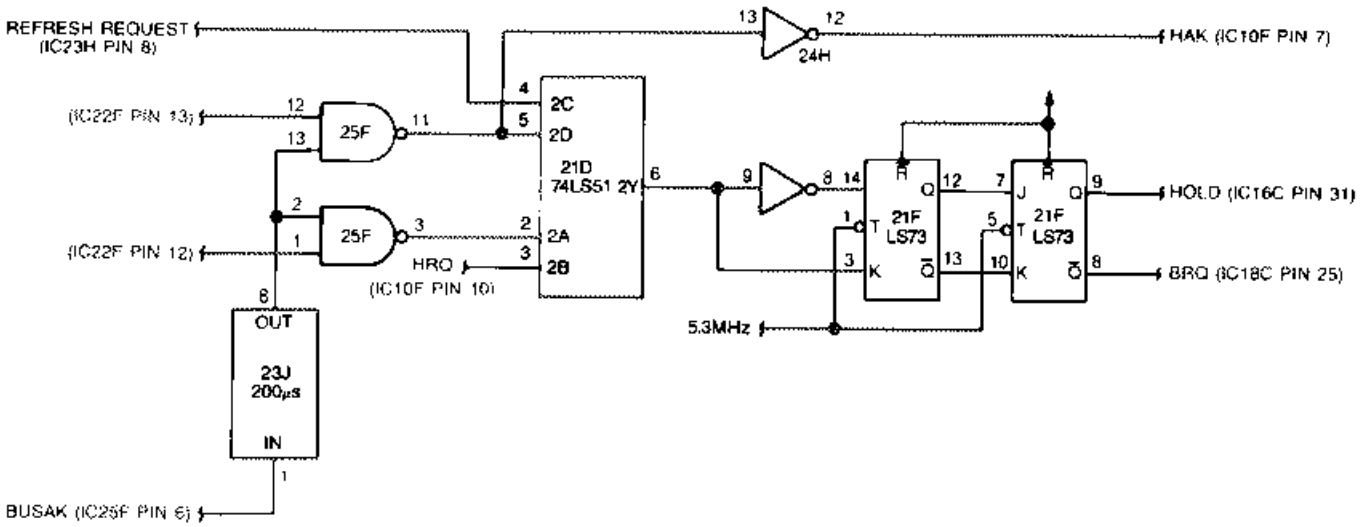


FIGURE 2-28. CPU BUS REQUEST CIRCUIT.

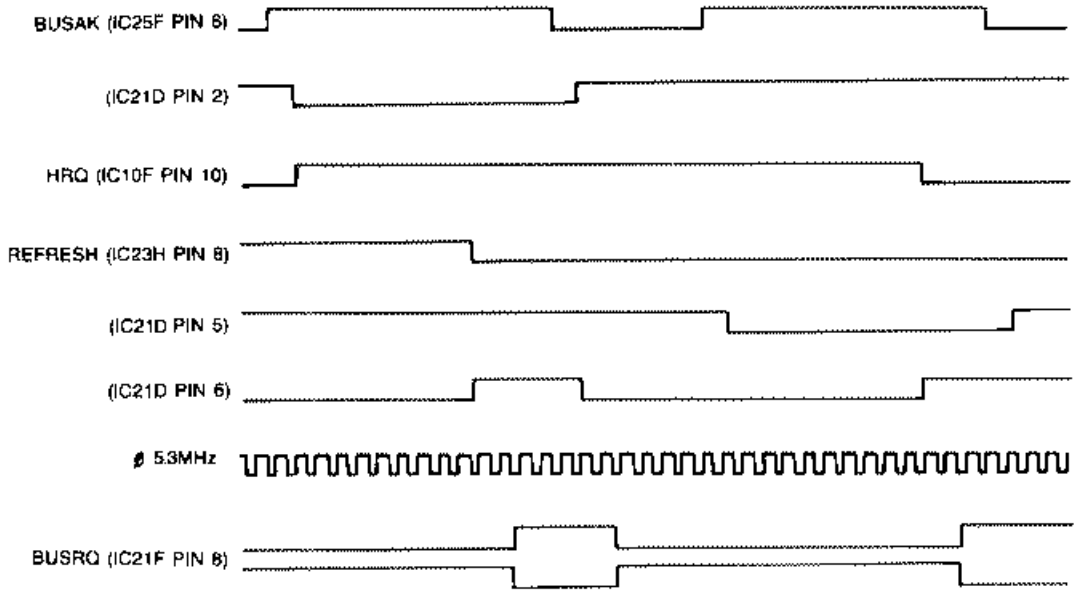


FIGURE 2-29. CPU BUS REQUEST TIMING DIAGRAM

2.3.2 Memory Control Circuits

The APX-ISYM board provides space for sixteen 256K x 1 dynamic random access memory chips (DRAMs), providing a possible total of 512K bytes system memory. The memory control circuit includes those devices used to access the memory. The Z-80A and 8088 CPUs require different memory control configurations, described in the following sections; therefore, the QX-16 includes two memory maps.

2.3.2.1 Memory Map Layout (Figure 2-30)

At power-on, resident RAM and the initial program loader (IPL) are the only memory devices selected. The IPL, at addresses 0000H to 0FFFH, can be enabled by writing a 0 to port 1CH. When IPL program execution is completed, the IPL selects the active CPU and memory map.

Z-80A Mode

The Z-80A has limited address space and must address the total memory area by switching between eight 64K-byte banks via two I/O ports. Each bank contains 56K bytes of DRAM dedicated to that bank, and 8K bytes resident RAM, at addresses 0E000H to 0FFFFH, which is shared between all banks.

In Z-80A mode, the 2K-byte CMOS RAM in the IPL is enabled by writing a value of 1 to port 20H. The CMOS RAM, at addresses 08000H to 087FFH, can be accessed from any of the eight banks. When this device is enabled, none of the memory in the selected bank between the end of the CMOS memory and the beginning of resident RAM can be accessed.

8088 Mode

The 8088 CPU does not have the same address limitations as the Z-80A, and is able to directly access the 512K bytes of DRAM as a single memory area (addresses 00000H to 80000H). The only other memory device required when the QX-16 s in 8088 mode is the BIOS firmware at addresses F8000H to FFFFFH of IC 24C. The CMOS RAM cannot be accessed from 8088 mode.

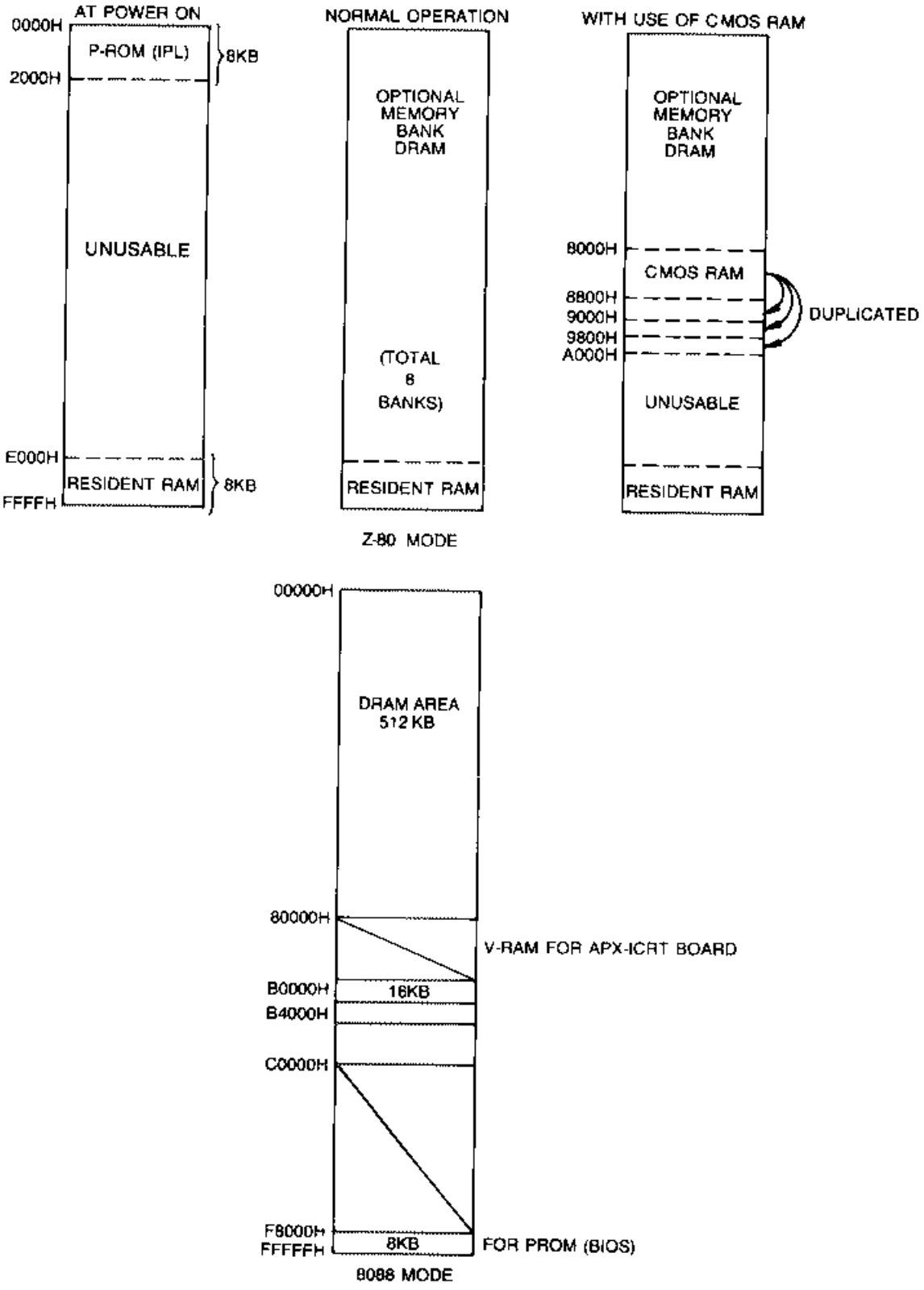


FIGURE 2-30. MEMORY MAP LAYOUT

2.3.2.2 Z-80A IPL Enable Circuit (Figure 2-31)

The IPL is the firmware which instructs the CPU to initialize the system hardware and read-in the boot loader from disk storage. This device is automatically selected at power-on by the system reset signal, and is enabled by two relatively simple circuits, chip enable ($\overline{CE}$) and output enable ($\overline{OE}$).

The chip enable ($\overline{CE}$) circuit has two inputs: the IPL select bit (15F pin 12), which is addressed as bit 0 of port 01CH, and the IPL range select signal, output active low from the Z-80A range select circuit when the Z-80A is addressing any location between 0000H and 1FFFH. When the IPL select bit and the IPL range bit are both low, IC 24D outputs a low level signal on pin 6.

The output enable ($\overline{OE}$) circuit receives both of its inputs from the Z-80A CPU. The memory request signal ($\overline{MRQ}$) goes low to indicate the current read or write operation is intended for memory, not I/O circuitry, and the Z-80A read signal ($\overline{RD}$) is issued active low by the CPU to enable the accessed memory or I/O device to put the requested data on the bus. When the Z-80A is ready to read the program contents from the IPL chip, IC 24D outputs a low at pin 11.

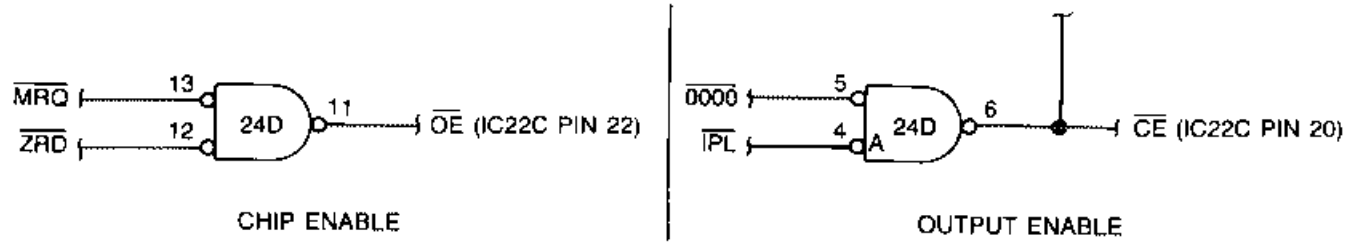


FIGURE 2-31. Z-80A IPL ENABLE CIRCUIT

2.3.2.3 8088 BIOS Enable Circuit (Figure 2-32)

IC 24C contains the BIOS firmware that the 8088 CPU executes when control is transferred from the Z-80A. This circuit requires only one gate, as the 8088 memory area is contiguous.

Three signals are input to the BIOS enable circuit: address bits A18 and A19, and the 8088 I/O memory select signal (I/$\overline{M}$). This circuit supplies a low level output from pin 12 of 26D whenever the 8088 accesses memory in the address range C0000H to FFFFFH.

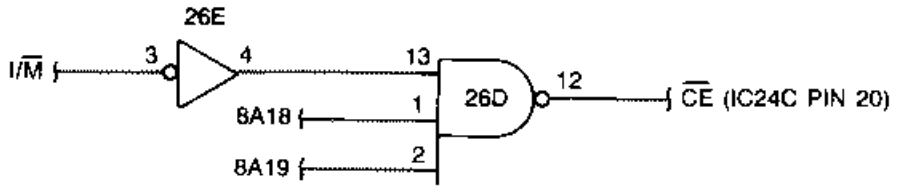


FIGURE 2-32. 8088 BIOS ENABLE CIRCUIT

2.3.2.4 449 CMOS RAM Enable Circuit (Figure 2-33)

The CMOS RAM enable ($\overline{CE1}$) circuit has five inputs. These signals are combined to generate three inputs to IC 26D.

The CMOS select bit (15F pin 4), addressed as bit 0 of port 020H, and the CMOS range select signal, output active from the Z-80A range select circuit when the Z-80A is addressing any location between 8000H and 9FFFH, are combined to produce a high level signal on pin 13 of IC 24F.

The Z-80A read ($\overline{RD}$) and write signals ($\overline{WR}$) are issued active low by the CPU to enable the accessed memory or I/O device to read data onto the bus or into the specified location. When the Z-80A is ready to read or write memory to I/O, IC 23D outputs a high on pin 8.

The memory request signal ($\overline{MRQ}$) goes low to indicate the current read or write operation is intended for memory, not I/O circuitry. This signal is inverted to high active by IC 26E.

When all of the above conditions are met, the three signal groups combine at IC 26D to produce a low level output, enabling the CMOS RAM.

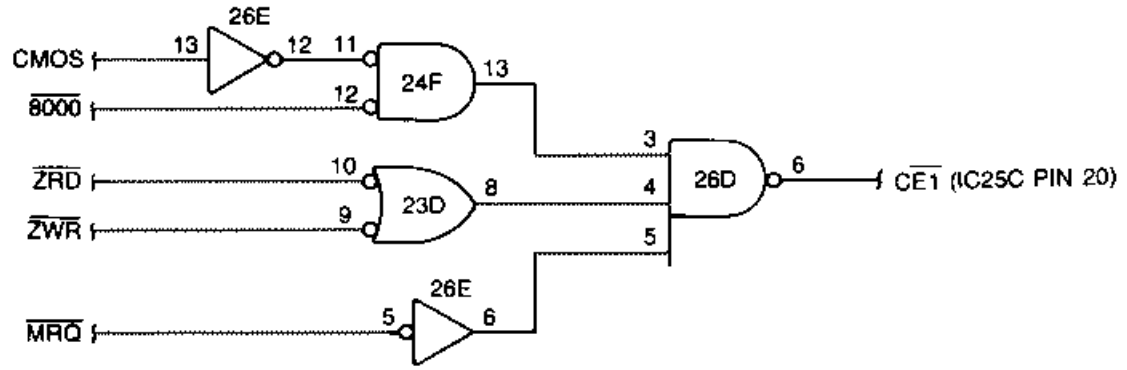


FIGURE 2-33. 449 CMOS RAM ENABLE CIRCUIT

2.3.2.5 Z-80A Memory Range Select Circuit (Figure 2-34)

In Z-80A mode, three special memory areas are active: the IPL region (0000H-1FFFH), CMOS RAM (8000H-87FFH), and the resident RAM space (E000H-FFFFH). The range select circuit is used to detect when any of these areas are being accessed.

The LS138 (21C) is used to decode the three most significant address bits of the Z-80A (A13, A14, and A15); when an access is made to any of these regions, the corresponding output goes low.

The gate inputs of IC 21C are used to enable the LS138. Input G1 is the active high input, and is always true (+5V). Inputs $\overline{G2A}$ and $\overline{G2B}$ are the active low enable inputs, and are tied to the CPU select circuit. When the Z-80A is selected, this input is low and the outputs are enabled. All outputs are high when the device is disabled.

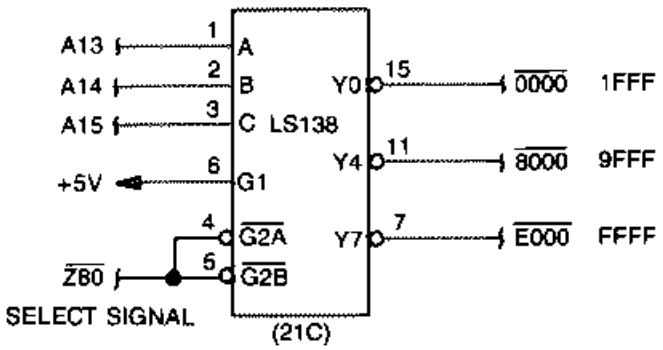


FIGURE 2-34. Z-80A MEMORY RANGE SELECT CIRCUIT

2.3.2.2 Z-80A IPL Enable Circuit (Figure 2-31)

The IPL is the firmware which instructs the CPU to initialize the system hardware and read-in the boot loader from disk storage. This device is automatically selected at power-on by the system reset signal, and is enabled by two relatively simple circuits, chip enable ($\overline{CE}$) and output enable ($\overline{OE}$).

The chip enable ($\overline{CE}$) circuit has two inputs: the IPL select bit (15F pin 12), which is addressed as bit 0 of port 01CH, and the IPL range select signal, output active low from the Z-80A range select circuit when the Z-80A is addressing any location between 0000H and 1FFFH. When the IPL select bit and the IPL range bit are both low, IC 24D outputs a low level signal on pin 6.

The output enable ($\overline{OE}$) circuit receives both of its inputs from the Z-80A CPU. The memory request signal ($\overline{MRQ}$) goes low to indicate the current read or write operation is intended for memory, not I/O circuitry, and the Z-80A read signal ($\overline{RD}$) is issued active low by the CPU to enable the accessed memory or I/O device to put the requested data on the bus. When the Z-80A is ready to read the program contents from the IPL chip, IC 24D outputs a low at pin 11.

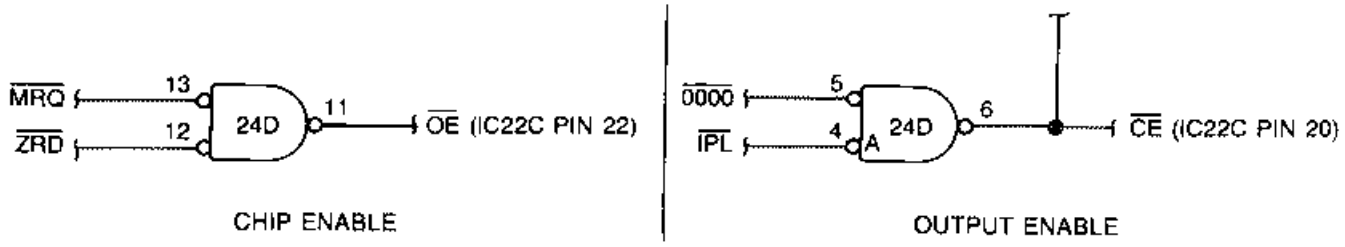


FIGURE 2-31. Z-80A IPL ENABLE CIRCUIT

2.3.2.3 8088 BIOS Enable Circuit (Figure 2-32)

IC 24C contains the BIOS firmware that the 8088 CPU executes when control is transferred from the Z-80A. This circuit requires only one gate, as the 8088 memory area is contiguous.

Three signals are input to the BIOS enable circuit: address bits A18 and A19, and the 8088 I/O memory select signal (I/$\overline{M}$). This circuit supplies a low level output from pin 12 of 26D whenever the 8088 accesses memory in the address range C0000H to FFFFFH.

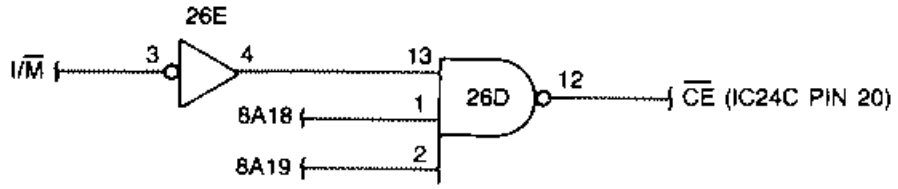


FIGURE 2-32. 8088 BIOS ENABLE CIRCUIT

2.3.2.4 449 CMOS RAM Enable Circuit (Figure 2-33)

The CMOS RAM enable ($\overline{CE1}$) circuit has five inputs. These signals are combined to generate three inputs to IC 26D.

The CMOS select bit (15F pin 4), addressed as bit 0 of port 020H, and the CMOS range select signal, output active from the Z-80A range select circuit when the Z-80A is addressing any location between 8000H and 9FFFH, are combined to produce a high level signal on pin 13 of IC 24F.

The Z-80A read ($\overline{RD}$) and write signals ($\overline{WR}$) are issued active low by the CPU to enable the accessed memory or I/O device to read data onto the bus or into the specified location. When the Z-80A is ready to read or write memory to I/O, IC 23D outputs a high on pin 8.

The memory request signal ($\overline{MRQ}$) goes low to indicate the current read or write operation is intended for memory, not I/O circuitry. This signal is inverted to high active by IC 26E.

When all of the above conditions are met, the three signal groups combine at IC 26D to produce a low level output, enabling the CMOS RAM.

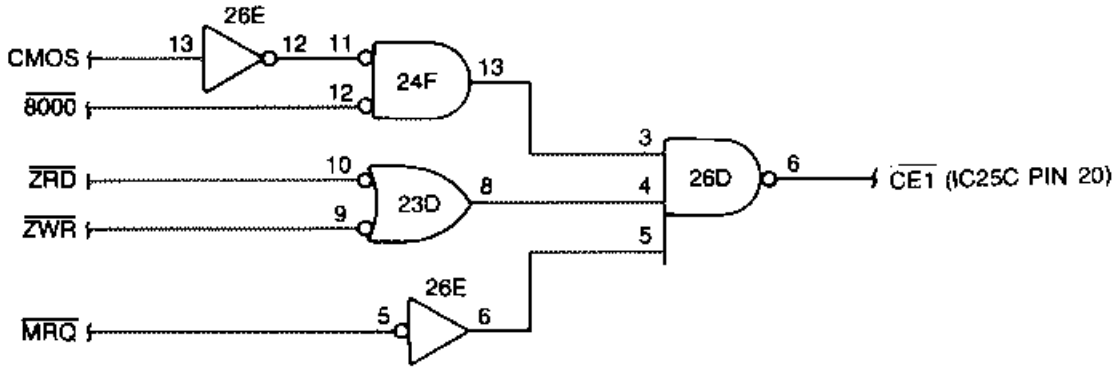


FIGURE 2-33. 449 CMOS RAM ENABLE CIRCUIT

2.3.2.5 Z-80A Memory Range Select Circuit (Figure 2-34)

In Z-80A mode, three special memory areas are active: the IPL region (0000H-1FFFH), CMOS RAM (8000H-87FFH), and the resident RAM space (E000H-FFFFH). The range select circuit is used to detect when any of these areas are being accessed.

The LS138 (21C) is used to decode the three most significant address bits of the Z-80A (A13, A14, and A15): when an access is made to any of these regions, the corresponding output goes low.

The gate inputs of IC 21C are used to enable the LS138. Input G1 is the active high input, and is always true (+5V). Inputs $\overline{G2A}$ and $\overline{G2B}$ are the active low enable inputs, and are tied to the CPU select circuit. When the Z-80A is selected, this input is low and the outputs are enabled. All outputs are high when the device is disabled.

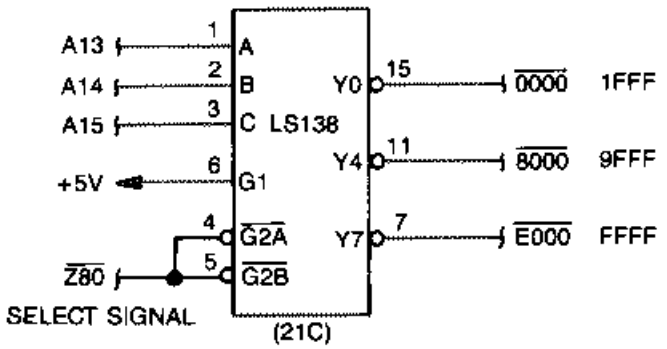


FIGURE 2-34. Z-80A MEMORY RANGE SELECT CIRCUIT

2.3.2.6 Z-80A RAS Inhibit Circuit (Figure 2-35)

To prevent signal conflict during memory bank selection and operation of the IPL and CMOS circuits, the row address strobe signal (RAS) for the DRAMs must be periodically disabled. There are four inputs to this circuit (CMOS select bit, A15, resident RAM range select, and $\overline{CE}$), and the output is supplied to the DRAM RAS timing generator.

When the CMOS select bit (15F pin 4), address bit A15, and the resident RAM range select signal are high, a low level signal is output on pin 8 of IC 22D, which indicates that CMOS is selected and the current address is greater than 8000H and less than E000H. This signal is input to pin 12 of 22E.

The IPL chip enable ($\overline{CE}$) signal is is applied to pin 13 of IC 22E. The output of IC 22D on pin 11 goes low when either of the inputs are low, inhibiting the generation of the RAS timing signal during use of the CMOS RAM or IPL.

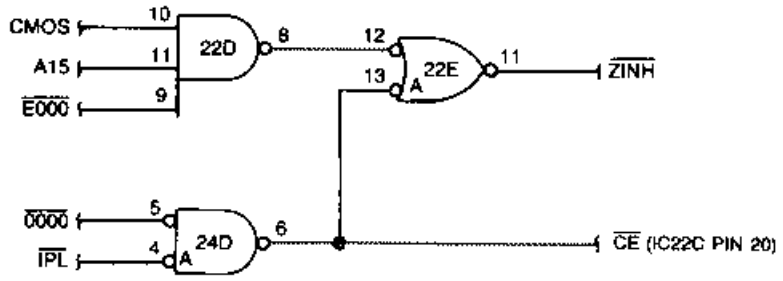


FIGURE 2-35. Z-80A RAS INHIBIT CIRCUIT

2.3.2.7 8088 RAS Inhibit Circuit (Figure 2-36)

In 8088 mode, the row address strobe (RAS) for the DRAMs must be disabled whenever the CPU is accessing memory outside the DRAM address space. There are four inputs to this circuit (A19, $\overline{HLDA}$, I/$\overline{M}$, and the CPU select signal), and the output is supplied to the DRAM RAS timing generator.

When address bit A19 (IC21D pins 1, 12, and 13) goes high, a low is ouput on pin 8, inhibiting the RAS signal when the 8088 requests access above address 80000H.

When the 8088 is active, in control of the bus, and attempting to access any I/O device, the hold acknowledge ($\overline{HLDA}$), I/O memory select line (I/$\overline{M}$), and select output from the CPU select circuit are combined to cause the output on pin 8 of 21D to go low, inhibiting the generation of the RAS timing signal.

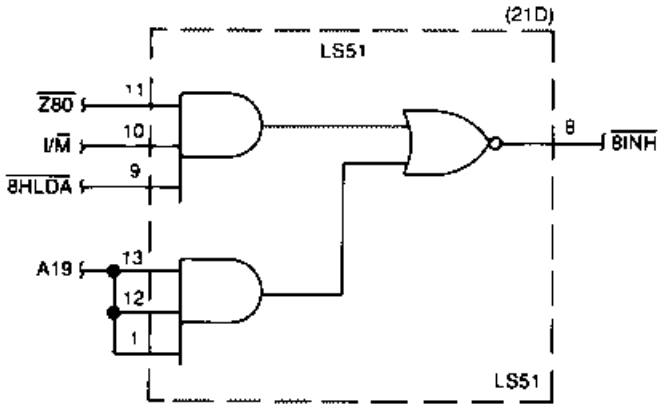


FIGURE 2-36. 8088 RAS INHIBIT CIRCUIT

2.3.2.8 DRAM Refresh Timing Generator Circuit (Figures 2-37 and 2-38)

Dynamic RAM chips require a refresh cycle to retain the data stored in their internal cells, and as chip size and memory density increase, the refresh rate must increase to accommodate the increased number of internal cells. The DRAMs used in the QX-16 require 256 refresh cycles every 4 milliseconds.

The refresh timing generator circuit is responsible for periodically stopping the active CPU and generating the signals which enable the DRAM address control circuits to provide the refresh cycles. Refresh cycles are requested approximately every 25 microseconds by the LS393 counter (23H). This IC is clocked by the output of 19F pin 11, a gated, 5.3 MHz square wave. The count proceeds until the output on pin 8 goes high. This output is fed back to the clock gate circuit through the inverter (20D), which stops the count and simultaneously begins a bus request cycle by causing a low on the output of IC 21D pin 6. (Refer to Section 2.3.1.8 for explanation of the bus request cycle.)

The output of IC 25F pin 6 goes high when the active CPU acknowledges the bus request. This has two effects: it latches the state of the pin 8 output of IC 23H into the LS73 (22F) flip-flop, and it supplies the signal to pins 2 and 13 of 25F with a 200 nanosecond delay inserted by delay line 23J. The refresh column address strobe output ($\overline{\text{REFCAS}}$, pin 3 of 25F) then goes low, enabling the RAS refresh generator (21E pin 9) and initiating the refresh timing cycle.

When pin 9 of 21E is brought high, it loads the preset value of 0CH into the D0-3 inputs and begins counting. The least significant bit (LSB) is input directly to pin 10 of 25F, and the most significant bit (MSB) is delayed 100 nanoseconds by IC 24J before being applied to pin 9 of 25F. These two signals generate four active low pulses on the output (pin 8) of 25F, which are the refresh row address strobe ($\overline{\text{REFRAS}}$) signals. When the count progresses past 0FH, the carry output on pin 15 (21E) resets the refresh timer (23H). The above operation must be performed 64 times to completely refresh the DRAMs. (Because it temporarily stops the active CPU, this operation does have an effect on software timing loops.)

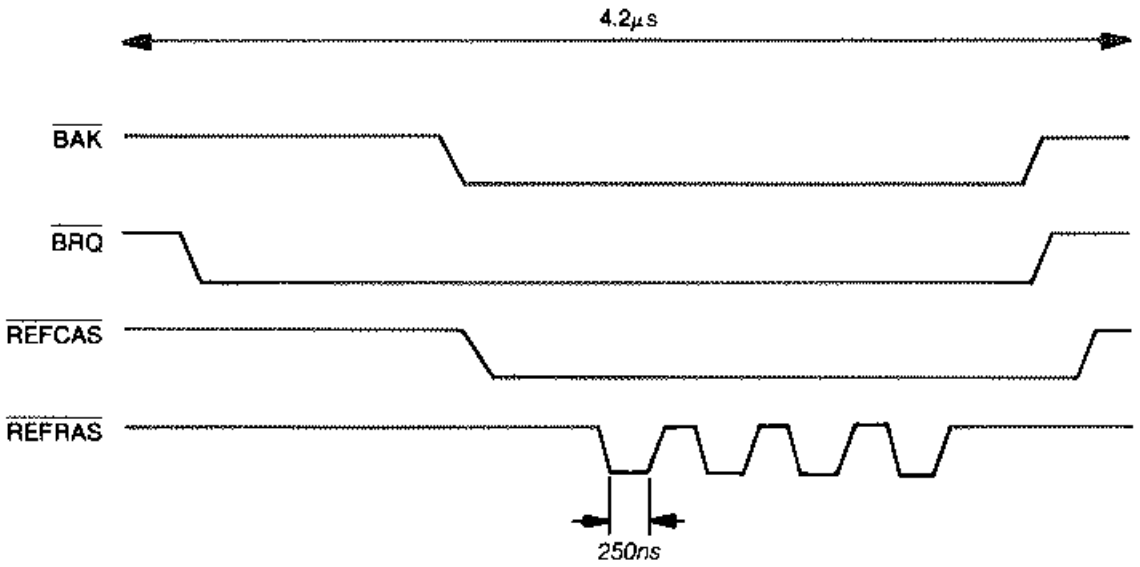


FIGURE 2-37. DRAM REFRESH TIMING CIRCUIT

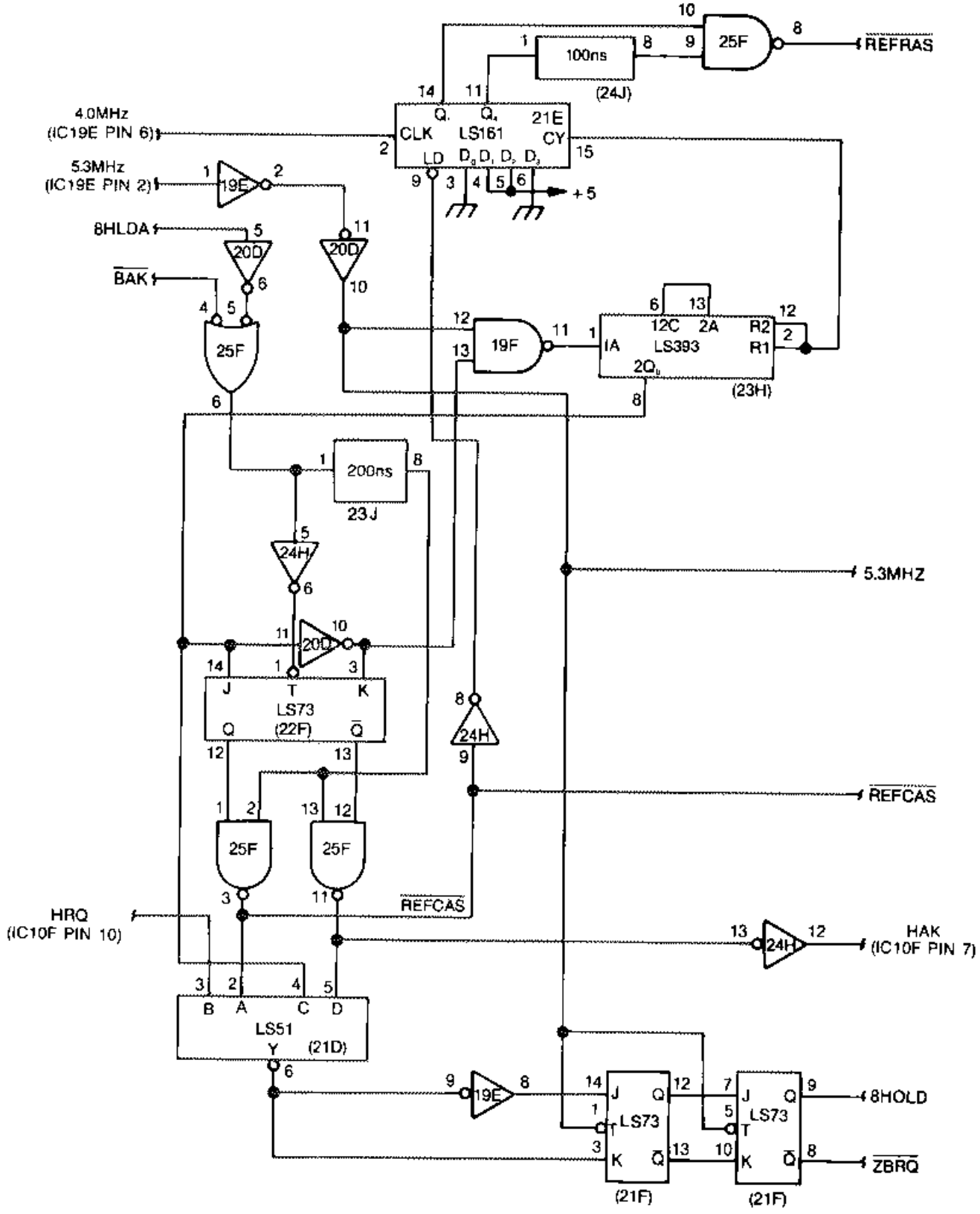


FIGURE 2-38. DRAM REFRESH TIMING CIRCUIT

2.3.2.9 DRAM RAS and Write Enable Generator Circuit (Figures 2-39 and 2-40)

The DRAM RAS and write enable ($\overline{WE}$) generator circuit coordinates the RAS signal for each DRAM bank with the refresh signal required by dynamic RAM, generating a common set of signals for controlling the DRAMs.

ICs 24E and 24F provide adequate timing margin to the signals from the 8237 DMA controller; these signals are combined by IC 24F to provide an active low to 22H pin 4 when the DMA controller begins a read or write operation from system memory.

The Z-80A memory request circuit generates a single, active low memory request signal in the M1 machine cycle for a valid memory read/write operation. Normally, the memory request signal goes low twice during the M1 cycle: once for a read/write operation and again for the Z-80A refresh cycle. Because the QX-16 uses an external refresh circuit, the circuit composed of ICs 23F, 25A, and 25E eliminates the second memory request pulse. ICs 25A and 25E provide high inputs to IC 23F when a memory request is occurring. The Z-80A clock signal loads this into IC 23F, causing the output on pin 13 to go low; the output, considered a modified Z-80A memory request ($\overline{MRQ'}$), returns to high when the memory request has ended.

IC 22H combines the modified Z-80A memory request ($\overline{MRQ'}$) signals, modified DMA controller read/write signals, and 8088 read/write signals; if any one of these goes low, an active high signal (3RAS) is output on pin 6 of IC 22H and supplied to the address multiplexer circuit. The 3RAS signal is used to generate the $\overline{RAS}$ timing signals.

IC 21H is used to generate the $\overline{RAS0}$ and $\overline{RAS1}$ timing signals that are supplied to the two groups of DRAMs. There are two identical 4-input NAND gates in IC 21H, and three identical input signals: $\overline{8INH}$, the 8088 RAS inhibit signal, $\overline{ZINH}$, the Z-80A RAS inhibit signal, and 3RAS, described above; if any of these signals goes low, the generation of a RAS timing signal is inhibited. The fourth input, address bit A18, inverted by 24H and input to pin 9 of 21H, is used to select between the two DRAM banks; when A18 is low, a $\overline{RAS0}$ is generated, and when it is high, a $\overline{RAS1}$ is generated. IC 21J is used to combine the RAS timing signals and the refresh RAS ($\overline{REFRAS}$) timing signal.

The Z-80A requires additional circuitry to generate a write signal. IC23F is clocked by the Z-80A CPU clock to latch the state of the read ($\overline{RD}$) line. This generates a high output on pin 9 of 23F when the CPU is not reading data. This output, the $\overline{RD}$ line, and the 25E pin 4 output cause a low to be generated on pin 12 of 25D when a valid memory request which is not a read cycle is received.

IC 25D is the write enable generator circuit, which combines all the write signals from the Z-80A, 8088, and 8237 to generate an active low output on pin 4 of IC 24H to indicate a valid write cycle. This signal is supplied to all of the DRAMs.

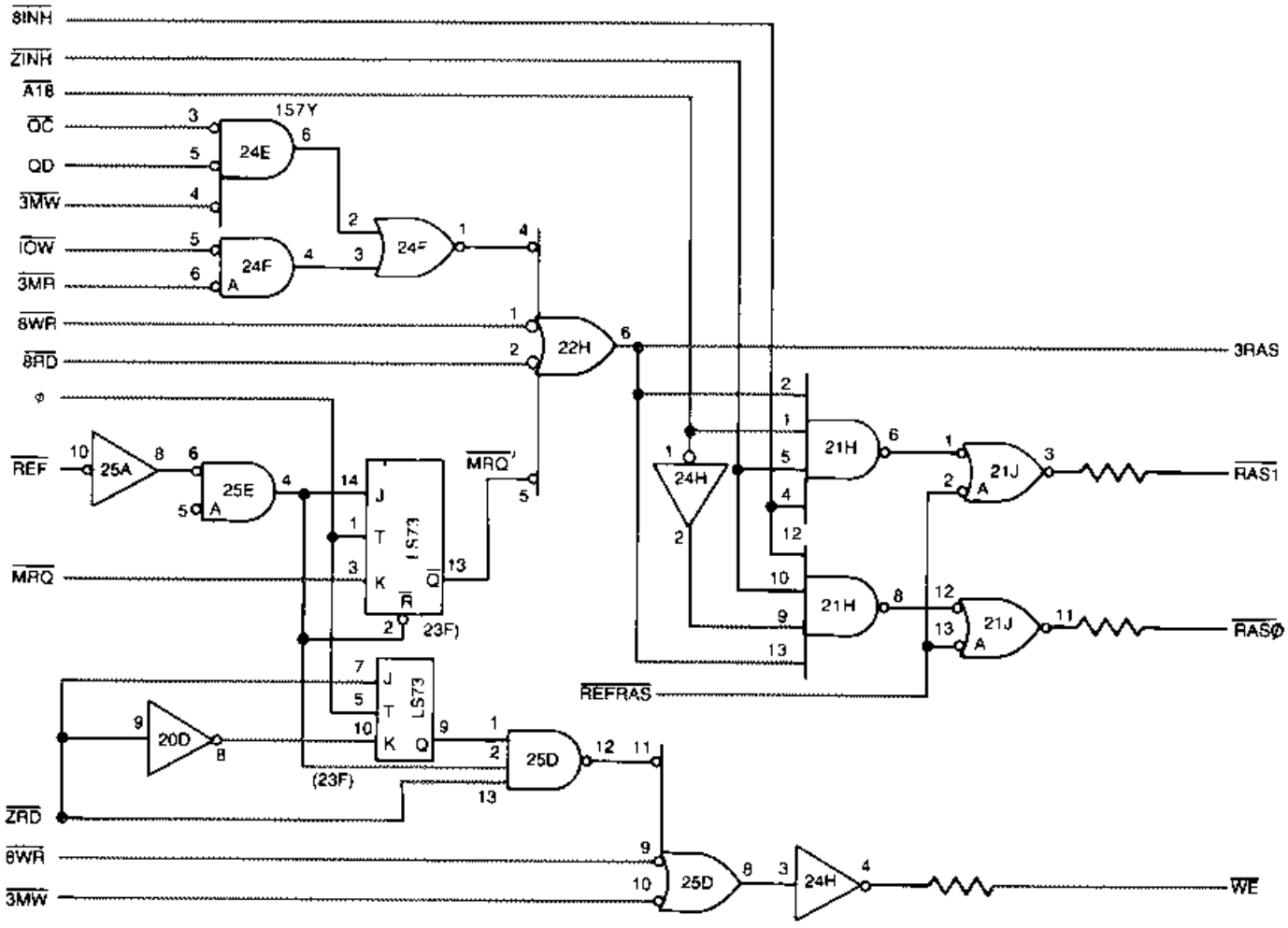


FIGURE 2-39. DRAM RAS AND WRITE ENABLE GENERATOR CIRCUIT

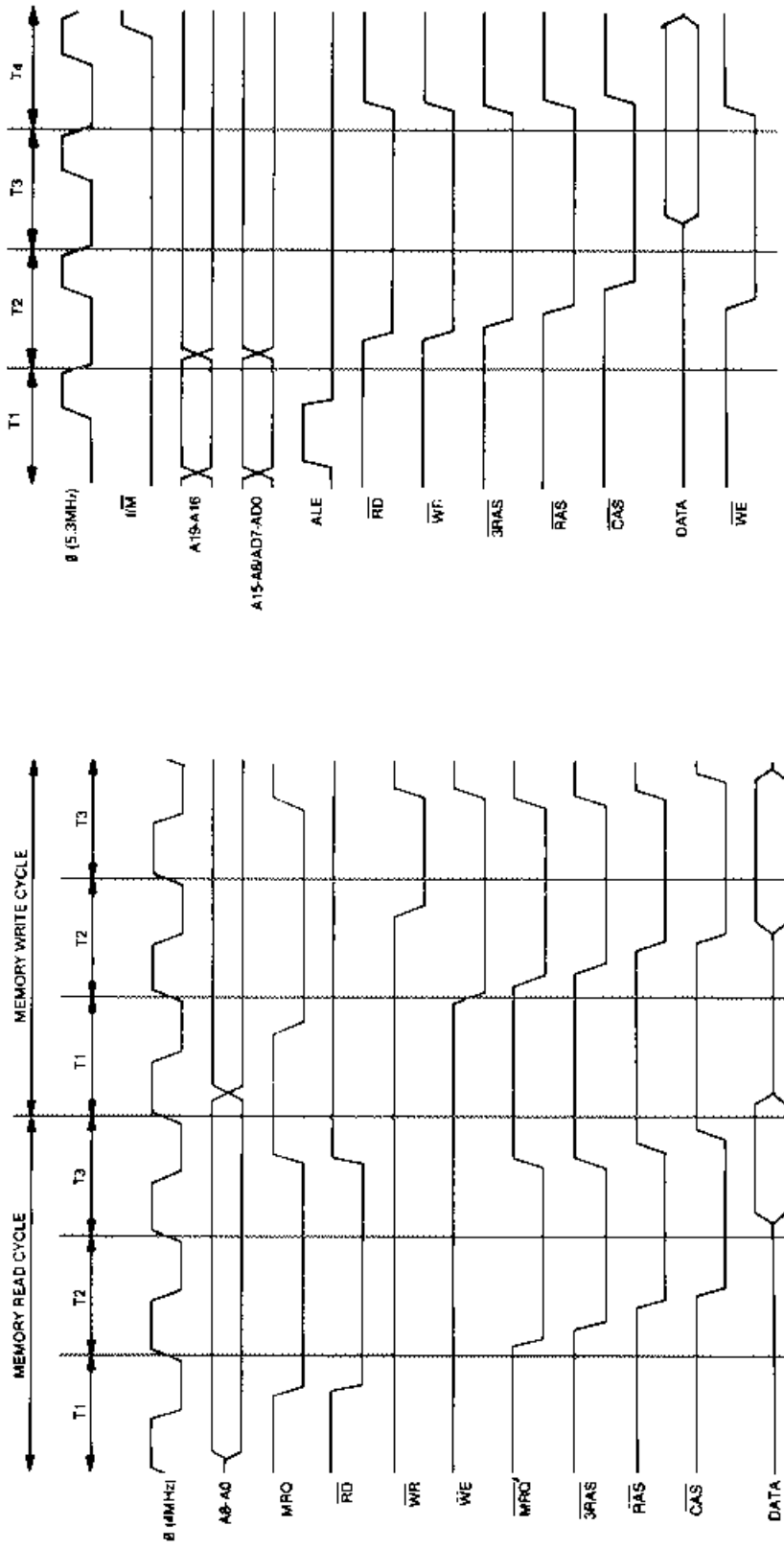


FIGURE 2-40. RAS AND WRITE ENABLE TIMING DIAGRAMS

2.3.2.10 Address Multiplexer and CAS Generator Circuit (Figures 2-41 and 2-42)

The DRAMs used in the QX-16 use a row/column matrix system to address a single memory cell. The row address strobe (RAS) signal is used to specify the active cell row; column address strobe (CAS) is used to specify the active cell column. At the intersection of these two locations is the selected memory cell. The cell value is output to DO (pin 14) during a memory read operation, and assumes the value of the DI input (pin 2) during a memory write.

The address multiplexer circuit is composed of three LS258 multiplexer ICs which are switched by a delayed RAS signal. In normal operation the address is placed on the bus and a $\overline{RAS0}$ or $\overline{RAS1}$ signal is generated. The select input of the multiplexers is low and supplies the A inputs to the Y outputs, providing the row address and $\overline{RAS}$ control signal to the correct group of DRAMs. The output on pin 12 of delay line 22J goes high 20 nanoseconds after the leading edge of the RAS signal, switching the multiplexer outputs from the A to B inputs.

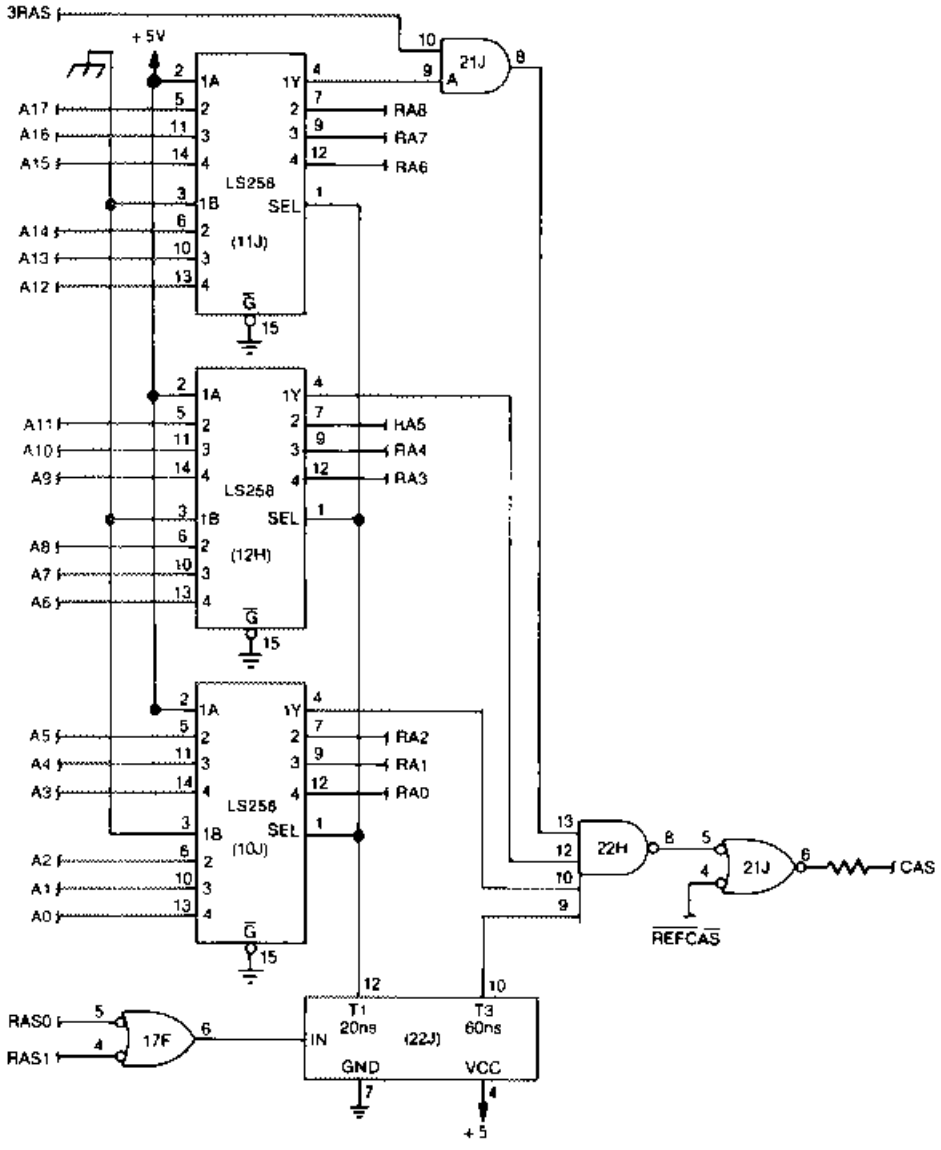


FIGURE 2-41. ADDRESS MULTIPLEXER AND CAS GENERATOR CIRCUIT

The CAS signal is generated on pin 6 of 21J under the following conditions:

1. During a refresh cycle, the refresh CAS ($\overline{\text{REFCAS}}$) signal on pin 5 of 21J causes the CAS output to go low for the entire refresh cycle.
2. When the B outputs of the multiplexers are selected, the 1Y output on pin 4 of each LS258 goes high and is applied to IC 22H with the output of 22J pin 10, which goes high 60 nanoseconds after the leading edge of the RAS signal. When all inputs are high, the output of 22H pin 8 goes low, bringing the $\overline{\text{CAS}}$ signal on pin 6 of 21J to low and providing the column address and $\overline{\text{CAS}}$ control signals to all of the DRAMs.

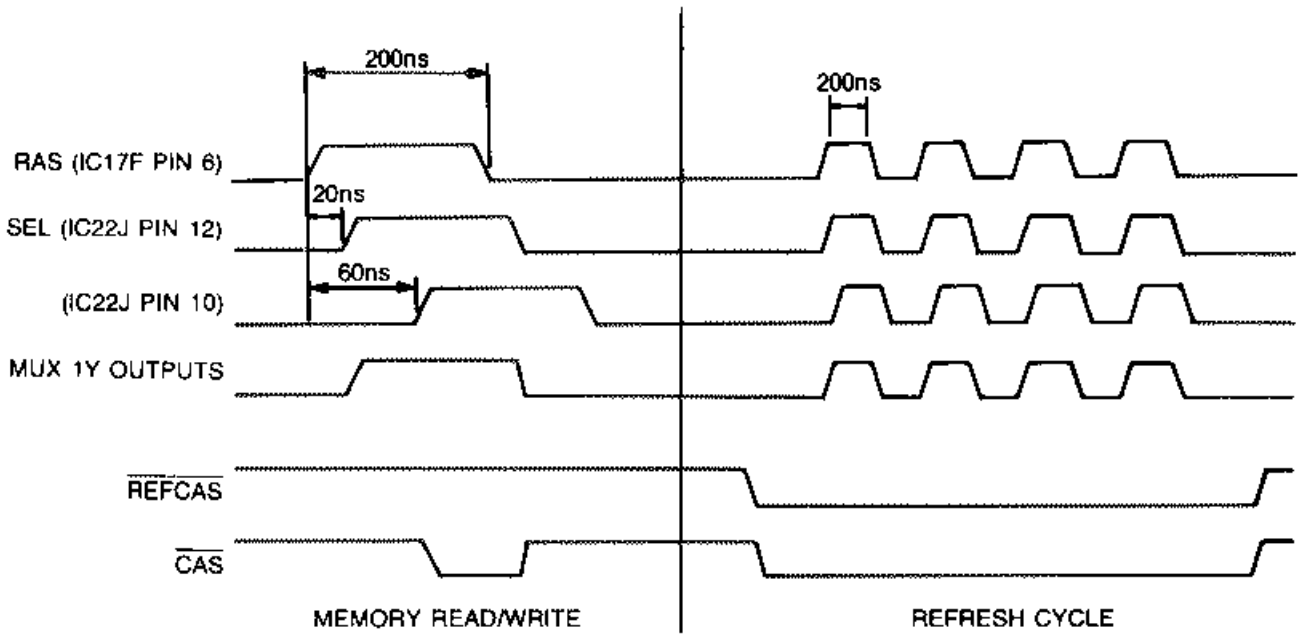


FIGURE 2-42. ADDRESS MULTIPLEXER AND CAS TIMING DIAGRAM

2.3.2.11 Z-80A DRAM Bank Select Circuit (Figure 2-43)

The Z-80A addresses the DRAM as two groups of four, 64K-byte banks via two I/O ports (Table 2-18). Each bank contains 56K bytes of DRAM dedicated to that bank and 8K bytes resident RAM (0E000H to 0FFFFH) which is common to all of the banks. The Z-80A RAS inhibit and DRAM address selector circuits always select the same region of memory for resident RAM, regardless of which bank is selected.

Port 28H determines which of the two DRAM bank sets is selected by address bit A18, which is output from the the LS259 (15F pin 6). When this signal is low, as in the power-on default condition, banks 0-3 are selected; when it is high, banks 4-7 are selected. The four most significant bits from port 18H enable one of four banks in the selected group. (Only one bank may be enabled at a time; enabling two banks causes improper bank selection.) Both I/O port outputs are supplied to the address selector circuit (Section 2.3.2.12).

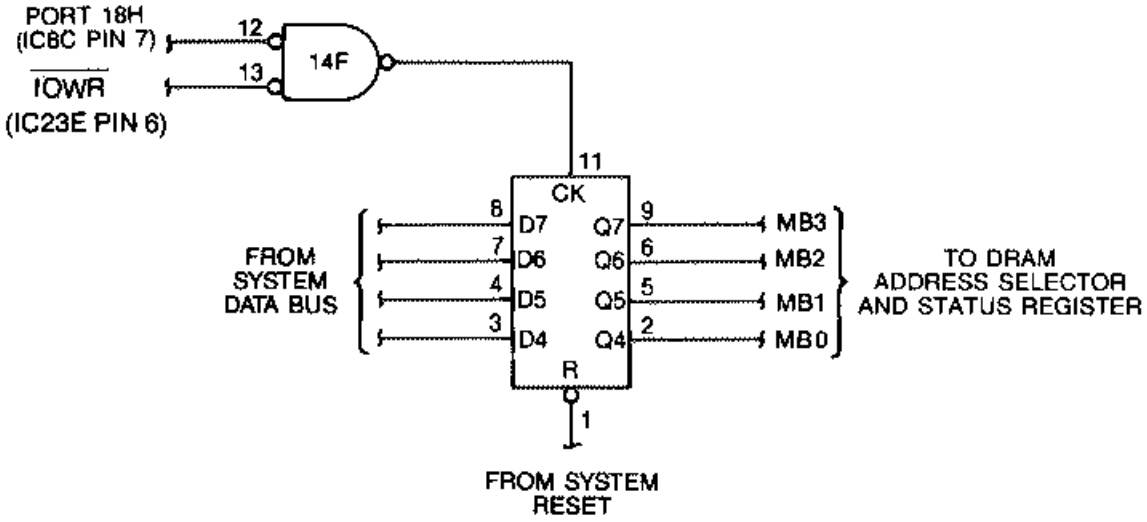


FIGURE 2-43. Z-80A DRAM BANK SELECT CIRCUIT

TABLE 2-18. Z-80A BANK SELECTION

I/O ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0	I/O ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0	SELECTED BANK
28H	0	0	0	0	0	0	0	0	18H	0	0	0	1	X	X	X	X	#0
	0	0	0	0	0	0	0	0		0	0	1	0	X	X	X	X	#1
	0	0	0	0	0	0	0	0		0	1	0	0	X	X	X	X	#2
	0	0	0	0	0	0	0	0		1	0	0	0	X	X	X	X	#3
	0	0	0	0	0	0	0	1		0	0	0	1	X	X	X	X	#4
	0	0	0	0	0	0	0	1		0	0	1	0	X	X	X	X	#5
	0	0	0	0	0	0	0	1		0	1	0	0	X	X	X	X	#6
	0	0	0	0	0	0	0	1		1	0	0	0	X	X	X	X	#7

X = Controls other functions (See Chapter 6).
NOTE: Bank 4-7 are valid only when 512K system RAM is installed.

2.3.2.12 DRAM Address Selector Circuit (Figure 2-44)

The Z-80A supplies sixteen address bits to select any location in its 64K byte address space (Table 2-19). The DRAM address selector is used to convert the output signals from the bank select circuit to the required four upper address bits, and also switches them with their 8088 equivalents if the 8088 CPU is enabled. IC 17F selects which CPU address signals are output to the system address bus. When the Z-80A is selected, the input on pin 2 goes low, causing a high output to be applied to pin 1 of the LS157 (20C) to select the B set of inputs from the Z-80A bank select circuit.

IC 14F is used to encode three of the bank select signals into the correct address. If bank 0 is selected, all inputs are low, and the upper address bits are low. The bank group select signal, from pin 6 of the LS259, is applied to the 3B input; the 3B input is switched to the 3Y output, address bit A18.

The gate input ($\overline{G}$) on pin 15 is used to ensure that the circuit is in bank 0 whenever resident RAM is selected. The $\overline{E000}$ signal is supplied by the Z-80A range select circuit, which is active low when the Z-80A accesses memory in the E000H to FFFFH range. If this input is low, the LS157 disables the outputs, bringing them all low.

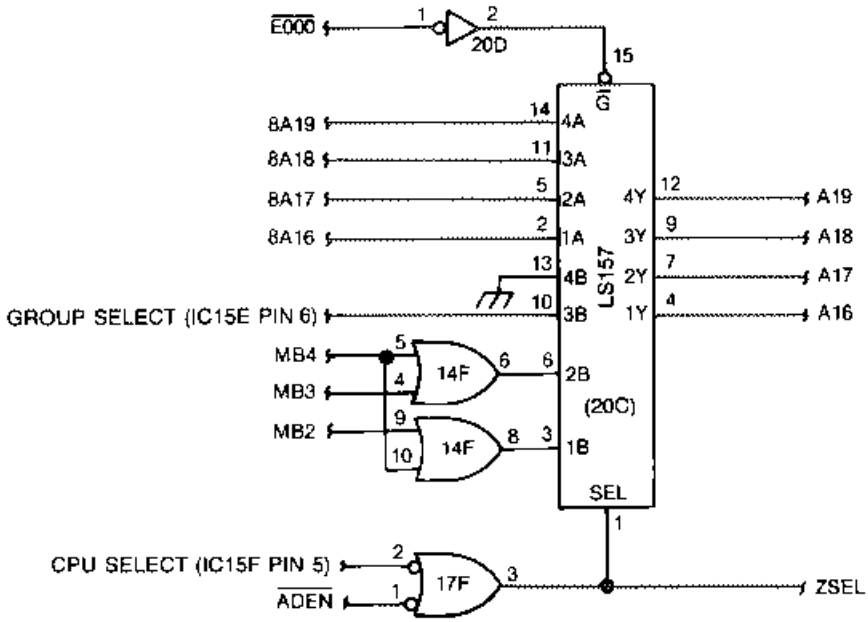


FIGURE 2-44 DRAM ADDRESS SELECTOR CIRCUIT

TABLE 2-19. Z-80A BANK LOCATION IN 8088 ADDRESS SPACE

Z-80A BANK NUMBER	8088 ADDRESS LOCATION
0	00000H — — 0FFFFH
1	10000H — — 1FFFFH
2	20000H — — 2FFFFH
3	30000H — — 3FFFFH
4	40000H — — 4FFFFH
5	50000H — — 5FFFFH
6	60000H — — 6FFFFH
7	70000H — — 7FFFFH

Z 80A resident memory is always located on bank 0 at E000 FFFFH

2.3.3 I/O Control Circuits

The I/O control circuits support the I/O devices, providing select signals to each, and are needed to generate read/write timing pulses. Differences in 8088 and Z-80A architecture necessitate, in some instances, dual I/O circuitry to provide the required control signals.

2.3.3.1 I/O Write Signal Generator (Figure 2-45)

The write signal generator provides a low output from pin 6 of IC 23E to initiate an I/O write operation in Z-80A, 8088, or 8237 DMA modes. An I/O write in any of these modes causes one of the three inputs of this gate to go high, inducing a low output.

In Z-80 operation mode IC 23E pin 12 goes high when all three inputs are low. The signal input at pin 2 causes the I/O write pulse-width to be a maximum of two clock cycles.

In 8088 mode an I/O write pulse is generated whenever the I/$\overline{M}$ pin of the CPU is high during a write operation. In 8237 DMA mode, when the DMA controller is performing a memory to output transfer, the $\overline{MR}$ pin of the selected 8237 goes low, initiating a read operation from system memory. Inputs on pin 9 and 10 of 23E, in conjunction with the $\overline{MR}$ signal, cause output at pin 8 to go high for three clock cycles, resulting in a low at pin 6 of IC 23E, which loads the data into the selected I/O device.

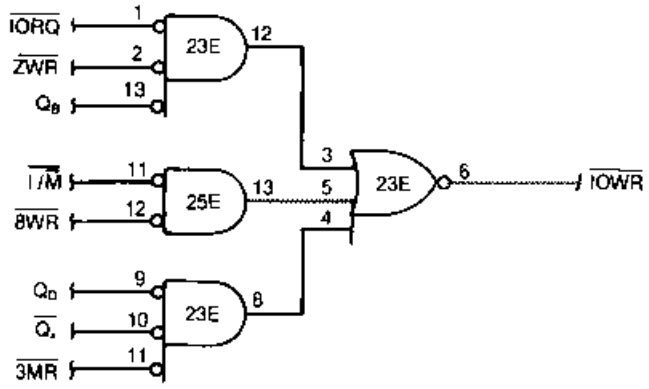


FIGURE 2-45. WRITE SIGNAL GENERATOR

2.3.3.2 I/O Read Signal Generator (Figure 2-46)

The read signal generator provides a low output from pin 12 of IC 24E for I/O read operations in Z-80A, 8088, or 8237 DMA operation modes, causing one of the three inputs of this gate to go high, resulting in a low output.

In Z-80 operation mode IC 25E pin 10 goes high when both inputs on pin 8 and 9 are low.

In 8088 mode an I/O read pulse is output whenever the $\overline{M}$/I pin of the CPU is high during a read operation.

In 8237 DMA mode, when the DMA controller is performing a transfer to memory from an input device, the $\overline{MW}$ pin of the selected 8237 goes low, initiating a read operation from the selected I/O device. Inputs on pin 9 and 10 of 24E, in conjunction with the $\overline{MW}$ signal, cause the output on pin 8 to go high for three clock cycles, resulting in a low at pin 12 of IC 24E, which loads the data from the selected I/O device into the specified memory location.

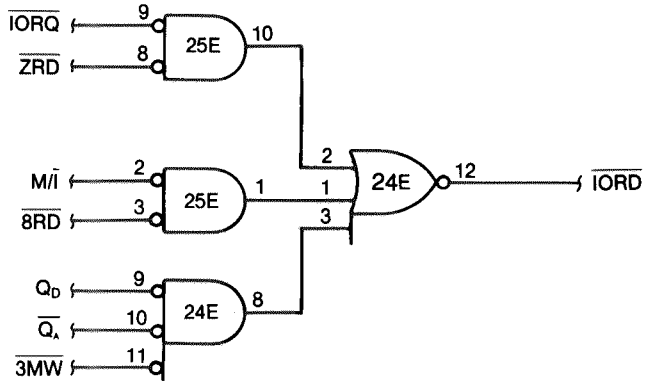
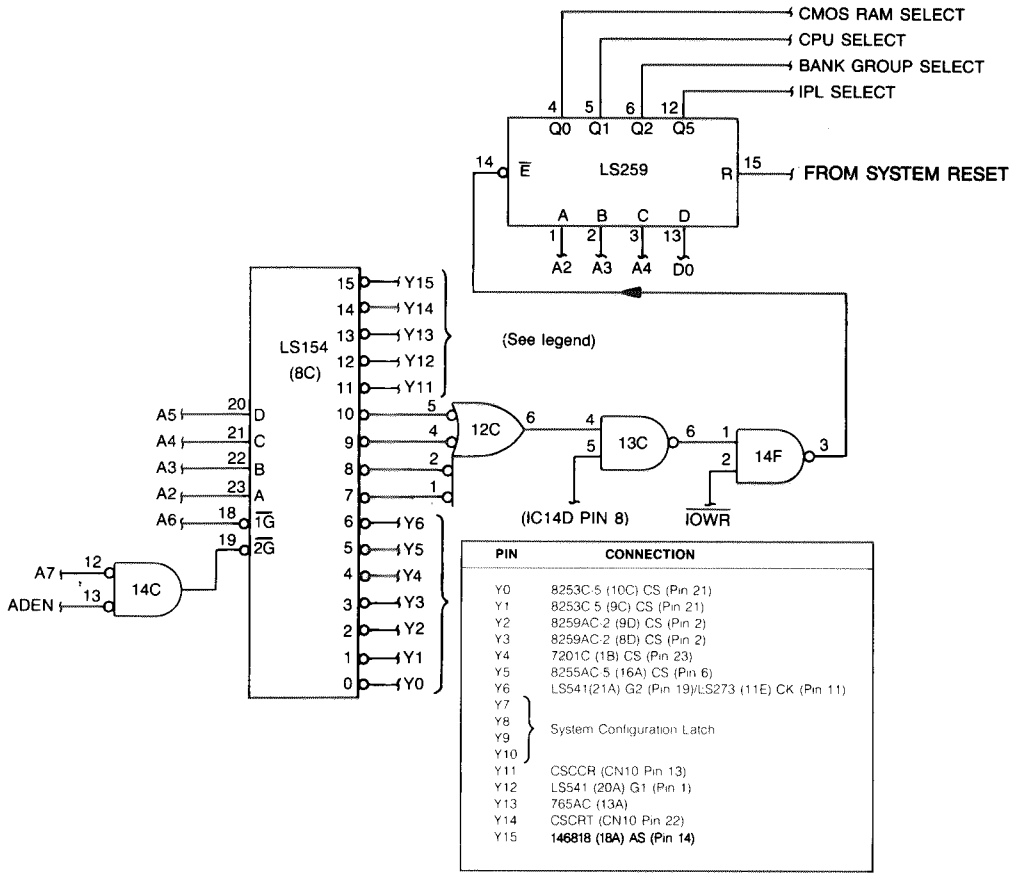


FIGURE 2-46. READ SIGNAL GENERATOR

2.3.3.3 I/O Address Decoder (Figure 2-47)

The I/O selector, LS154 (8C), decodes all of the base I/O port locations. This circuit decodes address bits A2 through A5 to set one of its sixteen outputs low, supplying chip select signals, $\overline{CS}$, for the various I/O functions on the APX-ISYM board. Table 2-20 describes the I/O address map.

The I/O selector is enabled only when pins 18 and 19 are low. Pin 18 is tied to address bit A6 and pin 19 is a combination of address bit A7 and the ADEN outputs of the master and slave 8237 DMA controllers. Therefore, the I/O selector is disabled when A6, A7, or either of the ADEN signals is high.



PIN	CONNECTION
Y0	8253C-5 (10C) CS (Pin 21)
Y1	8253C-5 (9C) CS (Pin 21)
Y2	8259AC-2 (9D) CS (Pin 2)
Y3	8259AC-2 (8D) CS (Pin 2)
Y4	7201C (1B) CS (Pin 23)
Y5	8255AC-5 (16A) CS (Pin 6)
Y6	LS541(21A) G2 (Pin 19)/LS273 (11E) CK (Pin 11)
Y7	System Configuration Latch
Y8	
Y9	
Y10	
Y11	CSCCR (CN10 Pin 13)
Y12	LS541 (20A) G1 (Pin 1)
Y13	765AC (13A)
Y14	CSCRT (CN10 Pin 22)
Y15	146818 (18A) AS (Pin 14)

FIGURE 2-47. I/O ADDRESS DECODER AND SYSTEM CONFIGURATION LATCH

TABLE 2-20. I/O ADDRESS MAP

HEX BASE	OFFSET 0	1	2	3
0 0	Speaker timer	SOFT timer No. 2	SOFT timer No. 1	8253 No. 1 command
0 4	Speaker frequency	Keyboard clock	RS-232C clock	8253 No. 2 command
0 8	8259 (Master)		RESERVED	RESERVED
0 C	8259 (Slave)			
1 0	Keyboard data	RS-232C data	Keyboard command	RS-232C command
1 4	Printer data	Printer status/ bank group	Printer control	8255 command
1 8	DIP switch status/bank select			
1 C	IPL select			
2 0	CMOS RAM select			
2 4	Z80A/8088 select			
2 8	Memory group select			
2 C	CRT circuit board type	R.G.B. plane select Q10 CMS	RESERVED	
3 0	FDD motor control/FDC and memory bank status	RESERVED		
3 4	FDC status/command	FDC data	RESERVED	
3 8	GDC parameter status	GDC command/data	APX-iGGS zoom/ enable	RESERVED
3 C	RTC data	RTC address	RESERVED	
4 0 4 4 4 8 4 C	8327 DMA CONTROLLER #1			
5 0 5 4 5 8 5 C	8327 DMA CONTROLLER #2			
6 0 6 4 6 8 6 C	RESERVED			
7 0 7 4 7 8 7 C	RESERVED			

NOTE Refer to Chapter 6 for more information on 8088 addresses used in conjunction with the APX-iCRT video board

2.3.3.4 System Configuration Latch

The LS259 system configuration latch (IC 15F) is used to establish the signal conditions which enable the Z-80A or 8088 CPU and associated memory devices. The bit-addressable latch, illustrated in Figure 2-47 with the I/O decoder, is addressed as a series of I/O ports (see Table 2-21). At power-on the chip is reset by the system reset pulse to select the Z-80A, IPL, and banks 0-3 of DRAM.

TABLE 2-21. SYSTEM CONFIGURATION LATCH FUNCTIONS

I/O ADDRESS	FUNCTION	PIN NO. IC15F	STATE HIGH (1)	LOW (0)
1CH	Z-80A IPL enable	12	IPL disabled	IPL enabled
20H*	CMOS RAM select	4	enabled	disabled
24H	Active CPU select	5	8088 active	Z-80A active
28H**	Upper/lower bank select	6	Banks 4-7	Banks 0-3

*This function is valid only when the Z-80 CPU is active.
**Port 18H is used to select one of the four active banks. Valid only in Z-80A mode.

2.3.4 Programmable Devices

The function of each of the programmable devices is determined by the values written into its command registers. This section describes the default functions; for additional information on these devices refer to Chapter 6.

2.3.4.1 8253 Programmable Interval Timer (Figures 2-48 and 2-49)

Two 8253 programmable interval timers (9C/10C) are located on the APX-ISYM circuit board. Each of these counters is dedicated to a specific function within the system, as described in Table 2-22.

Counters 1 and 2 of 9C generate the baud rate clocks that are supplied to the 7201 multi-protocol serial controller for the keyboard and RS-232C interfaces. Both of these counters are programmed to operate as square wave generators. Counters 1 and 2 of 10C are used for interrupt timers and are not configured in the IPL; the two interrupt channels assigned to the timers are disabled. The function of these devices can be defined by the resident operating system or application program. Tables 2-23 and 2-24 describe the functions of the 8253.

TABLE 2-22. 8253 PROGRAMMABLE TIMER FUNCTIONS

IC	COUNTER NO.	GATE	CLOCK	FUNCTION
9C	0	+5V	1.99MHz	Speaker frequency
9C	1	+5V	1.99MHz	Keyboard clock
9C	2	+5V	1.99MHz	RS-232C baud rate
10C	0	Port 18H, bit 0	Keyboard clock	Speaker duration
10C	1	+5V	Keyboard clock	Interrupt timer
10C	2	Port 18H, bit 2	1.99MHz	Interrupt timer

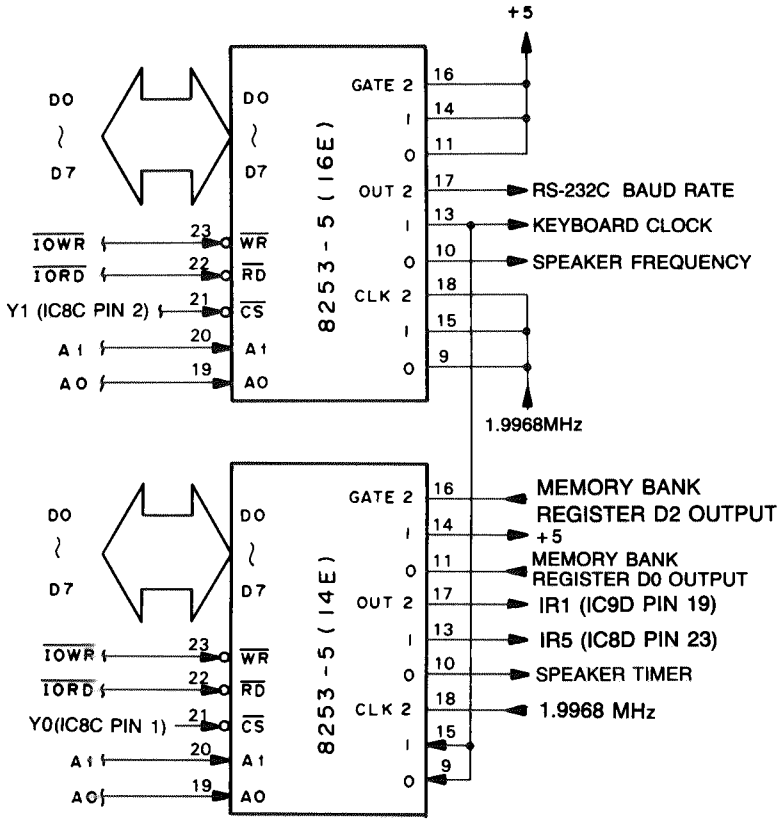


FIGURE 2-48. 8253 PROGRAMMABLE INTERVAL TIMER CIRCUIT

TABLE 2-23. 8253 PIN DESCRIPTION

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1-8	D7—D0	IN/OUT	Connected to data bus. Used to read/write counter values and configure individual counter modes.
23	WR	IN	Connected to system IOWR signal. Loads selected internal register when input is low.
22	RD	IN	Connected to system IORD signal. Places contents of selected internal register on bus when input is low.
21	CS	IN	Connected to I/O decoder. This input must be low for any read or write operation to the device.
19,20	A1,A0	IN	Connected to address bus. These inputs, in conjunction with RD, WR, CS, determine which internal register is selected.
9,15,18	CLK 0-2	IN	Counter Inputs.
10,13,17	OUT 0-2	OUT	Output signal is dependent on programmed counter function. See text for details.
11,14,16	GATE 0-2	IN	Used to control counter. Some of the counters are always enabled (+5V) and other are triggered by port 18H.

TABLE 2-24. 8253 INTERNAL REGISTER SELECTION

CS	RD	WR	A1	A0	FUNCTION
0	1	0	0	0	Loads to counter #0
0	1	0	0	1	Loads to counter #1
0	1	0	1	0	Loads to counter #2
0	1	0	1	1	Control word
0	0	1	0	0	Reads from counter #0
0	0	1	0	1	Reads from counter #1
0	0	1	1	0	Reads from counter #2
0	0	1	1	1	No operation (high impedance)
1	X	X	X	X	Disabled (high impedance)
0	1	1	X	X	No operation (high impedance)

Sound Generator Circuit

Two of the counters are used to supply inputs for the sound generator circuit, shown in Figure 2-49. The values programmed into counter 0 of 9C and counter 0 of 10C determine the frequency and duration of sound generated from the internal speaker. Counter 0 of IC 9C is configured as a square wave generator; counter 0 of 10C is configured as a one shot which is triggered by bit 0 of port 18H.

When pin 10 of 13C is brought low, the speaker frequency is output on pin 8 (13C) under two conditions: 1) setting bit 2 of port 18H to high causes sound to be generated continuously, and 2) a transition from high to low on bit 0 of port 18H causes sound to be generated for the duration specified by the programming of counter 0 of 10C.

The output on pin 8 (13C) is processed by the wave-shaping circuit consisting of R48, R49, C27 and IC 4C. The output of this circuit is input to the power amplifier consisting of C1, R50, VR1, C90, C16 and IC 5C.

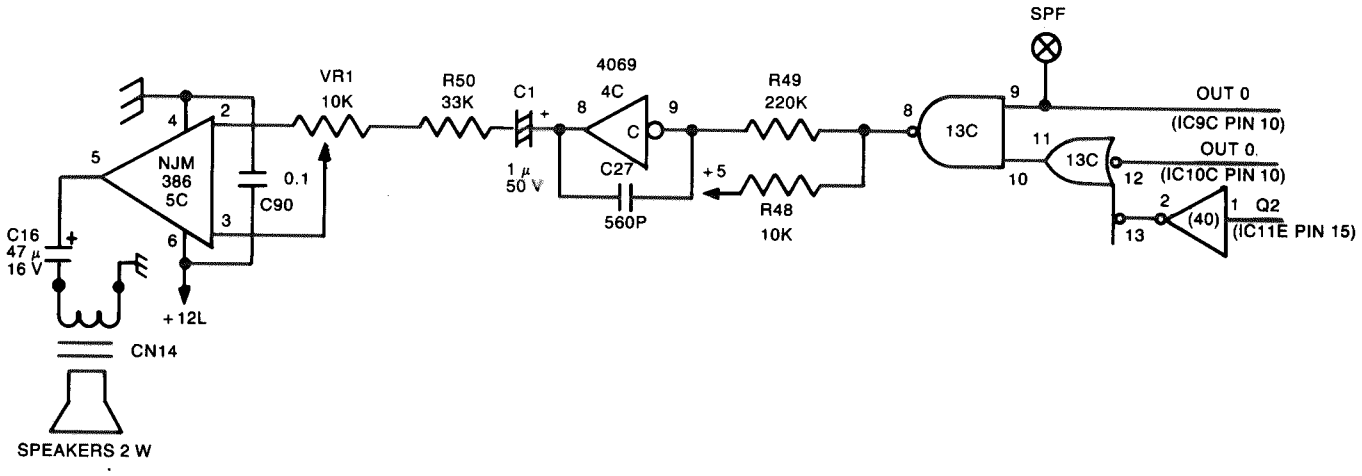


FIGURE 2-49. SOUND GENERATOR CIRCUIT

2.3.4.2 7201 Multi-Protocol Serial Controller (Figure 2-50 through 2-53)

The 7201 multi-protocol serial controller (MPSC) is a very flexible, two-channel serial interface chip responsible for communication with the keyboard and external devices. The 7201 converts data from the CPU into a serial bit stream, and converts serial input data to a format compatible with the CPU.

The 7201 has two channels: channel A is reserved for synchronous communication between the system unit and the keyboard; channel B is available as a general purpose RS-232C serial interface. Refer to Tables 2-25 through 2-27, and to Chapter 6 for additional information on configuration of the 7201 in the QX-16 by the IPL firmware.

The operative CPU (Z-80A/8088) communicates with the serial controller via the 8-bit data bus. The 7201 interrupt signal (INTR, pin 28) is connected into the master interrupt controller circuit (IC 9D pin 22) to allow fast response. (Software design determines the optimal use of this feature.)

The 7201 has 23 internal registers,which configure the device, provide status signals, and buffer serial data for the host CPU. Eight basic registers are selected by various combinations of the B/$\overline{A}$, C/$\overline{D}$, $\overline{WR}$, $\overline{RD}$ and $\overline{CS}$ signals. The extra registers used to configure the device are accessed via software. Refer to Table 2-27 for a description of the eight basic registers; refer to Chapter 6 for more information on the 7201.

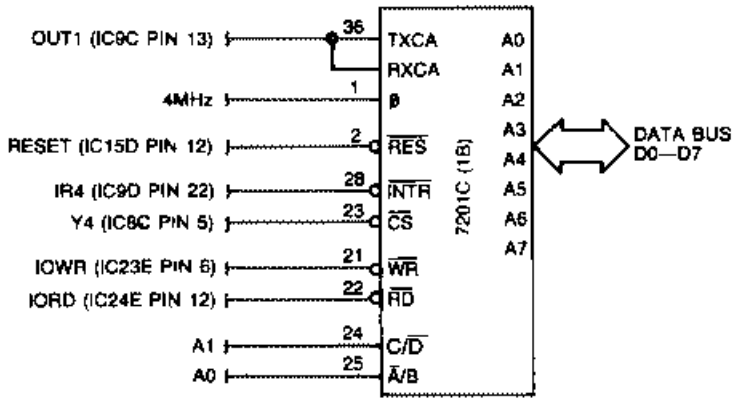


FIGURE 2-50. CPU BUS TO 7201 CIRCUIT

TABLE 2-25. 7201 BASIC REGISTER SELECTION

C/$\overline{D}$	$\overline{WR}$	$\overline{RD}$	$\overline{CS}$	$\overline{A}$/B	CHANNEL	FUNCTION
0	0	1	0	0	A	Writing transmission data
				1	B	
0	1	0	0	0	A	Reading received data
				1	B	
1	0	1	0	0	A	Writing the command/parameter register (WR0-7)
				1	B	
1	1	0	0	0	A	Reading from the status/vector register (RR0-2)
				1	B	

Channel A: Keyboard Interface

All output signals to the keyboard are driven by 7406 open-collector TTL inverters, and the receive data input is buffered by a 4584 CMOS inverter (Figure 2-51).

Communication with the keyboard is performed synchronously at 1200 baud. Receive data on pin 34 (RxDA) is sampled on the leading edge of the receive clock signal, pin 35 (RxCA) of IC 1B. Transmitted data on pin 37 (TxDA) is sent on the trailing edge of the transmit clock signal, pin 36 (TxCA) of IC 1B.

The keyboard power (+12V) is momentarily switched off whenever a system reset occurs, causing the keyboard to be re-initialized. Pin 9 of IC 12D is connected to the system reset signal; when this input goes low, the output on pin 8 goes high, turning off transistor Q4 via IC 1C.

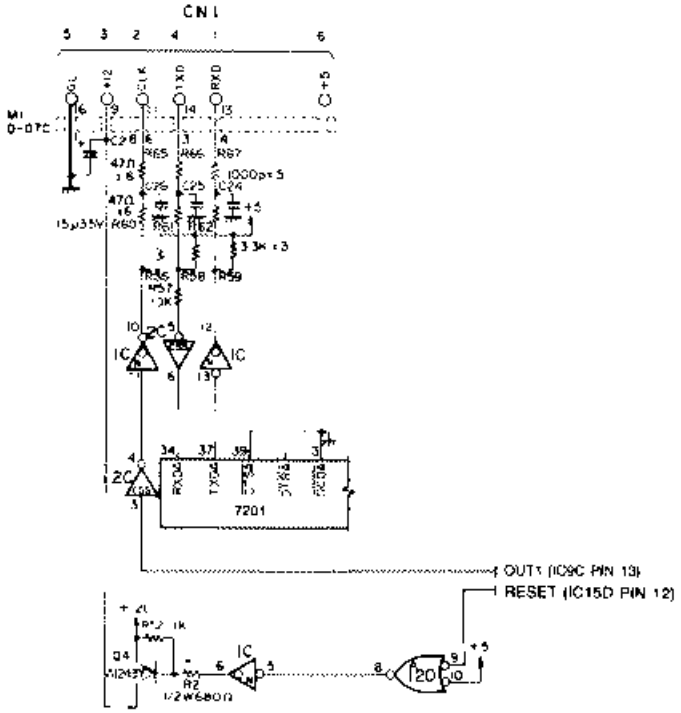


FIGURE 2-51. KEYBOARD INTERFACE CIRCUIT

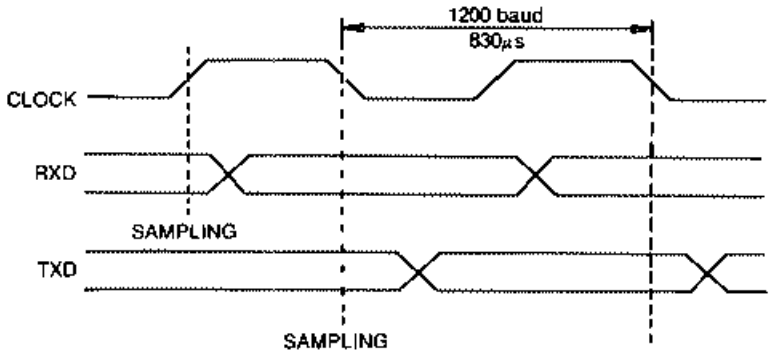


FIGURE 2-52. KEYBOARD TIMING DIAGRAM

Channel B: RS-232C Serial Interface

IC 4A (Figure 2-53) is a 75188 line-driver which provides sufficient signal level for the outputs to be compatible with the RS-232C standard. ICs 1A and 3A are 75189A line-receivers which convert incoming RS-232C signals to TTL signal levels compatible with the internal circuitry.

The baud rate for the RS-232C port is determined by counter 2 in IC 9C, or externally, based on the jumper settings described in Table 2-26. The RS-232C interface can be used for most applications by referring to the pinout and signal description for the RS-232C interface in Chapter 6. Non-standard devices or special applications can usually be accommodated by careful use of the jumpers located at the rear of the APX-ISYM board, under the option slot cover.

NOTE: *The DSR (Data Set Ready) signal on pin 6 of CN2 is not input to the 7201; it is read as Port B bit 0 (PB0) of the 8255 programmable I/O controller.*

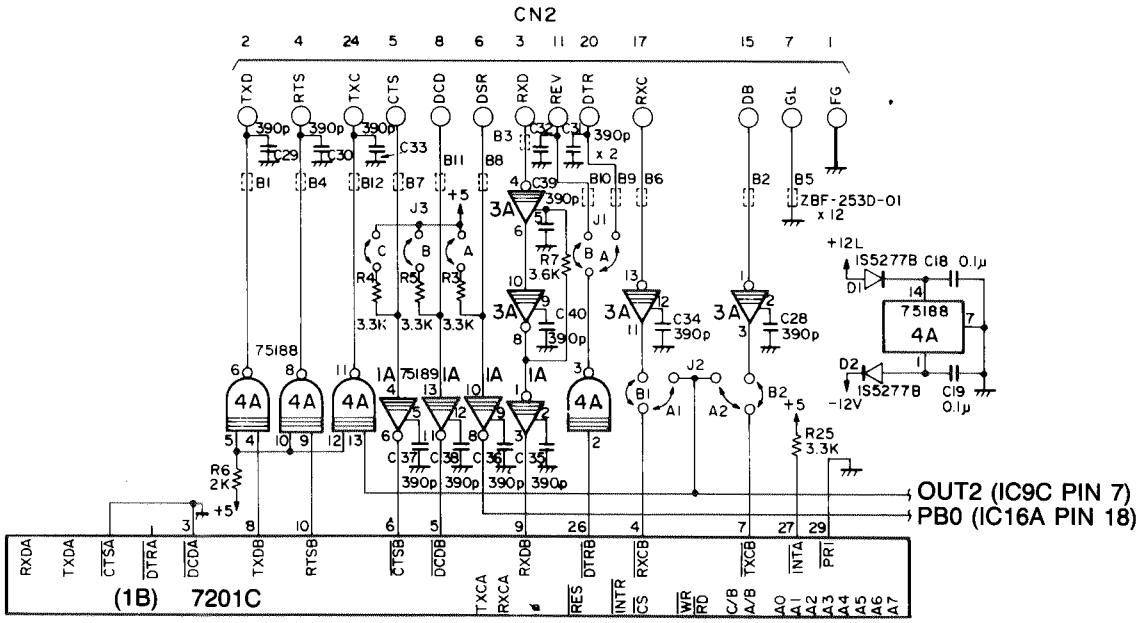


FIGURE 2-53. RS-232C INTERFACE CIRCUIT

TABLE 2-26. RS-232C CONFIGURATION JUMPERS

JUMPER		SIGNAL	DIRECTION	FUNCTION
J1	A	DTR	IN	Data Terminal Ready. Normally closed.
	B	REV	IN	Reverse channel.
J2*	A1	Input of RXCk		Selects the internal baud rate clock. Normally closed.
	A2	signal from	—	
	B1	RXC	IN	Selects external inputs as baud rate clock. Normally
	B2	DB	IN	open.
J3	A	DSR	IN	Pull-up of the control line. Space status is set with the
	B	DCD	IN	pull-up on. Normally closed.
	C	CTS	IN	

*Only the A or B set of pins J2 should be jumpered, not both.

TABLE 2-27. 7201 PIN DESCRIPTION

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
12-19	D0—D7	IN/OUT	8-bit data bus used for transmission of data, command, and status between the 7201 and the CPU.
28	INTR	OUT	Interrupt request signal output.
27	INTA	IN	Interrupt acknowledge input.
25	B/A	IN	Specifies the channel for read/write operations. Connected to A0.
24	C/D	IN	Indicates that the information on the data bus is data, command, or status. Connected to A1.
23	CS	IN	Enables data transfer to 7201. Connected to I/O decoder Y4 output.
2	RESET	IN	Reset input. Connected to system input.
22	RD	IN	Connected to system I/O read signal.
21	WR	IN	Connected to system I/O write signal.
1	*	IN	Clock input. Connected to Z-80A clock. (3.99MHz)
4 35	RXC	IN	Receive clock. Channel A — OUT1 (IC 9C pin 13) Channel B OUT2 (IC 9C pin 17)
7.36	TXC	IN	Transmit clock: Channel A — OUT1 (IC 9C pin 13) Channel B — OUT2 (IC 9C pin 17)
6.39	CTS	IN	Indicates transmission permission from an external device and controls data transmission.
26.31	DTR	OUT	Informs the receiving device that the transmitting communication channel is ready.
9.34	RXD	IN	Serial data line for received data
8 37	TXD	OUT	Serial data line for transmitted data.
10.38	RTS	OUT	Transmission permission from an external device.
3.5	DCD	IN	Indicates transmission permission from an external device.

2.3.4.3 8259 Programmable Interrupt Controller (Figures 2-54 through 2-56)

Two 8259 programmable interrupt controllers (8D/9D), connected as shown in Figure 2-54, provide 13 interrupt inputs or levels. The interrupt controllers operate in a master-slave arrangement with IC 9D acting as the master. These two devices are configured differently depending upon the active CPU. (Refer to Tables 2-28 and 2-29.)

When a valid interrupt condition is detected, the master (9D) outputs a high interrupt ($\overline{INT}$) directly to the interrupt (INTR) input on the 8088 CPU, or through an inverter (20D) to the Z-80A interrupt ($\overline{INT}$) input, and the active CPU then responds to the interrupt request.

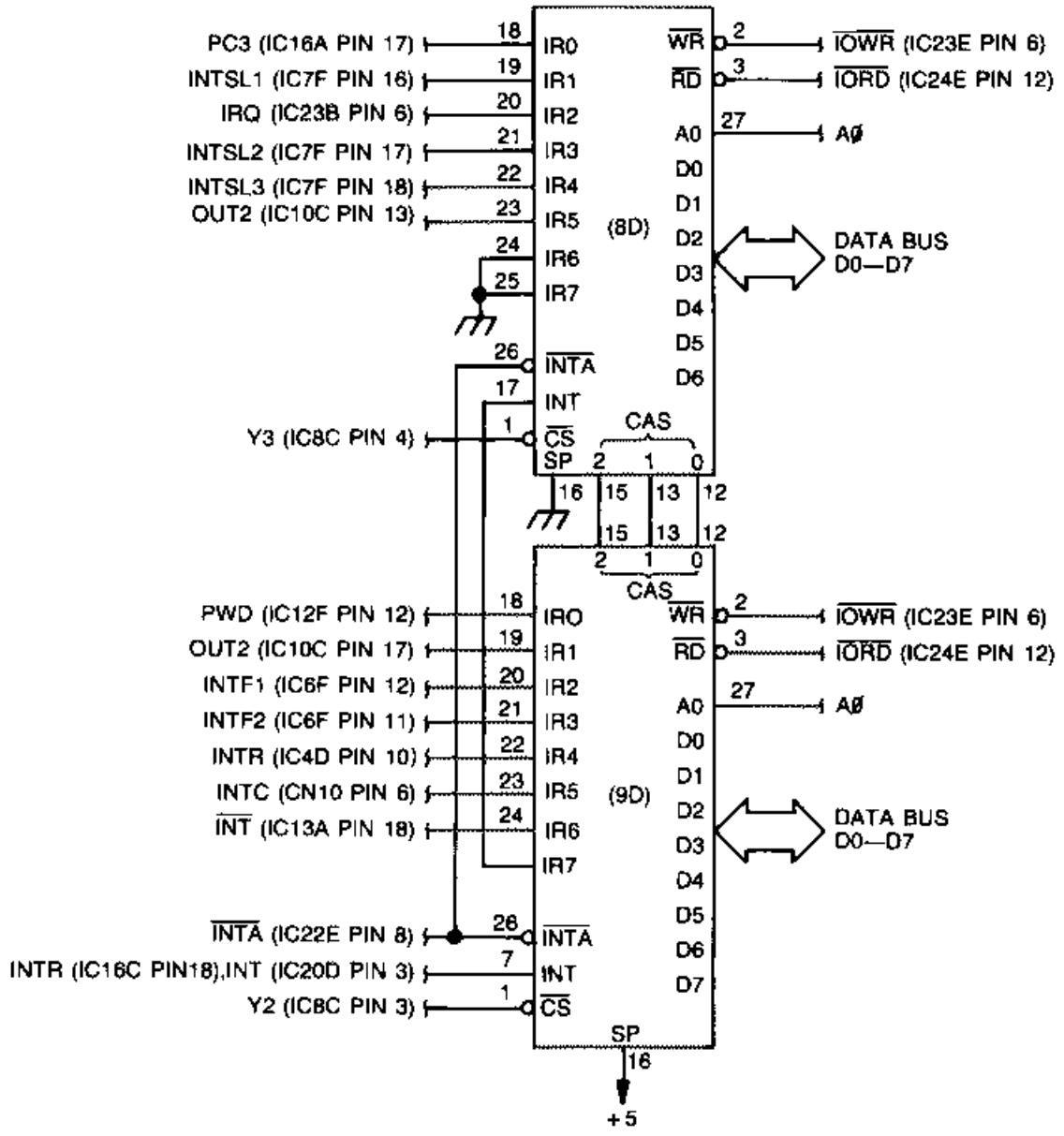


FIGURE 2-54. 8259 PROGRAMMABLE INTERRUPT CONTROLLER CIRCUIT

TABLE 2-28. 8259 PIN DESCRIPTION

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	CS	IN	RD and WR are valid when CS is low. Note that INTA is not affected by this signal.
4-11	D0—D7	IN/OUT	In read mode, these terminals output 8 bits of data from the status register or interrupt vector; in write mode, commands are written in
16	SP	IN	Determines whether the 8259 is to operate as a master (SP = 1) or a slave controller (SP = 0).
27	A0	IN	Along with signals CS, WR, and RD, this is used to write commands or read contents of a register.
12,13,15	CAS0—CAS2	IN/OUT	Output terminals when the 8259 is used as a master (SP = 1) and input terminals when it is used as a slave (SP = 0). To control a system of more than one 8259, the CAS lines form the bus of the 8259s.
17	INT	OUT	When the 8259 requests interrupt, INT goes high to deliver an interrupt request to the CPU or master 8259.
26	INTA	IN	Permits 8259 interrupt vector data output. This operation is performed in the sequence of INTA generated by the CPU.
18-25	IR0—IR7	IN	These terminals are asynchronous inputs. IR0 has the highest interrupt priority by default.

TABLE 2-29. 8259 INTERRUPT LEVELS

CONNECTION		INTERRUPT CAUSE	PRIORITY
Master	IR0	Power down detection interrupt	High-order
	IR1	Software timer #1 interrupt	
	IR2	External (option) interrupt INTF 1	
	IR3	External (option) interrupt INTF 2	
	IR4	Keyboard/RS-232C interrupt	
	IR5	Unused	
	IR6	Floppy controller interrupt	
	IR7	Slave controller	
Slave	IR0	Printer interrupt	
	IR1	External (option) interrupt #1 - INTSL	
	IR2	Calendar clock interrupt	
	IR3	External (option) interrupt #2 - INTSL	
	IR4	External (option) interrupt #3 - INTSL	
	IR5	Software timer interrupt #2	
	IR6	Unused	
	IR7	Unused	Low-order

Interrupt Acknowledge Circuit

The Z-80A and 8088 CPUs each use different control lines to signal acknowledgement of an interrupt. The circuitry composed of IC 22D, 22E, 23D,and 24E (Figure 2-55) is necessary to implement a standard interrupt acknowledge ($\overline{INTA}$) for the 8259s.

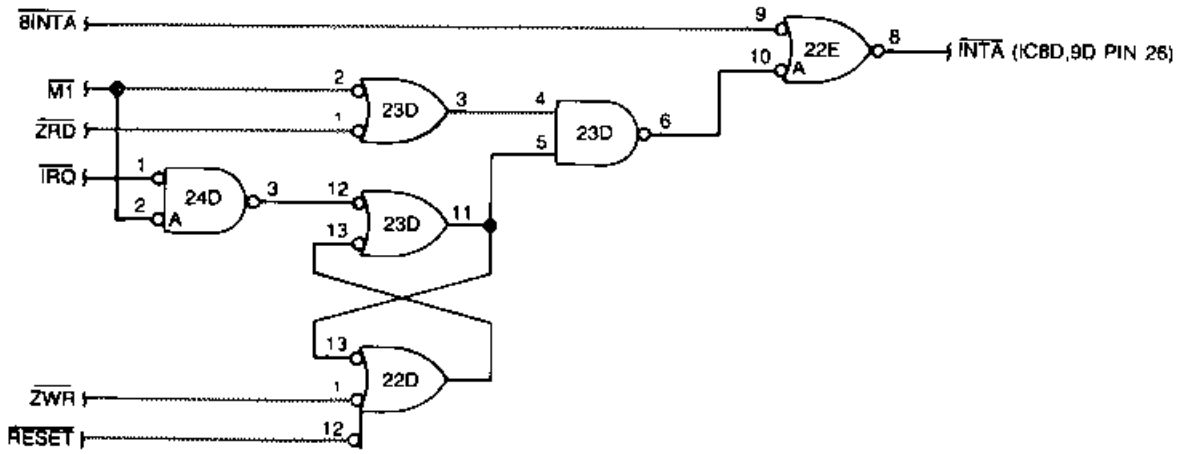


FIGURE 2-55. INTERRUPT ACKNOWLEDGE CIRCUIT

Interrupt Response Sequence

NOTE: *The following describes the interrupt response sequence when the Z-80A is set in interrupt mode 0 and the 8259 controllers are in the default state set by the IPL. The first three steps of the response sequence are identical for either Z-80A or 8088 operation. Refer to Figure 2-56 for a timing diagram of the interrupt response sequence.*

1. One or more of the interrupt request lines (IR0-7) are set high, which sets the corresponding bits in the interrupt request register (IRR).
2. The 8259 evaluates the pending requests, and sets the INT output high if necessary.
3. The active CPU responds,causing a low on the $\overline{INTA}$ line.

Z-80A Operation:

4. The interrupt controller sets the highest priority level bits in the in-service register (ISR) and resets the appropriate bit in the IRR. A CALL instruction (0CDH) is placed on the data bus.
5. The CALL instruction generates two more $\overline{INTA}$ pulses from the Z-80A.
6. The two $\overline{INTA}$ pulses cause the 8259 to release the interrupt vector address; low order address byte first, followed by the high order address byte.
7. If the 8259 is set for automatic end of interrupt (AEOI), it automatically resets the corresponding bit in the ISR; otherwise, it waits for a specific EOI command to be issued at the end of the interrupt subroutine.

8088 Operation:

4. The interrupt controller sets the highest priority level interrupt bit in the in service register (ISR) and resets the appropriate bit in the IRR. The 8259 does not drive the bus at this time.
5. The 8088 CPU generates a second $\overline{INTA}$ pulse. During this pulse, the 8259 releases a one-byte vector onto the data bus to be read by the CPU.
6. If, at the completion of the interrupt cycle, the 8259 is set for automatic end of interrupt (AEOI), it automatically resets the corresponding bit in the ISR. If not, it waits for a specific EOI command to be issued at the end of the interrupt subroutine.

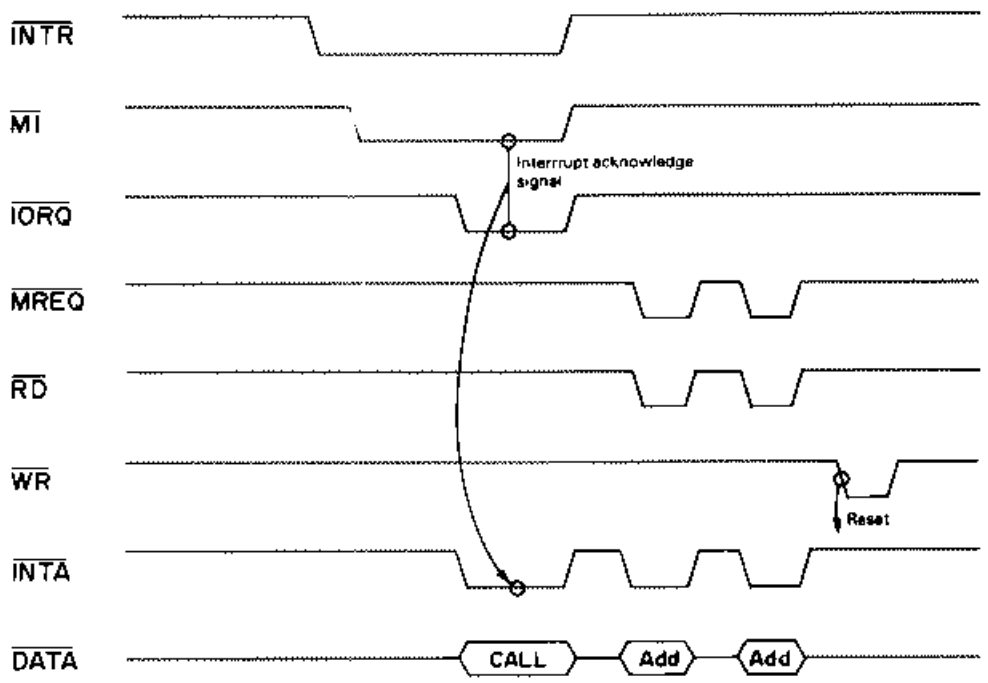


FIGURE 2-56. INTERRUPT RESPONSE SEQUENCE TIMING DIAGRAM (Z-80A)

2.3.4.4 8255 Programmable Peripheral Interface (Figures 2-57 and 2-58)

The 8255 programmable peripheral interface is used for four different purposes in the QX-16, as detailed in Table 2-30. The primary function is to provide the necessary hardware for the parallel printer interface port signals on CN3 (refer to Figure 2-58). Secondary operations include monitoring the DSR line of the serial interface (described in Section 2.3.4.2, in the discussion of the serial interface); controlling the step movement of the read/write heads; and reading the status of the extended memory bank switch. Table 2-31 details pin use in the 8255. Initialization is performed by the IPL program, as described in Chapter 6.

TABLE 2-30. 8255 PORT FUNCTIONS

PORT	BITS	FUNCTION
Port A	bits 0-7	Used to store the output byte for the printer.
Port B	bit 0	Used to sense the state of the Data Set Ready (DSR) line of the serial interface.
Port B	bit 1	Used to read the status of the extended memory bank switch. This value is a 0 if banks 0-3 are selected and 1 if banks 4-7 are in use.
Port B	bits 3-7	Used to read printer status.
Port C	bits 0, 4, and 5	Used to output control signals.
Port C	bits 3 and 6	Used to implement the interrupt circuit for printer handshake.
Port C	bit 1	Used to control operation of the stepper motor which moves the floppy disk read/write heads. This value is a 0 if the drives are operating in 48 TPI mode or 1 for 96 TPI mode. Refer to Chapter 6.

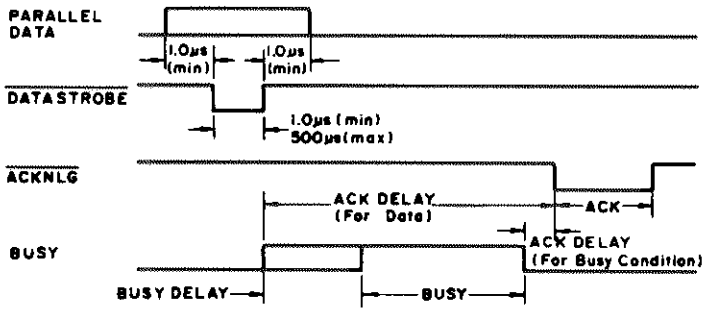


FIGURE 2-57. PARALLEL TIMING SEQUENCE

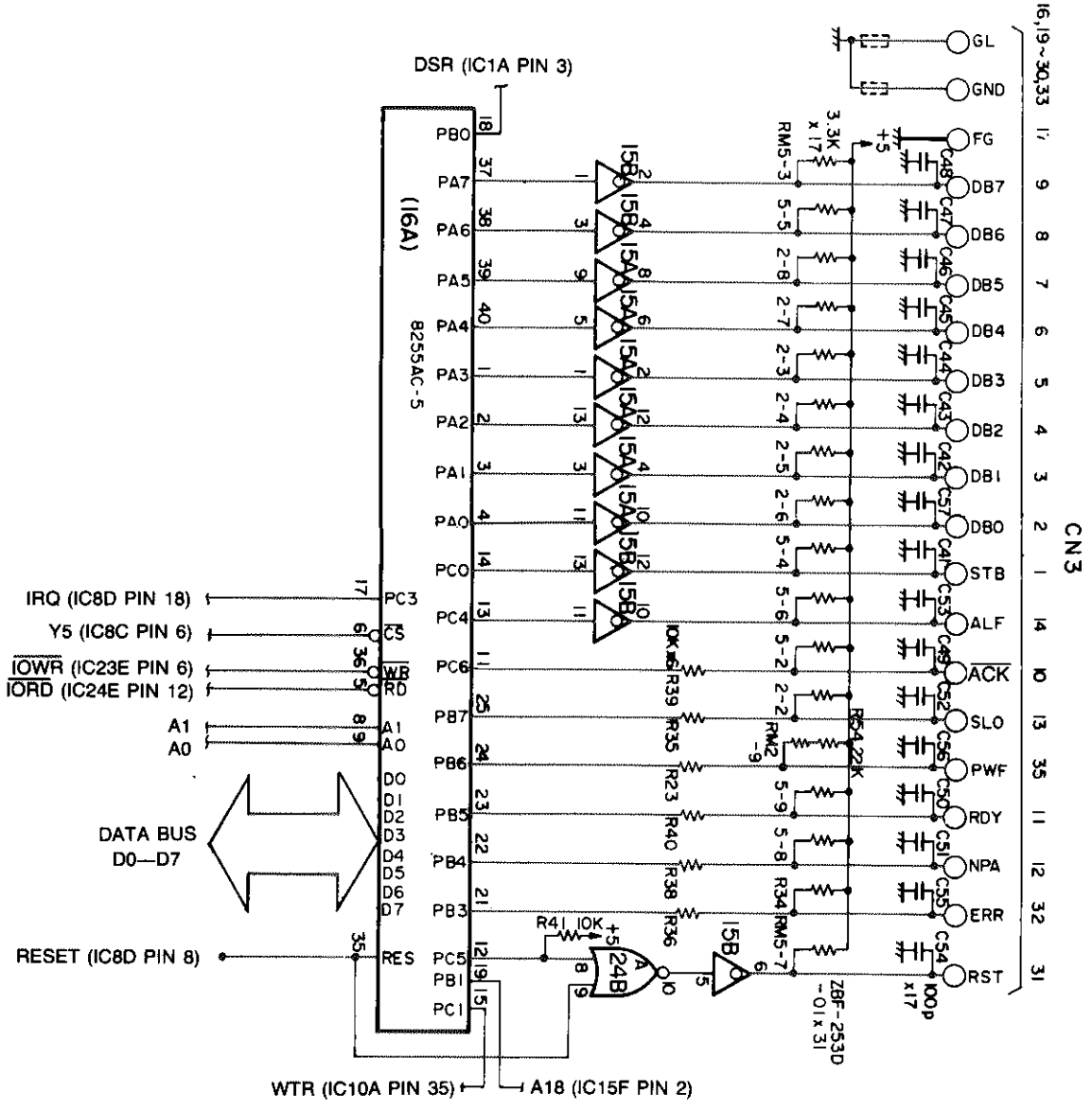


FIGURE 2-58. 8255 PROGRAMMABLE PERIPHERAL INTERFACE

TABLE 2-31. 8255 PIN DESCRIPTION

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
	D0—D7	IN/OUT	Connected to the CPU data bus and used for data transfer with the CPU.
6	CS	IN	Active low input to allow I/O operation. Connected to LS154 (IC 8C pin 6).
1-4 and 37-40	PA0 — PA7	OUT	Used as a data output port to the printer.
18	PB0	IN	This signal shows whether device is ready or not. (RS-232C signal).
19	PB1	IN	Bank group status input 0 = Banks 0-3 1 = Banks 4-7
21	PB3	IN	A low active input signal indicates printer error
22	PB4	IN	Accepts the paper-end signal from the printer.
23	PB5	IN	Low = Printer is ready to receive data. High = Printer is busy and cannot receive data.
24	PB6	IN	Low active signal detects printer power down
25	PB7	IN	Indicates that the printer is in the select state, and operation is effective.
14	PC0	OUT	A low active strobe pulse generated when data is sent to the printer
15	PC1	OUT	Controls floppy disk mode. 0 = 48 TPI 1 = 96 TPI
17	PC3	OUT	An interrupt input to the 8259A interrupt controller (8D).
13	PC4	OUT	By setting this signal low, the printer automatically line feeds after printing the input data.
12	PC5	OUT	An active low signal valid at reset by power on, reset switch, or an external I/O. At this time, all the internal registers (including the control register) are cleared.
8.9	A0.A1	IN	Connected to the CPU addresses A0 and A1 and used for mode setting of the 8255A in conjuction with IORD and IOWR signals.
5	RD	IN	Connected IORD line. Used to read data from inputs.
36	WR	IN	Connected IOWR line. Used to write data and configure the 8255.

2.3.4.5 Floppy Disk Controller — μPD765A, GAFDDC, and SED9421COB (Figures 2-59 through 2-66)

Three LSI integrated circuits are used to interface the CPU to the disk drive: the 765 floppy disk controller (FDC), the GAFDDC custom LSI floppy disk interface, and the SED9421COB data separator (VFO). The FDC accepts commands from the CPU, reports the status of the command execution, and retrieves and stores information from the floppy disks. The GAFDDC interface chip includes the custom circuitry required to enable the FDC to control the SD-543 disk drives. The SED9421COB VFO separates the data and clock pulses read from the floppy disk, and provides critical timing signals to the FDC and GAFDDC.

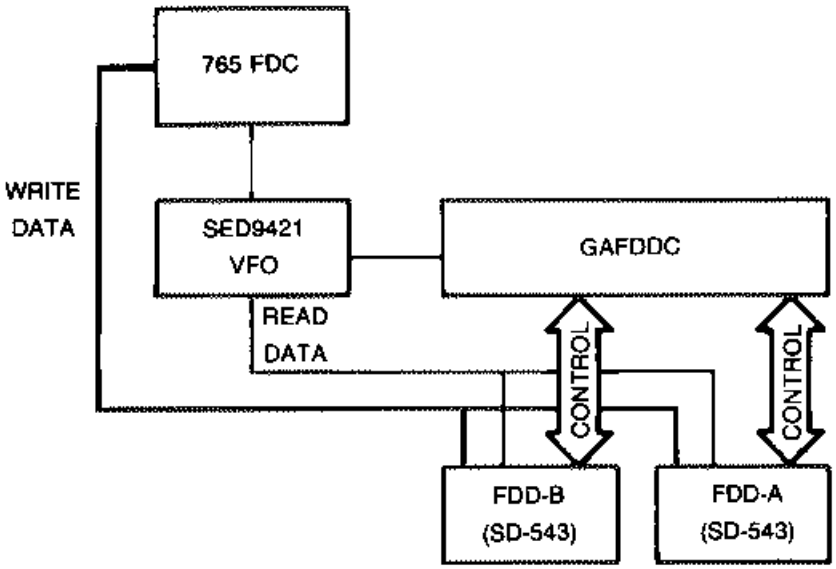


FIGURE 2-59. FLOPPY DISK CONTROLLER BLOCK DIAGRAM

CPU to 765 FDC Interface

The basic configuration of the 765 for the double sided, double density operation of the QX-16 is provided in Figure 2-60. The 765 interprets all commands issued by the active CPU and initiates the approriate control signals; some are used as inputs to the GAFDDC and others control DMA transfer (Table 2-32).

Clock inputs to the 765 are supplied by the SED9421. The two clock signals are CLK, a 4 MHz square wave, and WCLK, an asymmetrical square wave of 500 KHz. The other inputs to the 765 from the VFO are the separated data (RD) and the window timing (WND) signals.

Standard I/O interfacing is used to convey the data to the system bus. When the host CPU issues a command to the 765, the port address causes the I/O decoder (8C pin 15) to go low, bringing the chip enable input, $\overline{CE}$, (13A pin 4) low and enabling the FDC. The command byte is loaded into the command register when the $\overline{WR}$ line is pulsed low. A low address bit A0 selects the command/status register; a high selects the data register.

In the DMA mode, the active CPU issues the command and the 765 then requests service by raising the DMA service request (DREQ) line (pin 14) to high, signaling the 8237 DMA controller (10F, pin 19). The DMA acknowledge (DACK) line is used to select the chip for each byte transferred, and the $\overline{RD}$/$\overline{WR}$ lines determine whether data will be read from or written to the device (Figure 2-61). This process continues until the programmed count is reached, at which point the 765 issues an interrupt to the host CPU and status information can be read.

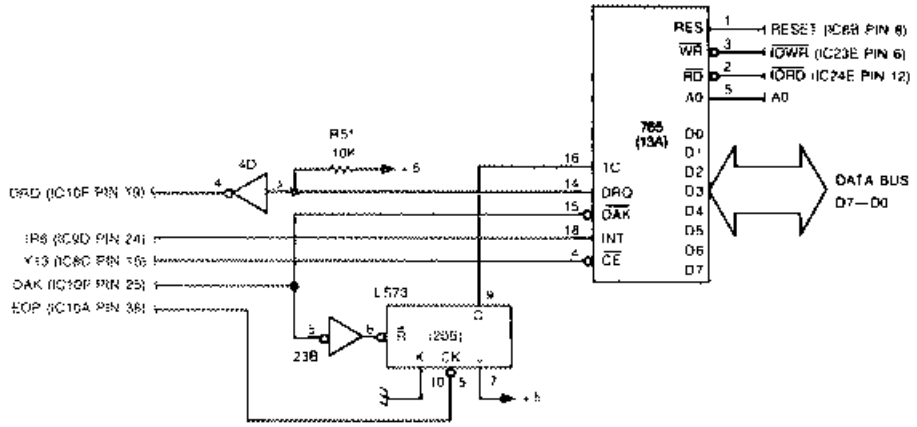


FIGURE 2-60. 765 FDC SYSTEM BUS INTERFACE CIRCUIT

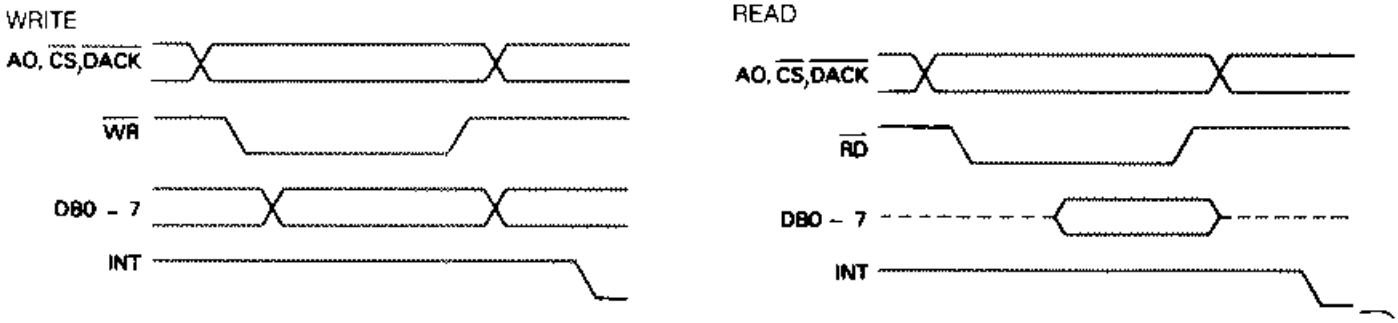


FIGURE 2-61. 765 FDC DMA TIMING DIAGRAM

TABLE 2-32. 765 PIN DESCRIPTION

PIN	SIGNAL	DIRECTION	DESCRIPTION
6-13	D0—D7	IN/OUT	Connected to the system data bus.
19	Ø	IN	4MHz single-phase clock is supplied from VFO circuit
1	RESET	IN	Reset Input
18	INT	OUT	Indicates that FDC is requesting service. This is output for every byte during non-DMA mode and during DMA mode on completion of command execution.
5	A0	IN	0 = Status/command register selected 1 = Data register selected
14	DRQ	OUT	Data transfer request signal between FDC and memory by DMA.
15	$\overline{DACK}$	IN	Indicates that DMA cycle may be entered.
39	RW/SEEK	OUT	Distinguishes between read/write (RW) and seek (SEEK) drive interface signal. 0 = RW and 1 = SEEK.
27	SIDE	OUT	Selects head 0 or 1 of a double-sided disk drive. 0 = head 0 and 1 = head 1.
38	LCT/DIR	OUT	When RW/SEEK designates RW, this works as LCT to indicate that the driver's read/write head selects a cylinder beyond #43. When RW/SEEK designates SEEK, this works as DIR to indicate seek direction (0 = outward 1 = inward).
37	FLTR/STEP	OUT	When RW/SEEK designates RW this works as FLTR to reset the fault state of the drive. When RW/SEEK designates SEEK this works as STEP which is the seek step signal. OUTPUT TO GAFDDC.
35	READY	IN	Indicates drive is ready.
34	WPRT/2 SIDE	IN	When RW/SEEK designates RW, this works as WPRT to indicate that the drive or disk is write-protected. When RW/SEEK designates SEEK, this works as 2 SIDE which indicates that a doubled sided disk drive is being used.
17	INDEX	IN	Indicates the physical start of tracks on the disk.
33	FLT/TRK0	IN	When RW/SEEK designates RW, this work as FLT to indicate that the drive is in fault state. When RW/SEEK designates SEEK, this works TK00 to indicate that the read/write head is positioned at cylinder 0
16	TC	IN	Indicates the end of read or write cycle by system.
30	WDATA	OUT	Clock and data bits to be written through the drive.
25	WE	OUT	Enables the drive to write data. OUTPUT TO GAFDDC
21	WCLK	IN	Write clock supplied to the drive from VFO circuit. 500KHz is used in FM mode and 1MHz in MFM mode.
23	RDATA	IN	READ DATA from VFO.
22	WINDOW	IN	Generated in VFO and used to sample RDATA. FDC synchonizes the data bits of RDATA with WINDOW in phase.
3	$\overline{WR}$	IN	Active low input used to write commands and parameters to 765.
2	$\overline{RD}$	IN	Active low input used to READ status and data from 765.
4	$\overline{CS}$	IN	Active low input used to select the 765 for access by active CPU.

GAFDDC to 765 FDC Interface

The SD-543 quad-density drives use the custom GAFDDC IC, easily identified at 10A on the APX-ISYM board as an 80-pin flat-pack, to convert standard FDD control signals from the 765 into control signals usable by the drive. Table 2-33 provides a full description of GAFDDC inputs; the major timing signals for the GAFDDC are supplied from the following sources.

1. CLK input (pin 40), used as a general purpose timing signal, is 1 MHz square wave from the VFO circuit.
2. OSCK (pin 46), used for spindle motor timing, is SQW output from 146818 RTC.
3. MS0 and MS1 (pins 56 and 57) are motor start pulses from the motor timing circuit.
4. RES (pin 53) is the system reset pulse.
5. WTR (pin 35), used to select 40 or 80 track operation, is supplied by 8255 port C bit 1.

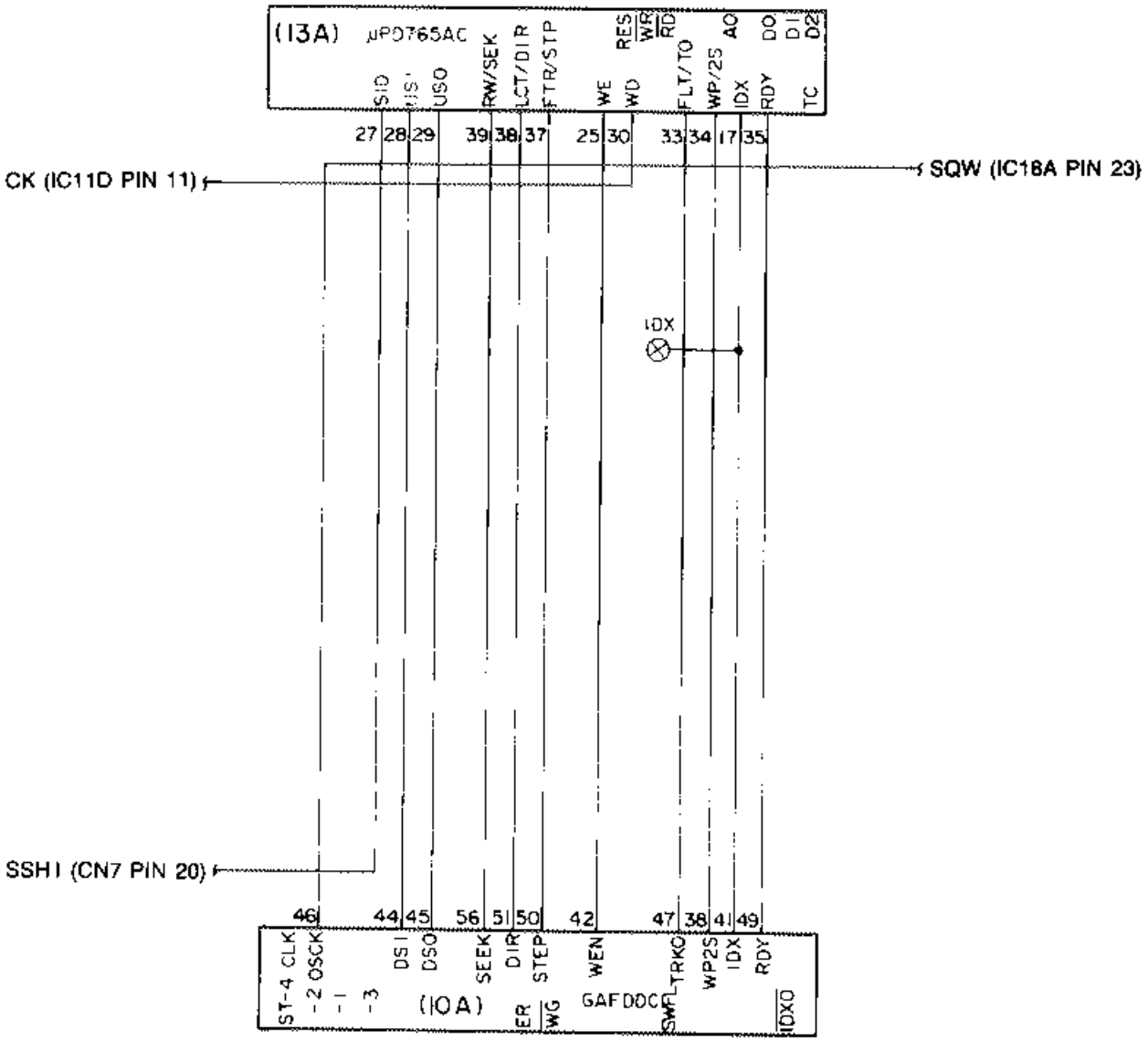


FIGURE 2-62. GAFDDC TO 765 FDC CIRCUIT

TABLE 2-33. GAFDDC PIN DESCRIPTION

PIN	SIGNAL	DIRECTION	DESCRIPTION
3-10	AD0-7	OUT	Tri-state bus output; not used in QX-16.
13-20	SW0-7	IN	Switch inputs; not used in QX-16.
11	TEST	IN	Test input; tied to +5V.
36	TER	IN	Test input; tied to +5V.
37	TMS	IN	Test input; tied to ground.
26	G	IN	Tri-states AD0-7, tied to +5V.
53	RES	IN	Active high reset input.
46	OSCK	IN	Clock for motor-on timing: RTC SQW signal.
40	CLK	IN	Clock input (1MHz) supplied by SED9421.
65,79	$\overline{IDX0}$,$\overline{IDX1}$	IN	Index signals from SD-543 drives.
41	INDX	OUT	Index signal output to 765 FDC.
49	RDY	OUT	Ready signal output to 765 FDC.
30,32,39	HDL0,HDL1, HDLD	—	Head load signals; not used on QX-16.
66,80	CIN0,CIN1	IN	For 3.5" drive; not used on QX-16.
57,58	MS0,MS1	IN	Motor on signal from motor control circuit.
29,67	$\overline{MST0}$,$\overline{MST1}$	OUT	Motor on signals to SD-543 drives.
54,55	FDS1,FDS2	IN	Sets drive type for output control signals. 1 = FDS1 0 = FDS2
2,68	TK00,TK01	IN	Track 0 detect inputs for SD-543 drives.
47	TRK0	OUT	Track 0 output signal to 765.
56	SEEK	IN	Specifies seek mode when high and read/write mode when low. Connected to 765
50	STEP	IN	Moves R/W head one track per pulse.
51	DIR	IN	Specifies direction of STEP operation. 0 = centrifugal (out) 1 = centripetal (in)
44,45	DS0,DS1	IN	Connected to 765; drive select signals. DS0 DS1 DRIVE 0 0 FDD-A 1 0 FDD-B
61,62	STP0,STP1	OUT	Active low hold signal for R/W stepper motor.
69-72	ST0 1-4	OUT	R/W stepper motor drive outputs for FDD-A.
74-77	ST1 1-4	OUT	R/W stepper motor drive output for FDD-B.
35	WTR	IN	Specifies 48 TPI or 96 TPI mode. Controlled by 8255 Port C bit 1. 0 = 48 TPI 1 = 96 TPI

TABLE 2-33. GAFDDC PIN DESCRIPTION (Continued)

PIN	SIGNAL	DIRECTION	DESCRIPTION
31	SWFL	OUT	Controls time constant of read amplifiers. 0 = tracks 0-42 1 = tracks 43-79
27,28	$\overline{SEL0}$,$\overline{SEL1}$	OUT	Enables FDD-A and turns on drive select LED.
24,25	$\overline{SEL2}$,$\overline{SEL3}$	OUT	Enables FDD-B and turns on drive select LED. Selects proper channel for VFO data input.

	SEL0	SEL1	SEL2	SEL3
FDD-A	0	1	1	0
FDD-B	1	0	0	1
NONE	1	0	1	0

22	$\overline{WG}$	OUT	Active low write gate signal.
42	WEN	IN	Active high write enable from 765.
21	ERS	OUT	Erase timing signal.
34	WPRS	IN	Selects polarity of write protect signals; tied to +5V.
64,78	WPR0-1	IN	Write protect signals from drives.
48	WPRT	OUT	Write protect signal for 179X series FDC, not used on QX-16.
38	WP2S	OUT	Write protect/two side signal to 765

GAFDDC to SD-543 Interface

The GAFDDC does not control the drives in the conventional daisy-chained configuration. It uses two sets of identical signals which are used to control the drives via connectors CN6 and CN7. These control the read/write head positioning, motor on timing and drive select functions. Inputs from each drive consist of index pulses, track 00 indication, and write project status.

There are three common control signals which control erase timing (ER), valid write condition ($\overline{WG}$) and side select (SIDE from the 765).

The data written to the drives is still supplied by the FDC through the circuit composed of IC 11D and 12D.

IC 11D acts as a divide-by-two circuit and provides complementary signals to the enable circuit composed of IC 12D. The two AND gates disable any signals when the $\overline{WG}$ signal (10A pin 22) is high, which indicates that a write protect condition is in effect.

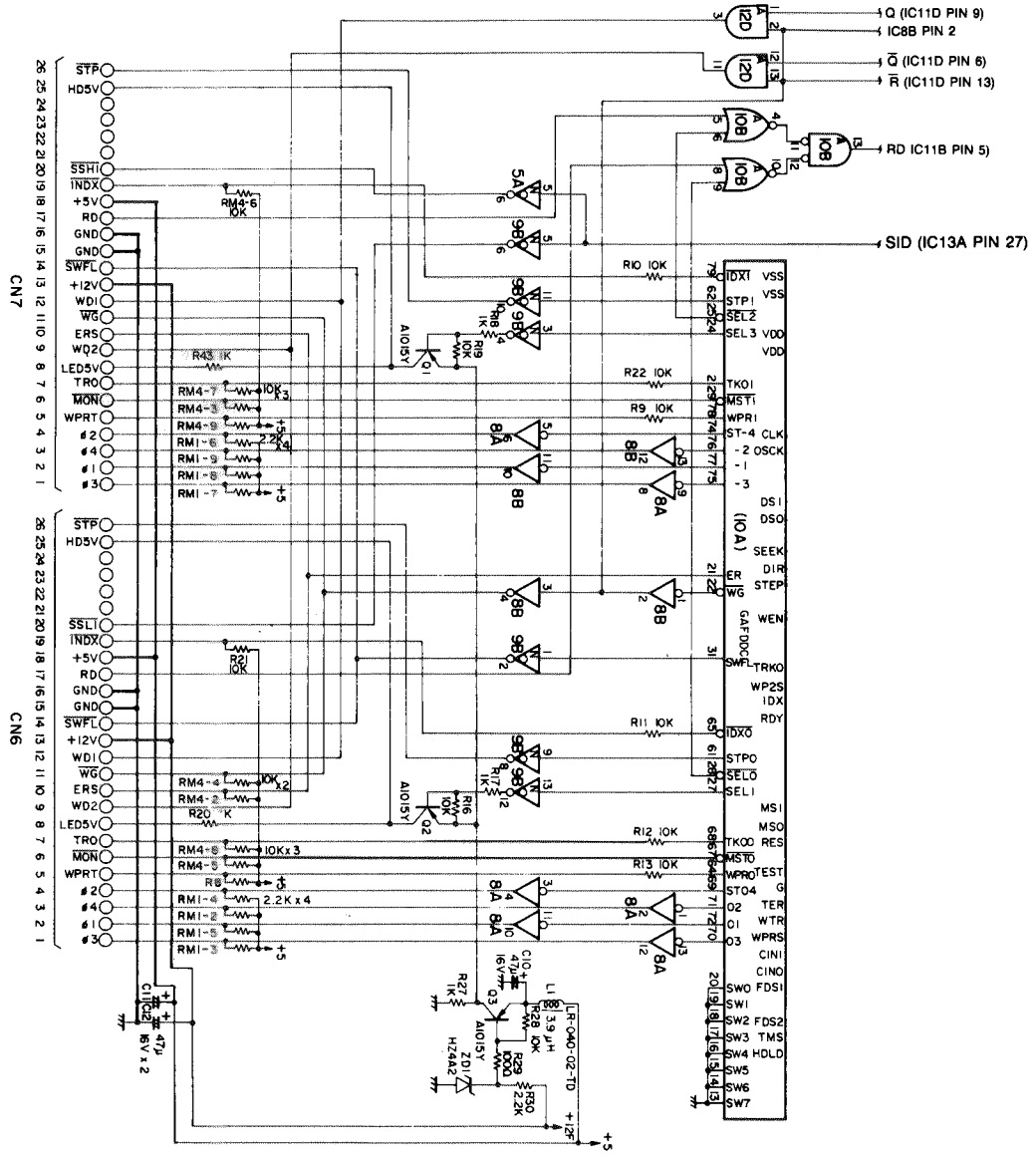


FIGURE 2-63. GAFDDC TO SD-543 INTERFACE CIRCUIT

VFO Data Separation

The SED9421COB variable frequency oscillator (VFO) at 11B (Figure 2-64) separates the data and clock pulses from the raw data read from the disk. Data received from the active drive via the select circuit at IC 10B is input to the VFO at pin 5, where the window (WND) and data (RD) signals are separated before being input to the 765 at pins 22 and 23, respectively. The VFO is also responsible for generating all timing signals for the FDC and GAFDDC chips. The clock signal used for all output timing signals (WCLK, 01 and 02) is generated by an internal oscillator circuit, and its frequency (16 MHz) is set by crystal CR2. (Refer to Table 2-34, and Chapter 6 for more details on the VFO integrated circuit.)

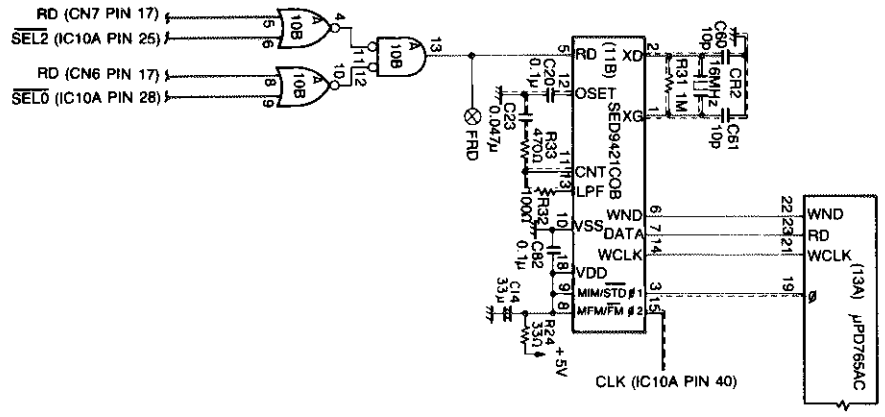


FIGURE 2-64. SED9421COB VFO CIRCUIT

TABLE 2-34. SED9421COB PIN DESCRIPTION

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1 2	XG XD	IN	Inputs for 16MHz quartz crystal.
3	01	OUT	Clock output to 765 FDC (1MHz square wave).
5	FD DATA	IN	Read data from disk drive
6	WINDOW	OUT	Data window signal supplied to 765 for separating data and clock pulses.
7	DATA	OUT	Data signal supplied to 765. This signal is combined clock and data pulses.
8	MFM/FM	IN	Selects recording method. QX-16 always uses double-density (MFM). This input is pulled high by R24.
9	MIN/STD	IN	Selects drive speed for 5 1/4" or 8" drives. This input is always high for SD-543 drives.
10	VSS	—	Ground terminal
11	CONTROL	IN	Control voltage input to VFO circuit.
12	OFFSET	IN	Offset input to set frequency of VFO.
14	WCLK	OUT	Write clock for 765. (1MHz square wave)
15	02	OUT	Clock output for 179X type FDC; not used on QX-16.
18	VDD	—	+5V supply terminal

FDD Motor Control Circuits

The FDD motor control signal is generated by the circuit composed of IC 21B, 23B, 24B,and 25B (Figure 2-65). When the CPU writes to the I/O address 30H, the output of IC 24B pin 4 goes high, which starts the two LS393 counters at 21B and 25B. The counters are clocked by the SQW output from the RTC and the count continues until the output on pin 8 of 21B goes high.

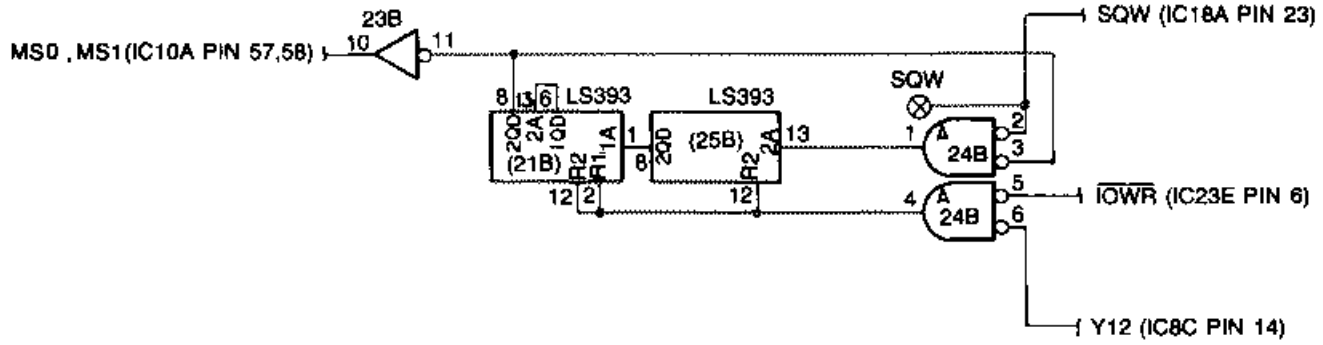


FIGURE 2-65. FDD MOTOR CONTROL CIRCUIT

FDC Status Port

Figure 2-66 shows the status port for the FDC,which can be read as port 30H. Three signals from the FDC circuit can be read from this port:

1. Bit 0 (pin 2 of 20A) allows you to read the INT output (13A pin 8) from the FDC. This signal is low to indicate a pending interrupt.
2. Bit 1 (pin 3 of 20A) is the motor on status. This signal is low when the motor is on.
3. Bit 3 (pin 5 of 20A) is the ready signal. This signal is high when the floppy disk drives are ready for operation.

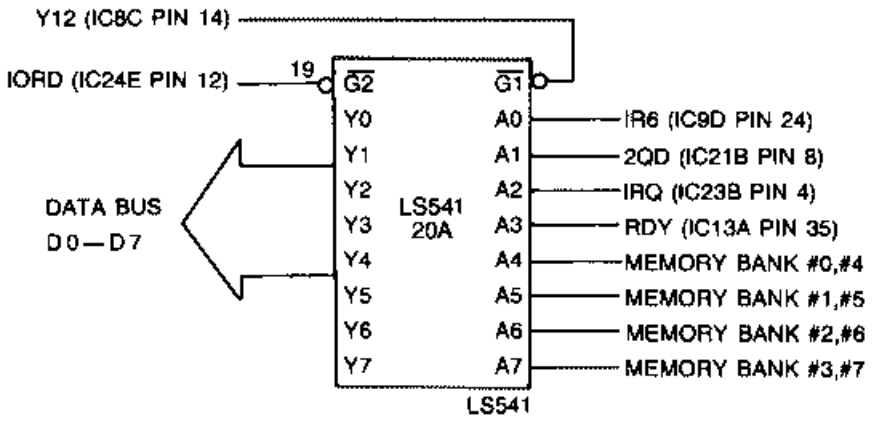


FIGURE 2-66. FDC STATUS PORT CIRCUIT

2.3.4.6 146818 Real Time Clock (Figure 2-67)

The real time clock (RTC) updates the time and calendar display, providing a means for programming real-time system interrupts and alarms, and includes a 50-byte RAM. The RTC is battery-backed by a NiCd cell connected to CN13, and continues to operate when the main power is turned off or disconnected. The RAM is typically used to store machine configuration data.

A 32.768 KHz crystal is used for the internal oscillator circuit. This value is divided to enable clock updates every second. Three types of interrupt can be generated:

1. The most commonly used interrupt is the update interrupt, which tells the host CPU that the update cycle is complete.
2. A periodic interrupt, ranging from once every 30 microseconds to once every 500 milliseconds, may be programmed into internal registers of the RTC.
3. An alarm interrupt, which generates an interrupt request when the programmed alarm values coincide with the current hour, minute, and second, may also be programmed.

The 50-byte RAM is accessed by assigning the address value to port 3DH and reading or writing the selected data on port 3CH. These values are retained until changed or until the battery discharges to less than 3 volts.

The SQW output from the 146818 chip is a programmable rate square wave generator. This signal is used as an input to the FDD motor control circuit.

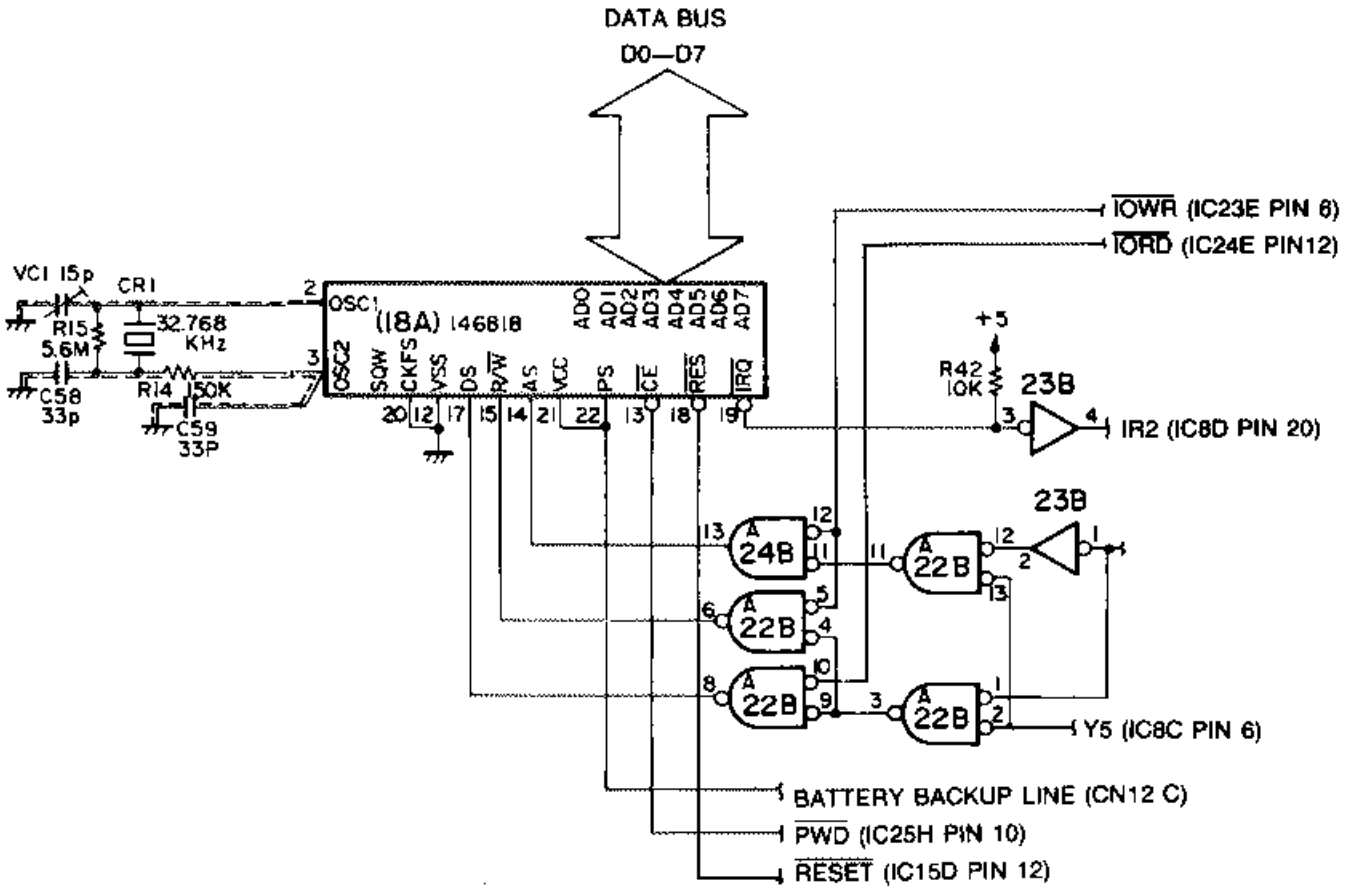


FIGURE 2-67. 146818 REAL TIME CLOCK CIRCUIT

TABLE 2-35. 146818 REAL TIME CLOCK PIN DESCRIPTION

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
2 3	OSC1 OSC2	IN	Input terminals for 32.768KHz crystal
20	CKFS	IN	Specifies divider for CKOUT signal. Connected to ground
23	SQW	OUT	Programmable square wave output used for floppy disk motor control circuit.
4-11	AD0—AD7	IN/OUT	Multiplexed address and data lines. Address is output to port 03DH and data can be read from or written to port 03CH.
14	AS	IN	Address strobe input. Used to latch contents of AD0—AD7 into address latch
17	DS	IN	Data strobe input. Active low input used to read from or write to AD0—AD7
15	R/W	IN	Selects whether data will be read or written when data strobe input is low.
13	CE	IN	Active low input used to select device for addess by active CPU
19	IRQ	OUT	Interrupt request output. Active low to signal an interrupt condition.
18	RES	IN	Active low reset input.
22	PS	IN	Power sense input. Connects to CMOS battery supply to detect low-voltage condition.

2.3.4.7 8237 Programmable DMA Controller (Figure 2-68)

Two 8237 programmable direct memory access (DMA) controllers (10F and 8F) are utilized to provide fast, efficient transfer of data from I/O devices to memory, or vice versa, without intervention by the host CPU. (The host CPU is held in an inactive state while the DMA transfer occurs.) Each controller normally provides four independent DMA channels (Table 2-36). The DMA controllers are linked in a master slave relationship, with 10F as master and 8F as slave, by connecting the hold request (HRQ) output, pin 10 of 8F, with the DMA service request (DRQ4) input, pin 16 of 10F, and the hold acknowledge (HAK) input, pin 7 of the slave, with DMA acknowledge (DAK4) output, pin 15 of the master (Table 2-37).

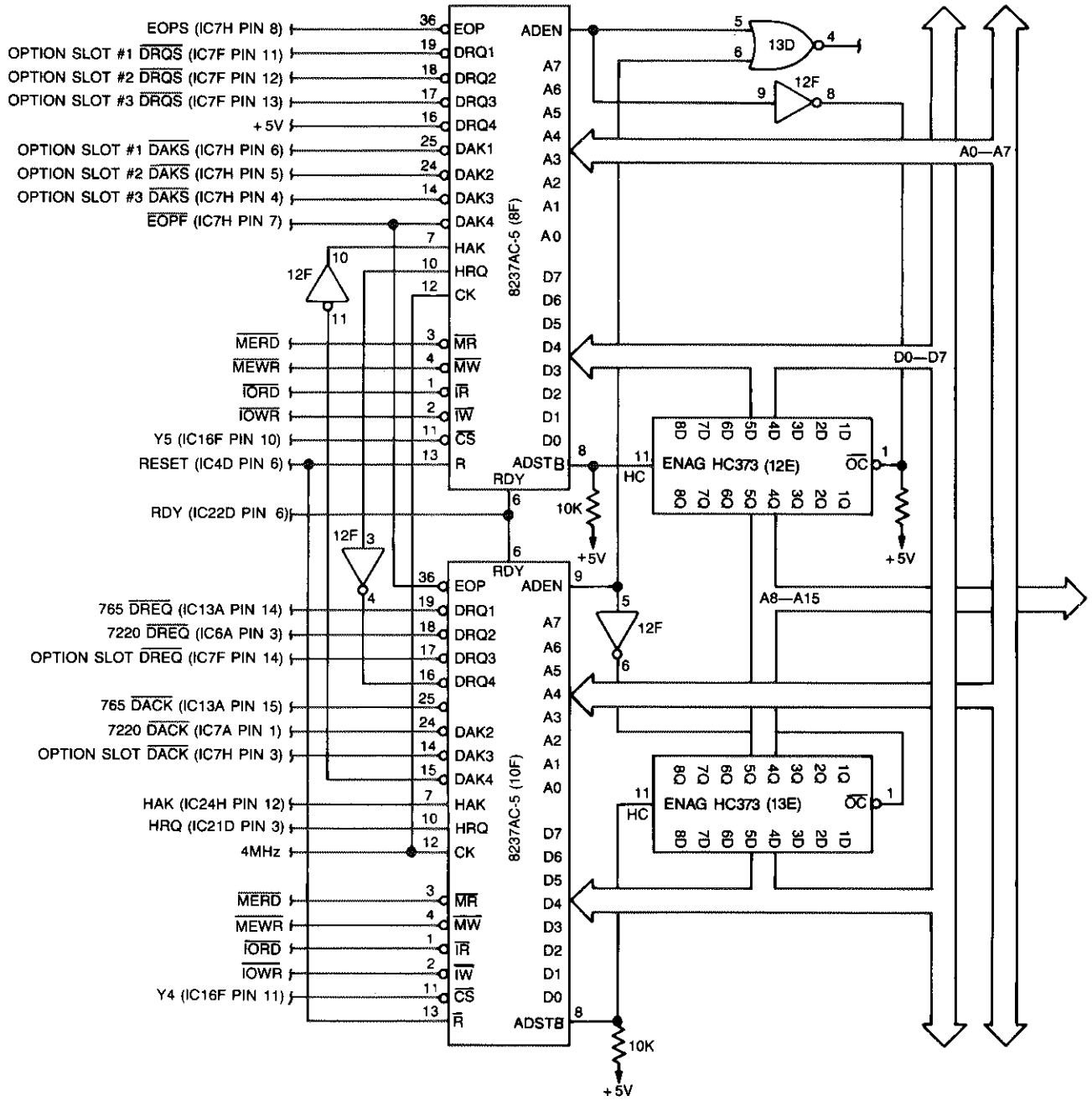


FIGURE 2-68. 8237 DMA CONTROLLERS

TABLE 2-36. DMA CHANNEL ASSIGNMENTS

CHANNEL		CONNECTION	PRIORITY
Master	1	765 Floppy Disk Controller	High
	2	APX-IGGS	
	3	Option slots (One of OP #1 through OP #3)	
	4	Slave DMA Controller	
Slave	1	Option slots (OP #1)	
	2	Option slots (OP #2)	
	3	Option slots (OP #3)	
	4	Unused	Low

TABLE 2-37. 8237 DMA CONTROLLER PIN DESCRIPTION

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
6	READY	IN	Used to expand memory read/write pulse output from 8237 to adapt to a low-speed memory or I/O device.
7	HLA	IN	Active high signal indicating the CPU has released control of the system bus.
16-19	$\overline{DREQ0}$ $\overline{DREQ3}$	IN	DMA request signals which peripheral devices use to receive DMA service through asynchronous channels. DREQ must be maintained until DMA becomes active.
24,25 14,15	$\overline{DACK0}$—$\overline{DACK3}$	OUT	Acknowledge signals to DMA request which inform specific peripheral devices of acceptance of DMA request.
9	ADEN	OUT	Enables the latch holding the most significant eight bits of address to output them to the address bus.
8	ADSTB	OUT	Strobes an external latch for the most significant byte of address.
10	HRQ	OUT	Hold request signal to the CPU bus request circuit.
36	EOP	IN/OUT	Information on completion of DMA service is available at this terminal. Signal EOP is generated internally or externally. This terminal is connected high through a pull-up resistor to prevent entry of spurious signals.
21-23 26-30	DB0—DB7	IN/OUT	During DMA cycle, the most significant eight bits of address are output to the data bus and placed in an external latch, strobed by ADSTB.
32,35	A0 A3	IN/OUT	During idle cycle: Addresses the control register loaded or read. During active cycle: Provides the least significant four bits of output address.
37-40	A4—A7	OUT	Provides the most significant four bits of address, permitted only during DMA service.
1	$\overline{IOR}$	IN	Active low signal used to read status information from 8237
2	$\overline{IOW}$	IN	Active low signal used to write configuration and address information to 8237.
3	$\overline{MR}$	OUT	Active low signal used to read data from memory into I/O device.
4	$\overline{MW}$	OUT	Active low signal used to write data that has been read from I/O device into memory.
11	$\overline{CS}$	IN	Active low signal used to select 8237 for access by CPU.

DMA I/O Selector

IC 16F, an LS138 1-of-8 decoder (Figure 2-69), is used to select the DMA controllers. The Y4 output (pin 11) is active low when the CPU outputs any address in the range of 40H to 4FH; the Y5 output (pin 10) is low when the CPU outputs an address in the range of 50H to 5FH. The outputs of the decoder are inactive (high) when either of the DMA controllers outputs a high address enable (ADEN) signal.

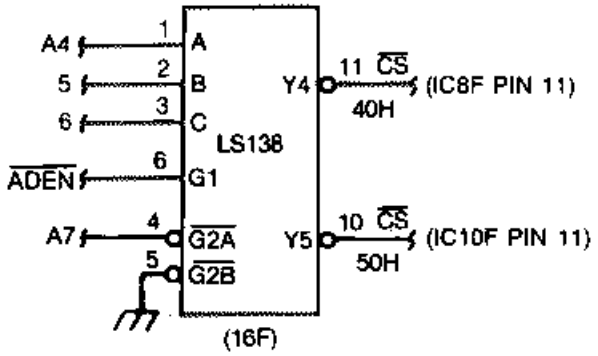


FIGURE 2-69. DMA I/O SELECTOR CIRCUIT

DMA READY Control Circuit

All of the DMA channels in the QX-16 are used for I/O-to-memory transfers. To provide adequate margin for read/write timing when providing DMA support to slower devices, the READY control circuit (Figure 2-70) temporarily makes the DMA controllers READY signals (pin 6) active low for a period of two clock cycles during each read or write operation by the DMA controllers.

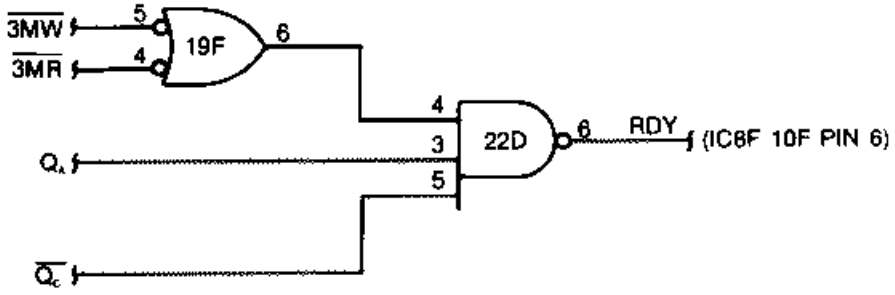


FIGURE 2-70. DMA READY CONTROL CIRCUIT

DMA Transfer Sequence

The operation sequences in I/O-to-memory and memory-to-I/O DMA transfers are very similar for Z-80A and 8088 operation. In Z-80A mode, DMA transfer is possible when a low $\overline{BRQ}$ bus request signal (pin 23 of 18C) enables Z-80A use of the system bus, and the Z-80A outputs a low $\overline{BAK}$ (pin 25) acknowledgement. In 8088 mode, DMA transfer is possible after the 8088 requests control of the system bus with a high HOLD signal (pin 31 of 16C), to which the 8088 responds with a high HLDA (pin 30). Thereafter, the transfer sequence is similar, as follows:

1. A DMA service request is supplied by an external I/O device by raising its corresponding 8237 DRQ input to a high level.
2. The 8237 determines the validity of the request and outputs an active high HRQ signal to the CPU control circuit, requesting control of the system bus from the active CPU. (Refer to Figure 2-71.)
3. The CPU switches the bus output and control lines to high impedance and outputs the acknowledge signal to the CPU control circuit.
4. When the HLA input is brough: high, the 8237 gains control of the bus and outputs a high ADEN signal to put the memory address on the bus. The 8237 also latches the high-order address byte to the external address latch (13E for the master, 12E for the slave) with the ADSTB signal.
5. The 8237 outputs the DAK signal to select the requesting I/O device.
6. The 8237 activates the $\overline{MR}$ line to read data from memory and load it into the I/O device, or the $\overline{MW}$ line to read data from the I/O device and load it into the memory address.
7. The end-of-process (EOP) signal is output at the completion of the DMA cycle.

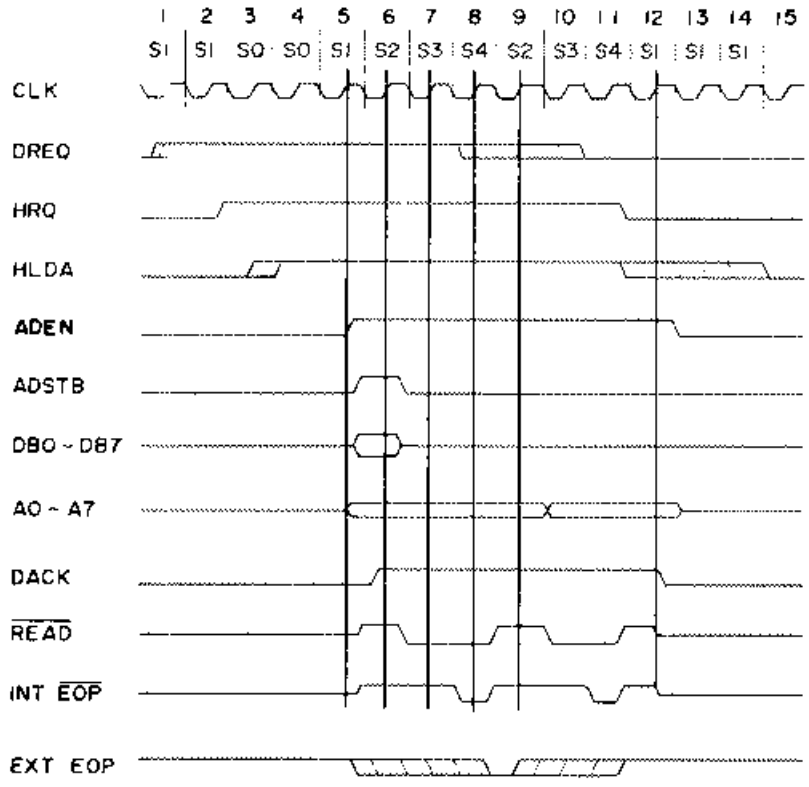


FIGURE 2-71. DMA TRANSFER SEQUENCE TIMING DIAGRAM

2.4 APX-IGGS CIRCUIT BOARD

The APX-IGGS circuit board provides all the necessary hardware for an 80-column by 25-line alphanumeric display or a 640 by 400 pixel graphics display. This board employs two LSI devices that provide the system bus interface, video timing signals, and control signals to manage 128K bytes of memory.

2.4.1 APX-IGGS Overview (Figure 2-72)

The RAM used on the APX-IGGS circuit board is isolated from the system bus of the QX-16 by the 7220 graphic display controller (GDC), separating the video RAM (VRAM) from the 512K system memory.

The 7220 GDC is responsible for generating most of the timing signals for the GAAPGD, based on its initialization values. (The GDC also performs other high-level functions under CPU control.) The GAAPGD LSI gate array performs most memory control functions and translates the VRAM data to video signals. The GAAPGD receives input signals from the 7220 and converts these to VRAM timing control signals for the RAM chips and the APX-IGGS internal bus control devices.

The VRAM circuitry consists of the memory devices and the bus control gates which direct the flow of information between the 7220 and the character generator. The memory is organized as 64K x 16 bits. The 16 bits of output data from the VRAM are latched and input to the character generator, which feeds the proper dot information into the GAAPGD for conversion to the video signal.

The character generator circuit is composed of two latches, which store the VRAM data; the character generator EPROM; and the output buffers, which select whether the RAM data are input to the GAAPGD directly, in graphics mode, or to the character generator, in alphanumeric mode.

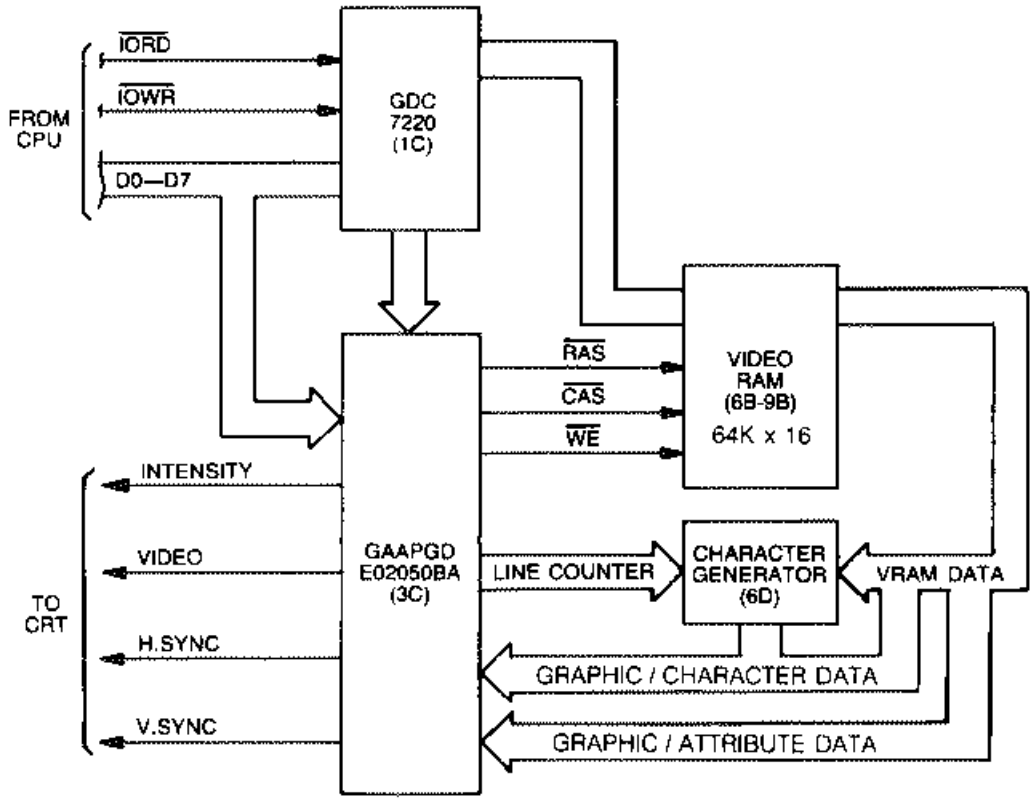


FIGURE 2-72. APX-IGGS BLOCK DIAGRAM

2.4.2 APX-IGGS System Interface (Figures 2-73 through 2-75)

The system interface circuitry decodes all I/O requests sent to the APX-IGGS circuit board, and selects the appropriate devices for access. This circuit also provides support for DMA mode transfers to the 7220 GDC.

ICs 2A and 3A provide gating for the I/O read and write signals ($\overline{IORD}$ and $\overline{IOWR}$), which are applied to pins 9 and 10, respectively, on the 7220 GDC. The gated read signal on pin 6 of 2A is also used to switch the direction of the LS245 (1B) bus transceiver. The output of IC 2A pin 6 provides the gating signal; this output is high whenever a read or write to port 038H or 039H is issued by the active CPU, or a DMA transfer acknowledge occurs.

ICs 2A, 3A, and 4A are used to implement the I/O address decoder for the APX-IGGS board, which is mapped to the addresses 02AH, 038H, 039H and 03AH. Port 02AH is used to decode the type of display board installed in the system. When port 02AH is accessed by a read or write command, the 2Y0 output on pin 9 of 4A pulls bit 0 on the data bus to ground, signifying that an APX-IGGS circuit board is installed.

The 1Y0 and 1Y1 open-collector outputs of 4A on pins 6 and 7 are tied together and used to enable the $\overline{IORD}$ and $\overline{IOWR}$ signals when the active CPU accesses port 038H or 039H. The 1Y2 output on pin 5 is active low when port 03AH is accessed, and is used to write bit 7 and the lower four bits of the data bus into the GAAPGD gate array.

ICs 2A, 6A, and 7A are used to implement DMA transfer handshaking logic. The DMA acknowledge input ($\overline{DACK2}$) is normally high and applied to pin 1 of IC 6A. This enables the $\overline{DREQ2}$ output on pin 3 to go low whenever the 7220 requests DMA service. When the request is acknowledged, pin 1 goes low and the output on pin 3 returns to high.

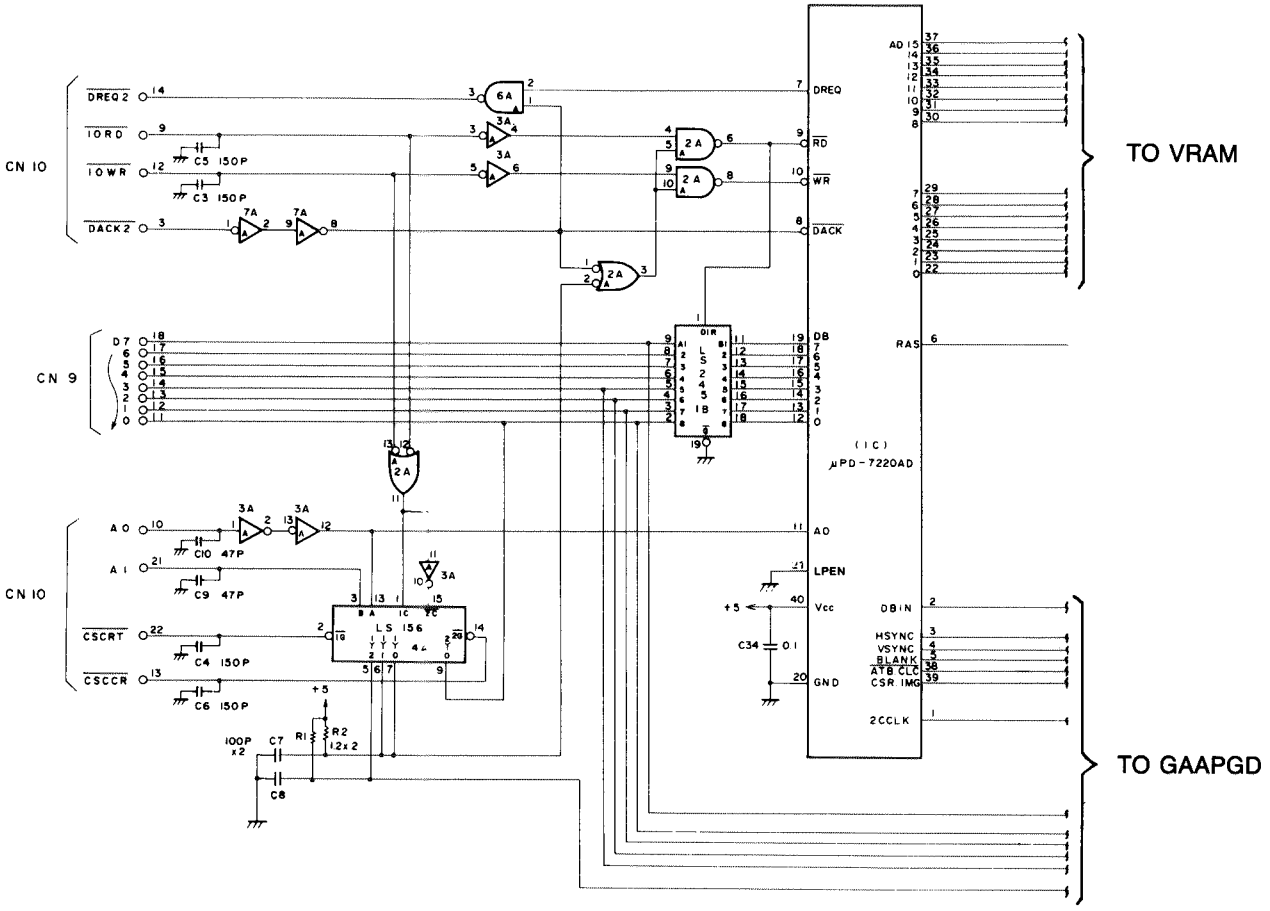


FIGURE 2-73. APX-IGGS SYSTEM INTERFACE CIRCUIT

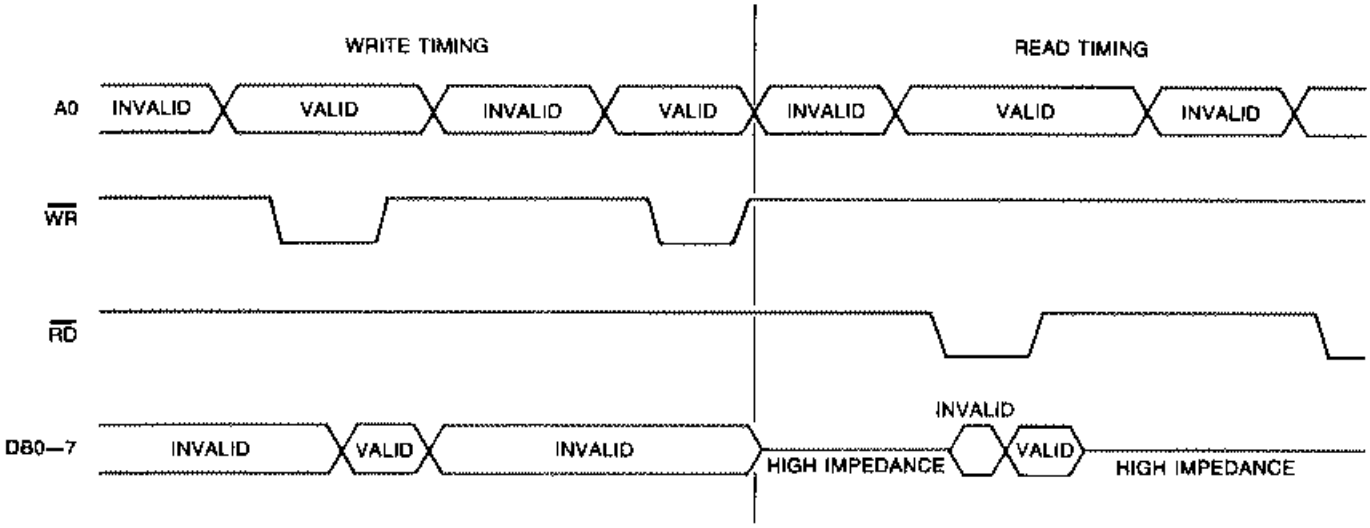


FIGURE 2-74. SYSTEM I/O READ/WRITE TIMING

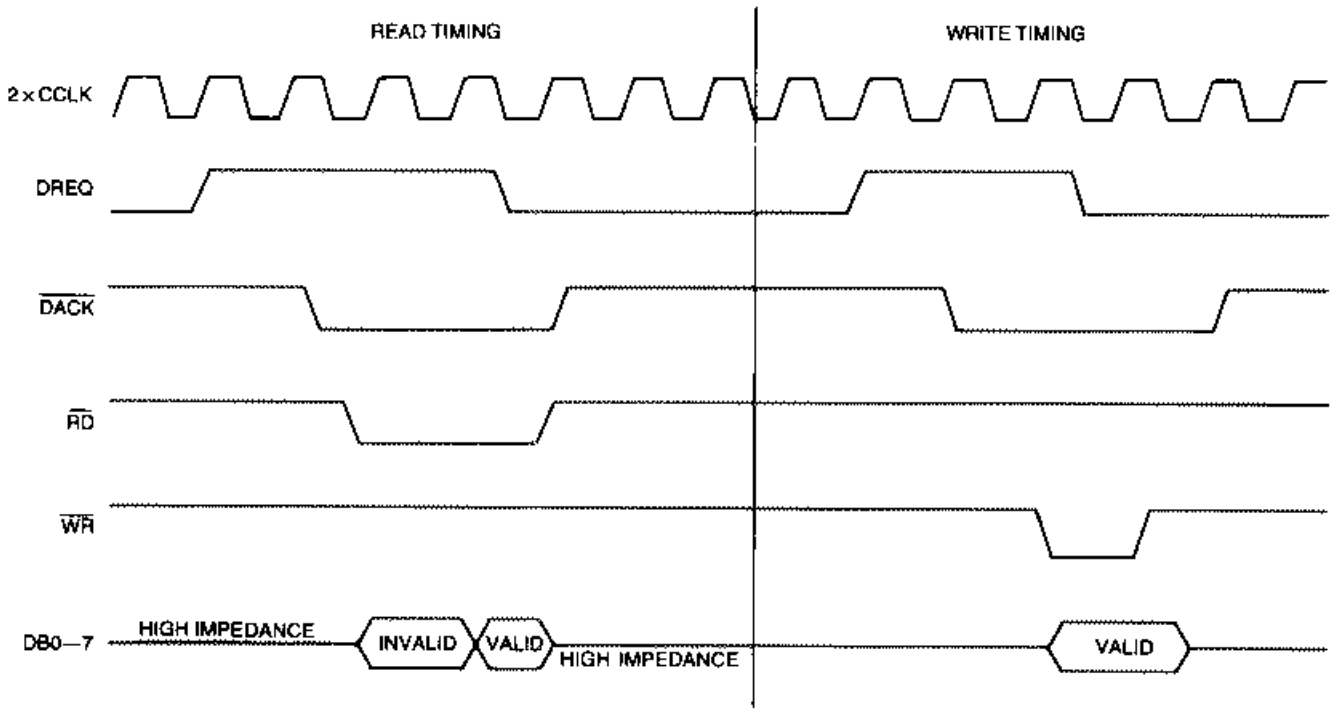


FIGURE 2-75. SYSTEM DMA READ/WRITE TIMING

2.4.3 7220 Graphic Display Controller (Figures 2-76 through 2-79)

The 7220 GDC is an advanced, LSI peripheral chip, which generates a high-resolution raster display and manages the display memory. The GDC is also responsible for carrying out high-level commands issued by the active CPU on the APX-ISYM board for graphics and display functions such as zoom, scrolling, and figure drawing.

The 2CCLK input on pin 1 of the GDC is a 4 MHz signal output from pin 9 of the GAAPGD. The signal originates at oscillator CR1 (16 MHz).

In the QX-16, the 7220 is an I/O device mapped to two different addresses. The $\overline{RD}$ and $\overline{WR}$ signals are brought low by the system interface whenever the active CPU accesses port 038H or 039H. The 7220 does not have a chip select input; access to the internal registers is determined by the status of address bit A0 when RD and WR lines are made active low. (Refer to Table 2-38 for internal register selection.)

Lines AD0-15 on the 7220 are multiplexed address and data lines used for display generation and VRAM updating. The $\overline{RAS}$ output on pin 6 of the 7220 is used to latch the display address into the external address latches and to generate proper timing of the memory signals by the GAAPGD. When the DBIN output on pin 2 of the GDC is low, the GAAPGD and the bus transceivers are signaled that the 7220 is requesting data at the specified location for a display memory update cycle.

The timing signals for the raster display are output from the 7220 to the GAAPGD for output to the CRT. VSYNC is the vertical synchronization signal used to reset the scan of the CRT to the upper left corner. HSYNC is the horizontal synchronization signal used to reset the scan of the CRT to the left side to prepare for the next scan.

Display attribute control is performed by the GAAPGD, and the GDC outputs the ATB.CLC signal which supplies the timing for the blinking attribute.

Organization of the display memory for graphic, text, or mixed mode is controlled by the GAAPGD based on the BLANK and CSR IMG signals output by the GDC. Character mode is selected when CSR IMG is low during an active blanking cycle; graphic mode is selected when CSR IMG is high during blanking.

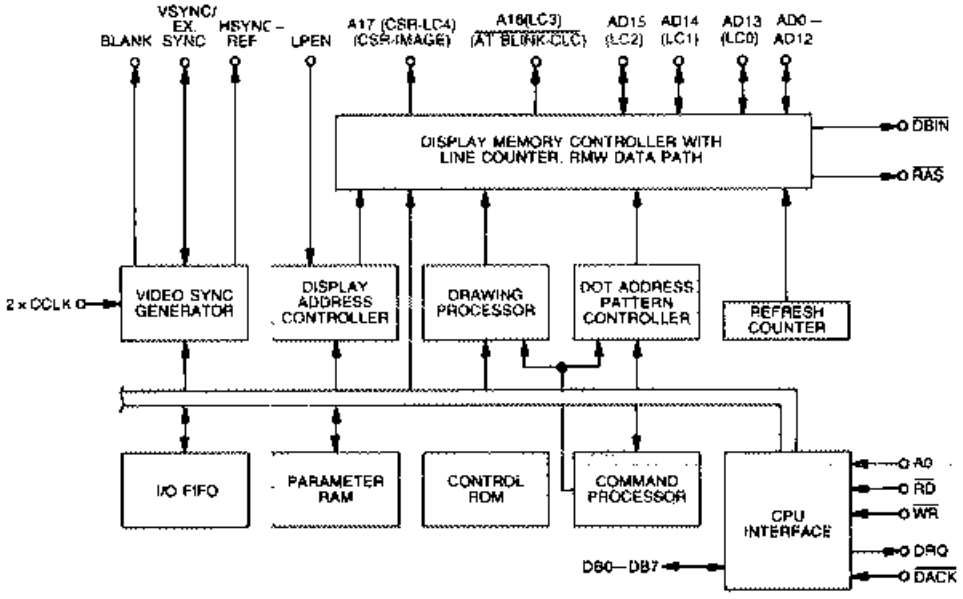


FIGURE 2-76. 7220 GDC BLOCK DIAGRAM

TABLE 2-38. 7220 REGISTER SELECTION

A0	RD	WR	MODE
0	0	1	Reads status flag
1	0	1	Reads data (from GDC)
0	1	0	Writes parameter
1	1	0	Writes command

TABLE 2-39. 7220 PIN DESCRIPTION

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
22-34	AD0-AD12	IN/OUT	Bidirectional address bus lines
35-37	AD13 (LC0) AD14 (LC1) AD15 (LC2) AD16 (LC3)	IN/OUT	During graphic and character-graphic mixed mode: address bus lines. During character mode: line counter.
12-19	DB0-DB7	IN/OUT	Bidirectional data bus
6	RAS	OUT	Memory control signal output from GDC to VRAM, also used as the timing signal to latch address. CAS is generated from this.
38	$\overline{\text{AT BLINK-CLC}}$	OUT	During blanking time (BLANK signal output): Clears the line counter. During tracing time (video signal output): Outputs attribute blinking timing signals.
39	CSR-IMAGE	OUT	During blanking time (BLANK signal output): Outputs cursor mark. During tracing time (video signal output): Outputs character/graphic area switching timing signal.
11	A0	IN	Connected to an address line of the CPU and used to designate internal registers. A0 RD WR FUNCTION 0 0 1 Read status flag 1 0 1 Read data 0 1 0 Write parameter 1 1 0 Write command
8	$\overline{\text{DACK}}$	IN	Supplied from the DMA controller to enable the GDC to distinguish between read and write performed by DMA.
7	DREQ	OUT	DMA request
2	DBIN	OUT	Memory control signal output from the GDC to VRAM (timing signal used to put VRAM output to the data bus).
4	V.SYNC	OUT	Vertical sync signal
3	H.SYNC	OUT	Horizontal sync signal
5	BLANK	OUT	Blanking signal output during horizontal retrace time, vertical retrace time, time between execution of SYNC and START commands and draw execution time
1	2XCCLK	IN	Supplied from an external dot clock generator. The clock frequency is determined by the relationship between the horizontal resolution in dots and the horizontal scanning time (4MHz).
9	$\overline{\text{RD}}$	IN	Used in combination with A0 to read status and data from 7220.
10	$\overline{\text{WR}}$	IN	Used in combination with A0 to write commands and parameters to the 7220

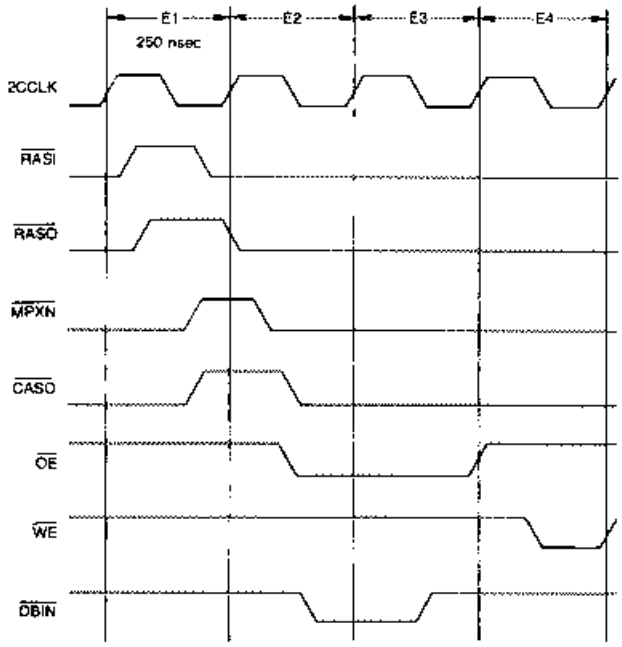


FIGURE 2-77. VRAM TIMING DIAGRAM

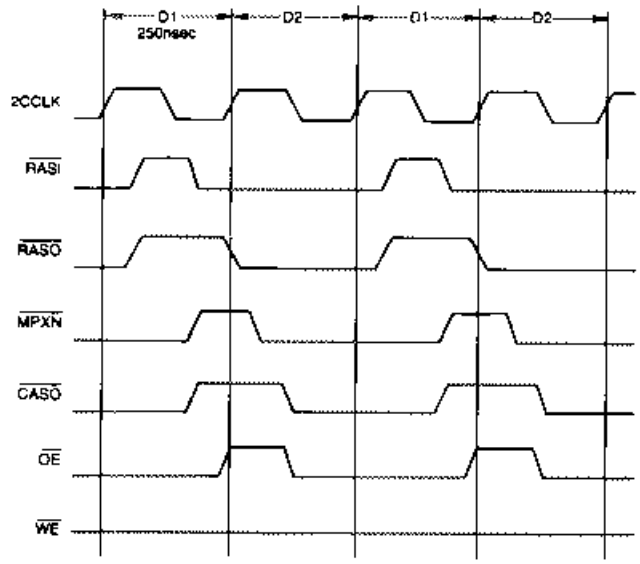


FIGURE 2-78. DISPLAY MODE TIMING DIAGRAM

2.4.4 GAAPGD LSI Gate Array (Figure 2-79)

The GAAPGD LSI gate array receives input signals from the 7220 and the active CPU and converts these to VRAM timing control signals for the RAM and APX-IGGS bus control devices. Control of the VRAM on the APX-IGGS board is dependent upon the hardware zoom register, accessed as port 03AH. When the zoom register is accessed, the lower four bits (ZOM 0-3) and bit 7 (STOP) of the data bus are written into the GAAPGD gate array. Bits 0-3 are used for controlling the row and column counters, and bit 7 is used to disable the video output signals from the GAAPGD.

The $\overline{\text{RASI}}$ (pin 2) and $\overline{\text{DBIN}}$ (pin 3) inputs are used to generate the memory timing signal outputs from the GAAPGD. MPXN (pin 47) is used as the enable signal for the column address latch (3B). $\overline{\text{MPXP}}$ is the enable signal for the row address latch (2B). These signals are used in conjunction with the $\overline{\text{RASO}}$ and $\overline{\text{CASO}}$ signals to strobe in the row and column addresses for the VRAM.

Write enable ($\overline{\text{WE}}$) is used to write the 7220 bus data into the VRAMs. The output enable ($\overline{\text{OE}}$) signal is used to read the contents of the VRAMs onto the bus during display or update cycles. The DLAT signal (pin 38) is used to latch the data from the VRAMs into the VRAM data latches (ICs 8C and 9C).

The LGTI, RVS, SCRT and BLINK inputs (pins 39-42) are the attribute inputs to the GAAPGD from the VRAM data latch (9C). Outputs LC0-3 (pins 33-35 and 37) are supplied from the line counter circuitry to the character generator (6D) when the display is in character mode.

The IMG output on pin 22 is active low during the character display mode to enable the outputs of the character generator; this output is high during graphic mode. The HB and LB signals (pins 22-23) are used to successively load the high and low bytes of the VRAM data latches into the GAAPGD during graphics mode operation. The video dot patterns loaded into the GAAPGD by the IMG, HB and LB signals are shifted out of the $\overline{\text{VIDE}}$ output on pin 21. If the display is in graphics mode, the highlight signal $\overline{\text{LGTO}}$ (pin 20) is low; $\overline{\text{LGTO}}$ is active high when the display is in character mode and the high intensity or bright attribute is set. $\overline{\text{VSOT}}$ and $\overline{\text{HSOT}}$ are the vertical and horizontal synchronization signals, respectively. The $\overline{\text{VIDE}}$, $\overline{\text{LGTO}}$, $\overline{\text{VSOT}}$ and $\overline{\text{HSOT}}$ signals are all disabled when the STOP (bit 7) input is high during a write to port 03AH.

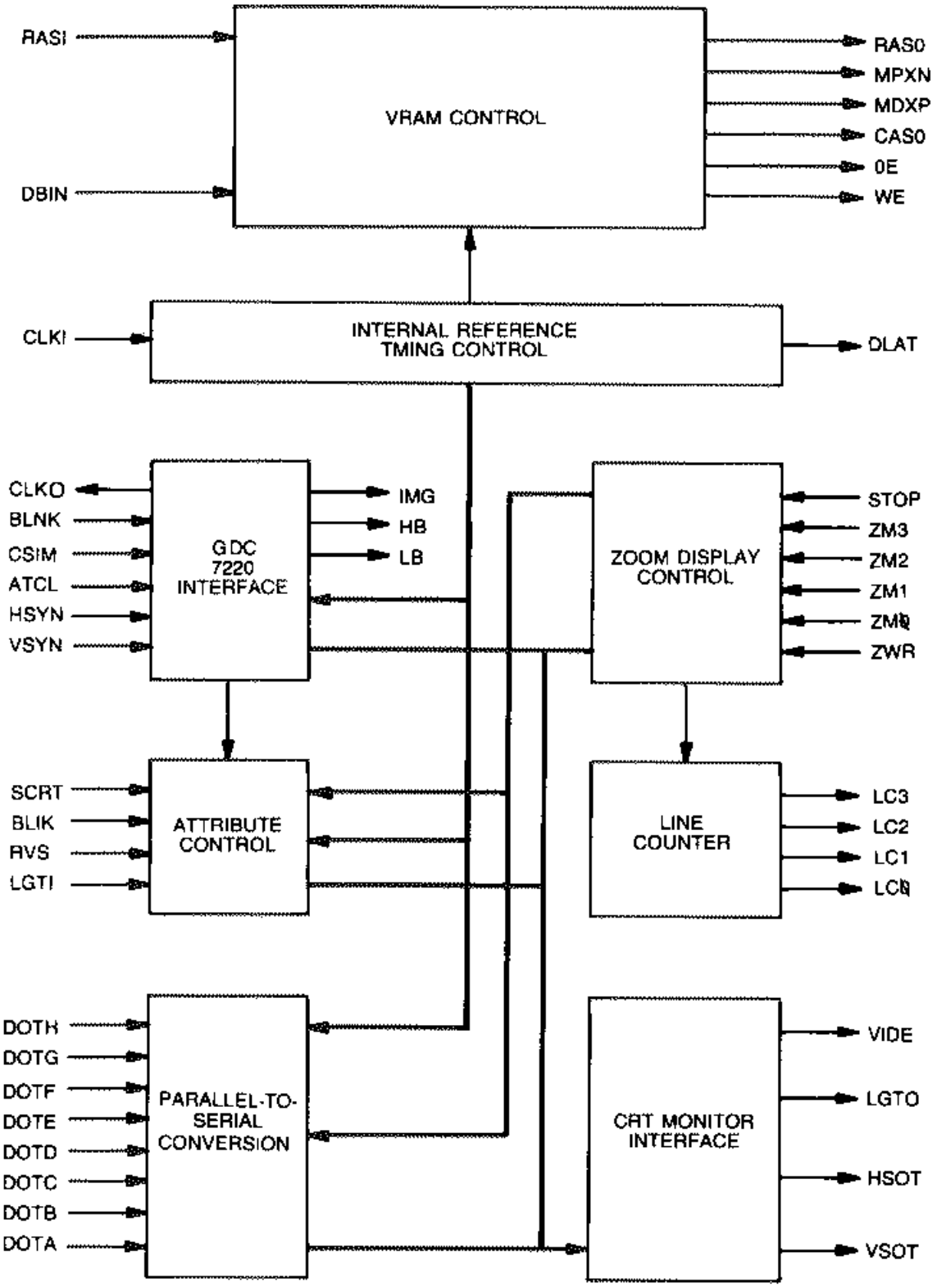


FIGURE 2-79. GAAPGD LSI BLOCK DIAGRAM

TABLE 2-40. GAAPGD PIN DESCRIPTION

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	CLKI	IN	Clock input from CR1.
2	RASI	IN	RAS memory timing signal from 7220
3	DBIN	IN	Used to read data from VRAM into 7220.
9	CLKO	OUT	CLKI input frequency is divided by four and applied to 7220 2xCCLK input.
48	RASO	OUT	RAS timing signal for VRAM devices. Based on RASI input.
47	MPXN	OUT	Active low signal to enable column address latch onto VRAM address bus.
46	MPXP	OUT	Active low signal to enable row address latch onto VRAM address bus.
45	CASO	OUT	CAS timing signal for VRAM devices.
44	WE	OUT	Write enable signal for VRAMs.
43	OE	OUT	Active low to read contents of VRAM.
38	DLAT	OUT	Latches VRAM data into 8C and 9C.
7	HSYN	IN	Horizontal sync signal from 7220
8	VSYN	IN	Vertical sync signal from 7220.
4	BLANK	IN	Blanking signal from 7220
5	ATCL	IN	Attribute clock signal from 7220.
6	CSIM	IN	Cursor/display mode signal from 7220
16-19	ZOM0-3	IN	Zoom port inputs from data bus.
15	STOP	IN	Stop signal; latched-in with zoom value.
14	ZWR	IN	Zoom port clock input; active low.
21	VIDE	OUT	Video dot signal to CRT.
20	LGTO	OUT	Intensity signal for CRT.
10	HSOT	OUT	Horizontal sync output to CRT.
11	VSOT	OUT	Vertical sync output to CRT.
33-35,37	LC0-3	OUT	Line counter outputs for 2764 character generator.
22	IMG	OUT	Enables character generator outputs in alphanumeric mode.
24	LB	OUT	Enables low byte of graphics word into GAAPGD.
25	HB	OUT	Enables high byte of graphics word into GAAPGD.
42	LGTI	IN	Highlight attribute signal.
41	RVS	IN	Reverse attribute signal.
40	SCRT	IN	Secret attribute signal.
39	BLINK	IN	Blinking attribute signal.

2.4.5 VRAM Memory Circuit (Figure 2-80)

The VRAM circuit is used to store the contents of the display image in graphics mode and the character code and attribute data in alphanumeric mode. The circuitry consists of the memory devices, address latches and the bus transceivers.

The row and column address latches hold the display memory address during VRAM memory cycles. The address is latched in by the RAS signal (1C pin 6) and the outputs of the latches are selectively enabled to coincide with the $\overline{RASO}$ and $\overline{CASO}$ signals from the GAAPGD.

The bus transceivers (ICs 4B and 5B) are used to control the direction of information between the GDC and the VRAMs. These devices are enabled by the $\overline{RASO}$ signal (IC 3C pin 48) while the memory address is being loaded into the RAMs by the $\overline{RAS}$ and $\overline{CAS}$ control lines. The direction is selected by the DBIN signal from the GDC, which is active low when it is reading from display memory.

The memory devices are very similar to those used on the APX-ISYM circuit board, with the exception of the output enable ($\overline{OE}$) pin. This active low signal is required for controlling the common data input/output lines, and is generated by the GAAPGD to enable the RAMs when the GDC needs information, or when data is to be output to the display.

Table 2-41 describes the function of the memory address bits for character and graphic modes.

TABLE 2-41. APX-IGGS VRAM CHIP FUNCTIONS

MODE	IC6B	IC7B	IC8B	IC9B
CHARACTER	ASCII VALUE		BRIGHT REVERSE	FLASHING SECRET
GRAPHIC	LSB ← GRAPHICS WORD → MSB			

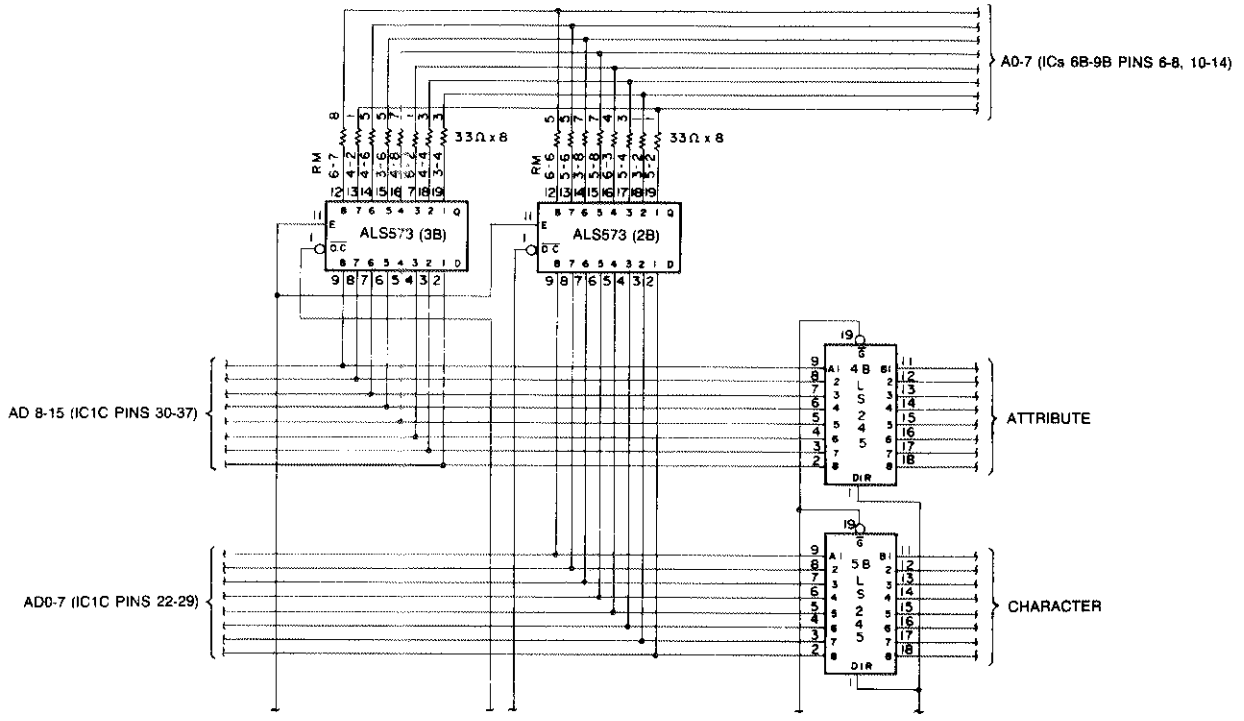


FIGURE 2-80. APX-IGGS VRAM CIRCUIT

2.4.6 Character Generator Circuit (Figure 2-81)

The character generator circuit provides the switching circuitry to output the VRAM information to the GAAPGD gate array as graphic or character data .

The two latches (IC 8C and 9C) store the VRAM data when the DLAT signal (3C pin 38) goes to high. The display mode programmed into the 7220 controls how the data stored in the latches is interpreted. The BLANK and CSR.IMG signals, output by the GDC control circuit, indicate which mode is in effect.

When character mode is selected, the content of latch 8C is interpreted as ASCII character code, and its value is supplied to the character generator address lines A4-A11. Four bits of latch 9C are used as the attribute data for the selected character. Line counter outputs from the GAAPGD are applied to the character generator address bits A0-A3. The GAAPGD chip brings the IMG output (pin 22) low to enable the character generator outputs to be read into the DOT A-H inputs (pins 25-32). Eighty consecutive addresses are repeated 16 times and the line counter value is incremented each time to form one alphanumeric display row. At the end of this process the display row counter is incremented and the process repeats itself for the next alphanumeric display line. This process occurs 24 or 25 times, depending on the display format (80 × 24 or 80 × 25).

When graphic mode is selected, the data in latch 8C is read into the GAAPGD when the LB output (pin 24) goes low. The data in latch 9C is read into the GAAPGD when the HB output (pin 23) goes low. This process is repeated for 40 consecutive addresses to create one scan line. At this point the display row counter is incremented and the process repeats for the next scan line. In graphic mode this process repeats itself 400 times for each display frame.

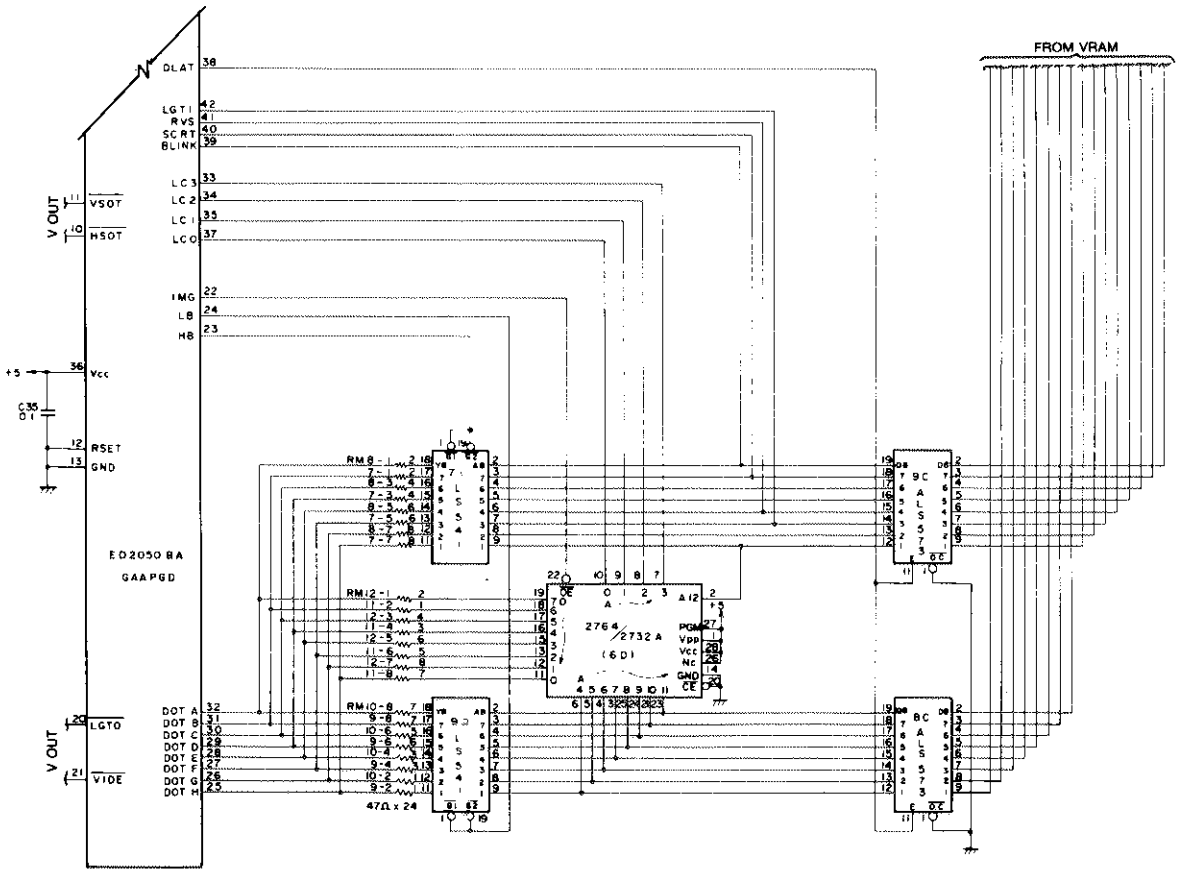


FIGURE 2-81. APX-IGGS CHARACTER GENERATOR CIRCUIT

2.4.7 APX-IGGS Output Circuit (Figure 2-82)

The APX-IGGS output circuit, composed of ICs 5A, 6A, 7A, and 8A, combines its outputs with those of the APX-ICRT board. The $\overline{VIDE}$, $\overline{LGTO}$, $\overline{VSOT}$, and $\overline{HSOT}$ outputs from the GAAPGD are all set high when the STOP input (bit 7) is high during a write to port 03AH. (Refer to Section 2.5.4.) This allows the APX-ICRT outputs, listed in Table 2-42, to drive the LS541 buffer. The APX-ICRT outputs are disabled when bit 7 is low during a write to port 03CFH. For a more detailed description of this port, refer to Section 2.5 and Chapter 6.

TABLE 2-42. APX-IGGS VIDEO INPUT SIGNALS*

CN1 PIN	SIGNAL NAME	FUNCTION
1	GND	Signal ground
2	$\overline{V.S.}$	Vertical sync
3	$\overline{H.S.}$	Horizontal sync
4	$\overline{B}$	Blue video signal
5	$\overline{G}$	Green video signal
6	$\overline{R}$	Red video signal
7	$\overline{I}$	Intensity signal
8	N/C	No connection

*All inputs to the APX-IGGS are from the APX-ICRT board.

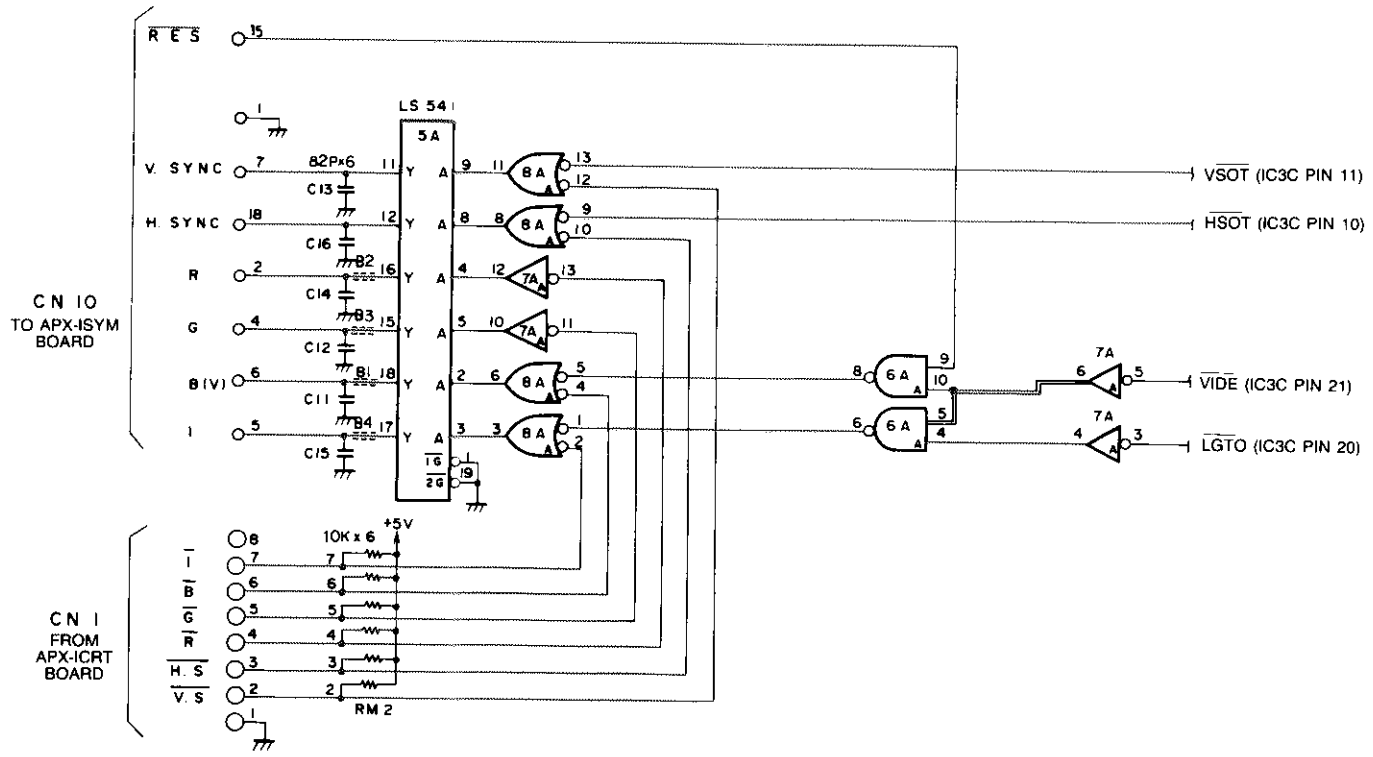


FIGURE 2-82. APX-IGGS VIDEO OUTPUT CIRCUIT

2.5 APX-ICRT CIRCUIT BOARD

The APX-ICRT circuit board provides all the necessary hardware to emulate the monochrome and color video display circuitry of the IBM PC. This board employs three LSI devices to provide system bus interfacing, video timing, and control signals to manage 32K bytes of video memory. (Refer to the APX-ICRT schematic, Figure 6-66.)

2.5.1 APX-ICRT Overview (Figure 2-83)

The APX-ICRT board uses the HD46505 CRT controller (6845 compatible), a 2764 8K character generator, four 16K x 4 bit 81416 VRAMs, and the GAIBVA and GAIBVD gate arrays, which fetch display data from the VRAM based on control signals generated by the 46505.

Figure 2-83 diagrams the connection of the VRAMs to the QX-16 system bus via the GAIBVA at 2D and the GAIBVD at 2F. The VRAMs are organized as 16K x 16 bits: the 16 bits of output data are input to the GAIBVD gate array for conversion to the video signal. VRAM memory is separate from the 512K system memory, and the devices used on the APX-ICRT board are different from those used on either the APX-ISYM or APX-IGGS boards.

The 46505 generates most of the timing signals for the GAIBVA and GAIBVD LSI gate arrays based on its initialization values. The GAIBVA and GAIBVD do most of the memory control and translate the VRAM data to video signals.

The character generator stores the character matrix patterns. This EPROM receives the character address from the GAIBVD and the row address from the 46505. The character patterns are input to the GAIBVD.

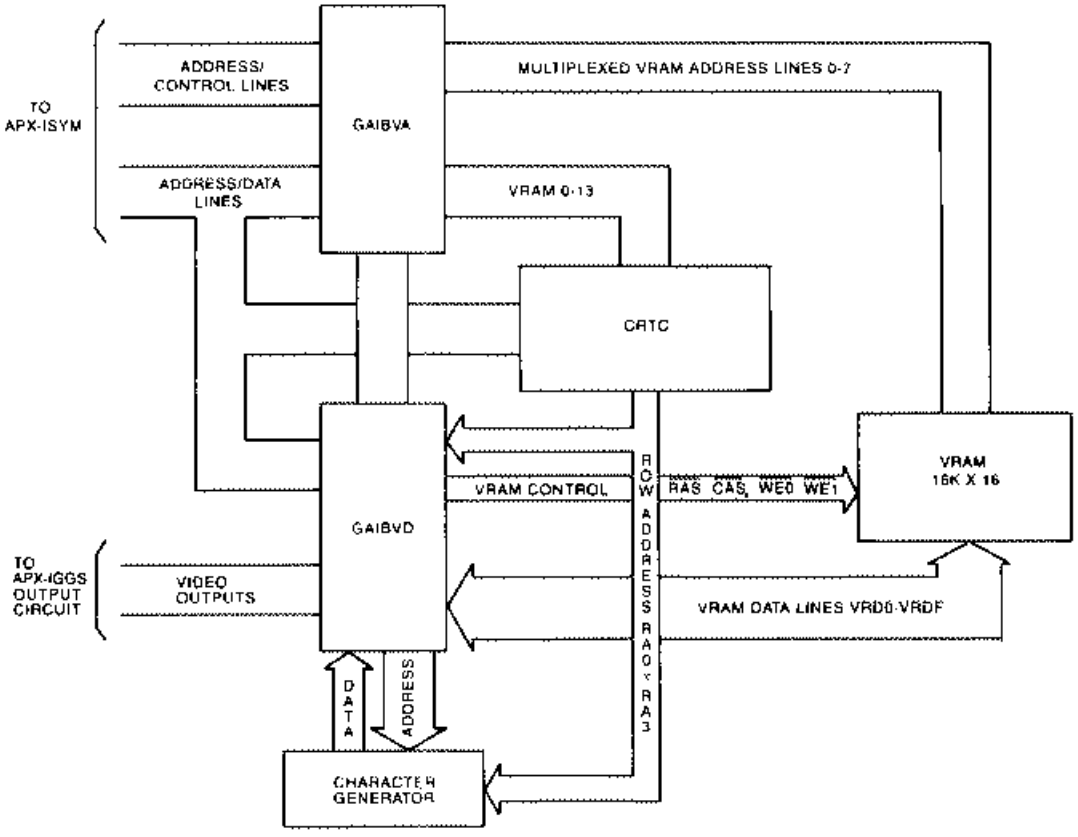


FIGURE 2-83. APX-ICRT BLOCK DIAGRAM

2.5.2 APX-ICRT System Interface

The system interface circuit (ICs 1E and 1F) buffers the incoming bus control signals and the multiplexed AD0-AD7 signals. The GAIBVA gate array buffers the remaining address and control lines. IC 1F is always enabled to buffer the incoming control and timing signals to the GAIBVA chip. IC 1E (ALS 245) is enabled by the GAIBVA and the bus direction is determined by the 8088 DT/R line, which is buffered by IC 1F. All I/O registers, except the internal registers of the 46505, are contained in the GAIBVA and GAIBVD LSIs.

2.5.3 46505 CRT Controller

The 46505 CRT controller (CRTC) generates display memory addresses, row addresses for the character generator, display timing, and cursor signals, enabling the APX-ICRT board to provide all the functions of the IBM monochrome and color graphic display hardware. In conjunction with the advanced gate array circuits, the CRTC is able to provide additional display modes (Table 2-43).

The 46505 uses a different clock rate depending upon which display mode has been programmed. When the display mode is 40 characters per line, the clock input of the CRTC is 1 MHz. This value is switched to 2MHz when 80 character mode is selected. The CLK input on pin 21 of the CRTC is output from pin 40 (CCLK) of the GAIBVD and originates at oscillator CR1.

The 46505 is used as an I/O device in the QX-16, and is mapped to two different sets of addresses, depending upon whether the monochrome or color board is being emulated: the CRTC is mapped to I/O addresses 03B4H-03B5H for monochrome board emulation and addresses 03D4H-03D5H for color board emulation. Mapping is controlled by the GAIBVA gate array.

The 46505 has eighteen internal registers, which are accessed by setting the register number in the index register at port 03B4H or 03D4H (depending on mode). The data value for the selected register is accessed through port 03B5H or 03D5H (Table 2-44).

TABLE 2-43. 46505 PIN DESCRIPTION

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	Vss		Ground
2	$\overline{RES}$	IN	Reset signal input
3	LPSTB	IN	Light pen strobe signal input. Not used in the QX-16.
4-17	MA0-MA13	OUT	VRAM memory address signals.
18	DISPTMG	OUT	Active high timing signal used to define active display area
19	CUDISP	OUT	Active high cursor timing signal.
20	Vcc		+5V supply connection.
21	CLK	IN	Timing clock supplied by GAIBVD. 1MHz. 40 column display 2MHz. 80 column display
22	$\overline{R/W}$	IN	Read/write signal from GAIBVA.
23	E	IN	Enable signal for read/write operations.
24	RS	IN	Register select signal supplied by GAIBVA.
25	$\overline{CS}$	IN	Active low chip select signal.
26 33	D0- 7	IN/OUT	Bidirectional data bus signals.
34-38	RA0 RA4	OUT	Row address signals for gate arrays and character generator to select correct scan row.
39	HSYNC	OUT	Horizontal sync output to GAIBVD.
40	VSYNC	OUT	Vertical sync output to GAIBVD.

TABLE 2-44. 46505 CRTC REGISTER SELECTION

CS	RS	ADDRESS REGISTER 4 3 2 1 0	REGISTER	REGISTER NAME	PROGRAM UNIT	READ	WRITE	DATA BIT 7	6	5	4	3	2	1	0
1	X	X X X X X			—	—	—								
0	0	X X X X X	AR	Address register	—	X	O								
0	1	0 0 0 0 0	R0	Horizontal total*	Character	X	O								
0	1	0 0 0 0 1	R1	Horizontal displayed	Character	X	O								
0	1	0 0 0 1 0	R2	Horizontal sync position*	Character	X	O								
0	1	0 0 0 1 1	R3	Sync width	Vertical-register, Horizontal-Character	X	O	wv3	wv2	wv1	wv0	wh3	wh2	wh1	wh0
0	1	0 0 1 0 0	R4	Vertical total*	Line	X	O								
0	1	0 0 1 0 1	R5	Vertical total adjust	Raster	X	O								
0	1	0 0 1 1 0	R6	Vertical displayed	Line	X	O								
0	1	0 0 1 1 1	R7	Vertical sync position*	Line	X	O								
0	1	0 1 0 0 0	R8	Interface and skew	—	X	O	C1	C0	D1	D0				
0	1	0 1 0 0 1	R9	Maximum raster address	Raster	X	O								
0	1	0 1 0 1 0	R10	Cursor start raster	Raster	X	O		B	P					
0	1	0 1 0 1 1	R11	Cursor end raster	Raster	X	O								
0	1	0 1 1 0 0	R12	Start address (H)	—	O	O								
0	1	0 1 1 0 1	R13	Start address (L)	—	O	O								
0	1	0 1 1 1 0	R14	Cursor (H)	—	O	O								
0	1	0 1 1 1 1	R15	Cursor (L)	—	O	O								
0	1	1 0 0 0 0	R16	Light pen (H) (not used)	—	O	X								
0	1	1 0 0 0 1	R17	Light pen (L) (not used)	—	O	X								

NOTE: 1. The registers marked *: (Written value) = (Specified value) − 1
2. Written value of R9 is mentioned below.
1) Non-interlace mode / Interlace mode } (Written value Nr) = (Specified value) − 1
2) Interlace sync and video mode
(Written value Nr) = (Specified value) − 2
3. C0 and C1 specify skew of CUDISP output signal.
D0 and D1 specify skew of DISPTMG output signal.
When S is "1", V specifies video mode. S specifies the interlace sync mode.
4. B specifies the cursor blinking. P specifies the cursor blinking period.
5. wv0-wv3 specify the pulse width of vertical sync signal.
wh0-wh3 specify the pulse with of horizontal sync signal.
6. R0 is ordinally programmed to be an odd number in interlace mode.
7. O; Yes, X; No.

2.5.4 GAIBVA LSI Gate Array (Figure 2-84)

The GAIBVA LSI gate array, an 80-pin flat-pack, converts display memory addresses from the 46505 and inputs from the APX-ISYM board into timing control signals for the VRAMs and the GAIBVD gate array. The GAIBVA is clocked (pin 28) at 5.3 MHz, the same rate as the 8088. This device regulates CPU and display requests for VRAM access using the WAIT output (pin 44). The CRTC has priority over the 8088 for access to APX-ICRT VRAM. The number of wait cycles is not fixed, and varies with the display mode.

All display addresses generated by the 46505 are input to the GAIBVA (pins 46-50 and 53-61),where they are multiplexed into the VRAM address signals (VRA0-7, pins 72 and 74-80). All I/O port address decoding for the 46505 is done in the GAIBVA gate array. The GAIBVA chip performs address mapping of the 46505 for IBM color and monochrome emulation. The chip select signals for the 46505 are output on pins 64-67.

To synchronize operations with the GAIBVD gate array, the GAIBVA outputs signals on pins 3-10, including the CPU control signals (CPRQ and CPAK), VRAM control signals (MPX, MALT, $\overline{MRD}$ and $\overline{MWR}$), and the I/O port range select signals (W3CX and $\overline{RW3X}$).The GAIBVA pin description is provided in Table 2-45.

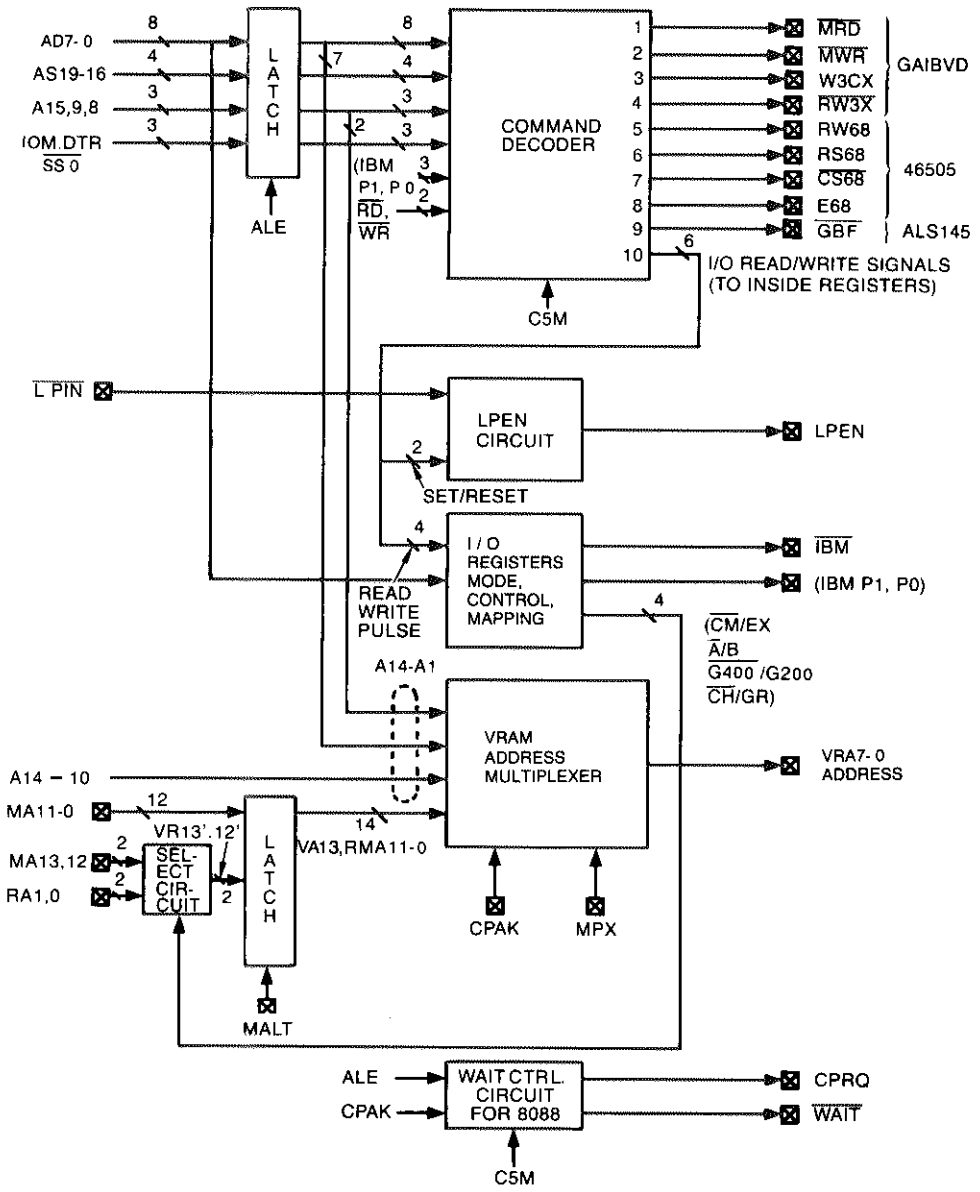


FIGURE 2-84. GAIBVA LSI BLOCK DIAGRAM

TABLE 2-45. GAIBVA PIN DESCRIPTION

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1,2	RA0,1	IN	Raster address input from 46505.
3	$\overline{MWR}$	OUT	VRAM memory write signal for addresses in the range B0000H-BFFFFH.
4	$\overline{MRD}$	OUT	VRAM memory read signal for addresses in the range B0000H-BFFFFH.
5	$\overline{RW3X}$	OUT	I/O select for port addresses in the range 03B0H-03DFH.
6	W3CX	OUT	Write pulse for control and mapping registers in GAIBVD.
7	MALT	IN	Memory address latch timing signal from GAIBVD.
8	MPX	IN	Multiplex signal for RAS and CAS timing from GAIBVD 0 = RAS 1 = CAS
9	CPAK	IN	CPU acknowledge signal for VRAM access.
10	CPRQ	OUT	CPU request signal for VRAM access.
11	ALE	IN	Address latch enable signal input from 8088 CPU
12,52	Vss	—	Ground.
13	LPSW	IN	Light pen signal input. Not used in the QX-16
14-21	AD0 7	IN/OUT	Multiplexed address and data bus for bits 0-7.
22	RSET	IN	Reset signal input.
23,63 68-71	N/C	—	No connection - unused pins.
24	C5M	IN	8088 CPU clock signal (5.3248MHz).
25	DT/$\overline{R}$	IN	Data bus direction signal from the 8088 CPU 0 = External device drives bus 1 = CPU drives bus
26	$\overline{WR}$	IN	8088 write signal.
27	IO/$\overline{M}$	IN	8088 bus control signal. 0 = Memory access 1 = I/O access
28	$\overline{RD}$	IN	8088 read signal.
29	$\overline{GBF}$	OUT	Control signal for LS245 bus buffer.
30	A8	IN	Address line 8 from 8088.
31	$\overline{SS0}$	IN	Status control line from 8088.
32	A9	IN	Address line 9 from 8088.
33,73	Vdd	–	+5V supply connection.
34	AS19	IN	Address/Status line 19 from 8088.
35	A10	IN	Address line 10 from 8088.
36	AS18	IN	Address/Status line 18 from 8088.
37	A11	IN	Address line 11 from 8088.

TABLE 2-45. GAIBVA PIN DESCRIPTION (Continued)

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
38	AS17	IN	Address/Status line 17 from 8088.
39	A12	IN	Address line 12 from 8088.
40	AS16	IN	Address/Status line 16 from 8088
41-43	A13—A14	IN	Address lines 13-14 from 8088.
44	$\overline{\text{WAIT}}$	OUT	Wait signal to synchronize CPU accesses to VRAM.
45	$\overline{\text{IBM}}$	OUT	IBM emulation mode signal 0 = APX-ICRT active 1 = APX-ICRT disabled
46-50 53-61	MA0—13	IN	VRAM memory address signals from 46505.
51	$\overline{\text{LPIN}}$	IN	Light pen switch input. Not used in the QX-16.
62	LPEN	OUT	Light pen flag. Not used in the QX-16
64	RS68	OUT	46505 register select signal. 0 = Address register 1 = Data register
65	CS68	OUT	46505 chip select signal.
66	E68	OUT	46505 enable signal.
67	RW68	OUT	I/O read/write signal for 46505.
72,74-80	VRA0—VRA7	OUT	Multiplexed VRAM address lines.

2.5.5 GAIBVD LSI Gate Array (Figure 2-85)

The GAIBVD LSI gate array, also an 80-pin flat-pack, receives input signals from the 46505, VRAMs, character generator, and the GAIBVA gate array, and converts these to VRAM control signals, character generator addresses, and video output signals. The GAIBVD performs display attribute control according to data received from the VRAM circuits. The main timing signal for this chip is the 16 MHz signal generated by CR1 and input to pin 41 (Refer to Table 2-46.)

VRAM control varies with the selected display mode and the type of access being performed. The GAIBVD controls the memory $\overline{RAS}$ and $\overline{CAS}$ control lines to specify the type of address being output from the GAIBVA. When the 8088 CPU is accessing VRAM, the output data are read into the GAIBVD, then transferred to the system data bus via the ALS245 buffer (IC 1E). In display mode, VRAM data is read into the GAIBVD, which converts it to the video signal (graphic mode) or supplies it to the character generator (character mode). The video dot patterns loaded into the GAIBVD from VRAM or the character generator are converted to the appropriate signals based on the mode and color information programmed in the GAIBVD.

Two jumpers on the APX-ICRT board are available for modifying the operation of the GAIBVD; both J1 and J2 are factory set open. Normally, VRAM data are refreshed when the APX-ICRT board is disabled. When jumper J1 is installed, refresh is inactive and VRAM data are lost when the board is disabled. The open configuration of J2 eliminates video output interference during access by the CPU in high resolution character mode (80x25). When J2 is closed, display interference is caused when the 8088 tries to access VRAM; to prevent interference, high speed RAMs (MB81416-10) should be installed at 3B-3E.

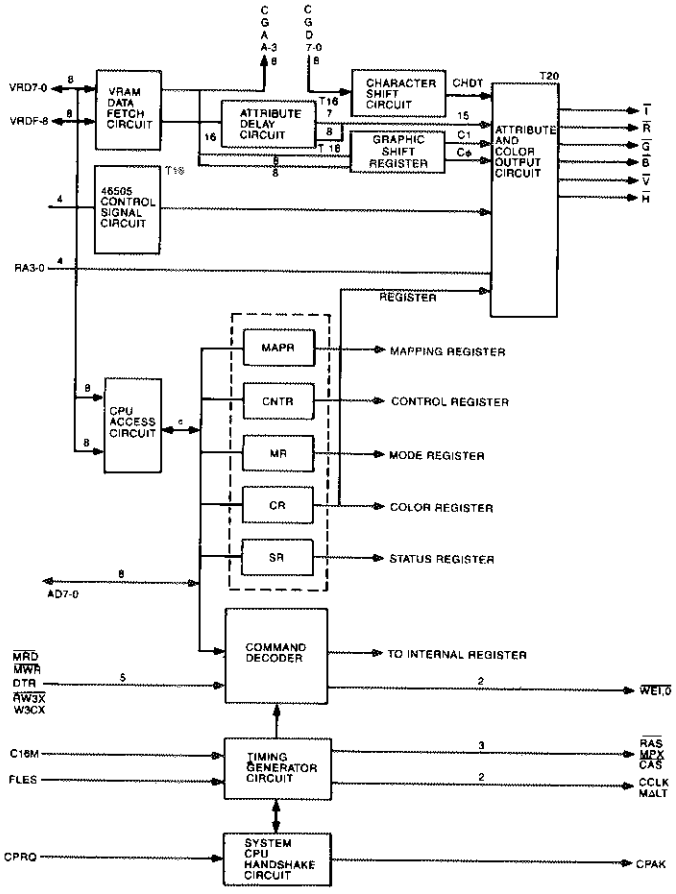


FIGURE 2-85. GAIBVD LSI BLOCK DIAGRAM

TABLE 2-46. GAIBVD PIN DESCRIPTION

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
1	FLES	IN	Controls VRAM access mode 0 = Flash mode 1 = Flashless mode
2 9,72 74-80	VRD0-VRDF	IN/OUT	VRAM bidirectional data signals.
10 11 13 18	CGD0-CGD7	IN	Character generator data inputs.
12,52	Vss	—	Ground
19-28	CGA3-CGAC	OUT	Character generator address outputs.
29	$\overline{I}$	OUT	Video intensity signal.
30	$\overline{H}$	OUT	Horizontal sync signal.
31	$\overline{G}$	OUT	Green video signal.
32	$\overline{V}$	OUT	Vertical sync signal.
33,73	Vdd		+5V supply connection.
34	$\overline{R}$	OUT	Red video signal
35	$\overline{B}$	OUT	Blue video signal.
36	CU68	IN	Active high cursor timing signal from the 46505.
37	VS68	IN	Vertical sync input from 46505.
38	DI68	IN	Active high display timing signal from the 46505.
39	HS68	IN	Horizontal sync signal from the 46505
40	CCLK	OUT	46505 controller clock.
41	C16M	IN	16MHz master timing signal from CR1.
42	DT/$\overline{R}$	IN	8088 bus direction control signal.
43	RSET	IN	Reset signal input.
44-51	AD0—AD7	IN/OUT	Multiplexed bidirectional address and data lines to system bus.
53	TEST	IN	Active low input stops timing circuits.
54	ALE	IN	8088 address latch enable signal.
55	CPRQ	IN	CPU request input for VRAM access.
56	CPAK	OUT	Acknowledge for CPU VRAM request.
57	MPX	OUT	VRAM address multiplex signal. 0 = RAS 1 = CAS
58	MALT	OUT	Memory address latch timing signal to GAIBVA.
59	W3CX	IN	Write pulse for control and mapping registers.
60	$\overline{RW3X}$	IN	I/O select for port addresses in the range 03B0H-03DFH
61	$\overline{MRD}$	IN	VRAM memory read signal for addresses in the range B0000H-BFFFFH

TABLE 2-46. GAIBVD PIN DESCRIPTION (Continued)

PIN NO.	SIGNAL	DIRECTION	DESCRIPTION
62	$\overline{MWR}$	IN	VRAM memory write signal for addresses in the range B0000H-BFFFFH
63-66	RA0 RA3	IN	Raster address inputs from 46505.
67	TQD	OUT	Test signal for timing circuit. Not used in the QX-16
68	$\overline{CAS}$	OUT	Column address strobe for VRAMs.
69	$\overline{RAS}$	OUT	Row address strobe for VRAMs.
70-71	$\overline{WE0}$—$\overline{WE1}$	OUT	Write enable signals for VRAMs. 0 = Write 1 = Read

2.5.6 VRAM Memory and Character Generator Circuits (Figures 2-86 through 2-90)

The VRAM circuit, four MB81416-10 dynamic RAMs (ICs 3B-3E), store the character code and attribute data in character mode and the contents of the display image in graphics mode. Unlike the APX-IGGS board, which is I/O mapped, the APX-ICRT board is mapped to the 8088 address space, and the VRAM are directly accessible similar to system memory. The 32K bytes of VRAM are mapped to addresses B0000H-B7FFFH or B8000H-BFFFFH, depending on the contents of the mapping register at I/O location 03CFH. (Refer to Chapter 6 for an overview of I/O register mapping.)

During VRAM addressing, the 8088 accesses the VRAM memory as consecutive addresses, starting at B0000H, with a single byte at each address; however, the 46505 treats each address as two bytes. This means that the 8088 sees VRAM as 7FFFH locations while the 46505 sees only 3FFFH locations. This conflict is resolved in the GAIBVA and GAIBVD gate arrays, which translate the data according to the source. Data are transferred between the GAIBVD and VRAMs over a 16-bit bidirectional bus. Because of the expanded memory capacity on this board, the VRAMs are separated into two groups. The row and column addresses for both groups are output by the GAIBVA and are synchronized with the $\overline{RAS}$ and $\overline{CAS}$ outputs of the GAIBVD. Data are written into the VRAMs when the write enable input (WE pin 4) is low. ICs 3B and 3C are controlled by the $\overline{WE1}$ signal (IC 2F pin 71) and ICs 3D and 3E are controlled by the $\overline{WE0}$ signals (IC 2F pin 70).

CPU data to be written to or read from the system data bus are directed through the GAIBVD. Display data are sent to one of two destinations: in character mode, the data are used to select the character pattern from the 8K-byte EPROM character generator (see Section 2.5.6.1); in graphic mode, data from the VRAMs are converted to display pixels based on programmed resolution and color information (Section 2.5.6.2), and the character generator is not used. High and low resolution displays are possible in each mode, enabling a wide variety of display formats to be established. Tables 2-47 and 2-48 summarize the most common modes, and Figure 2-87 diagrams VRAM memory allocation.

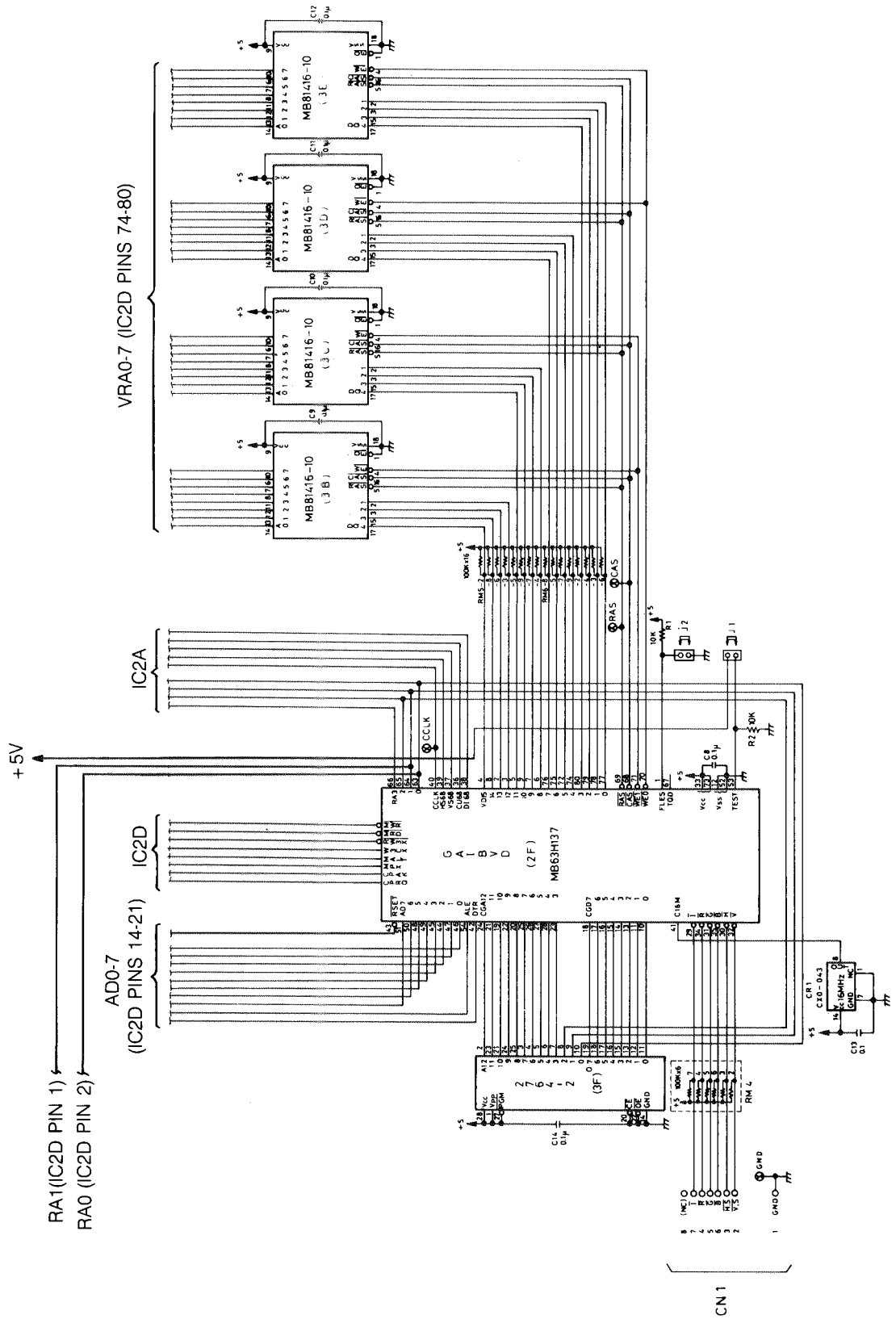
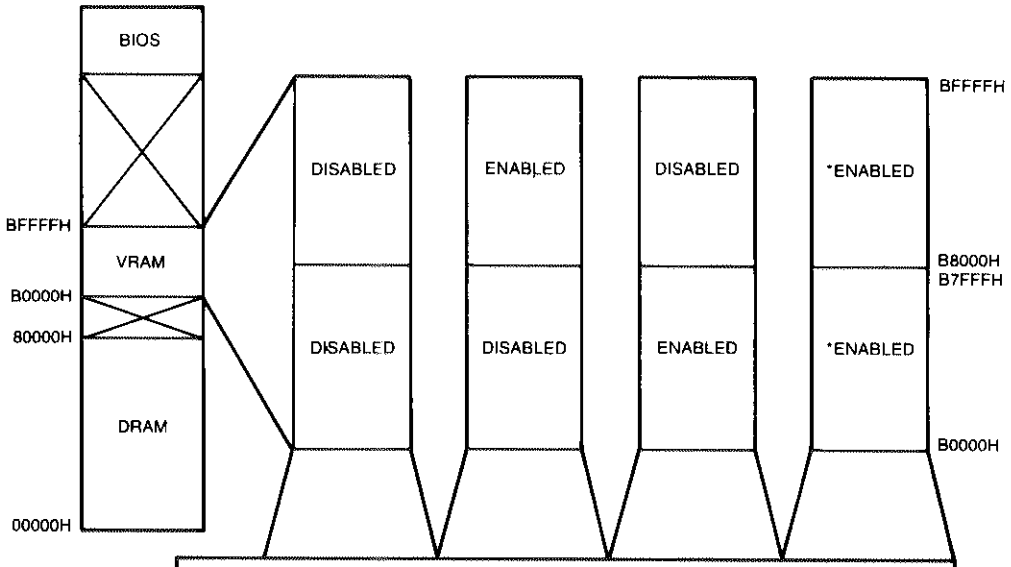


FIGURE 2-86. APX-ICRT VRAM/CHARACTER GENERATOR CIRCUIT



PORT 03CFH - MAPPING REGISTER					
BIT 7	0	1	1	1	1
BIT 6	X	0	1	0	1
BIT 5	X	0	0	1	1

X = NOT USED

* = ADDRESSES ARE DUPLICATED (i.e., B0000H = B8000H)

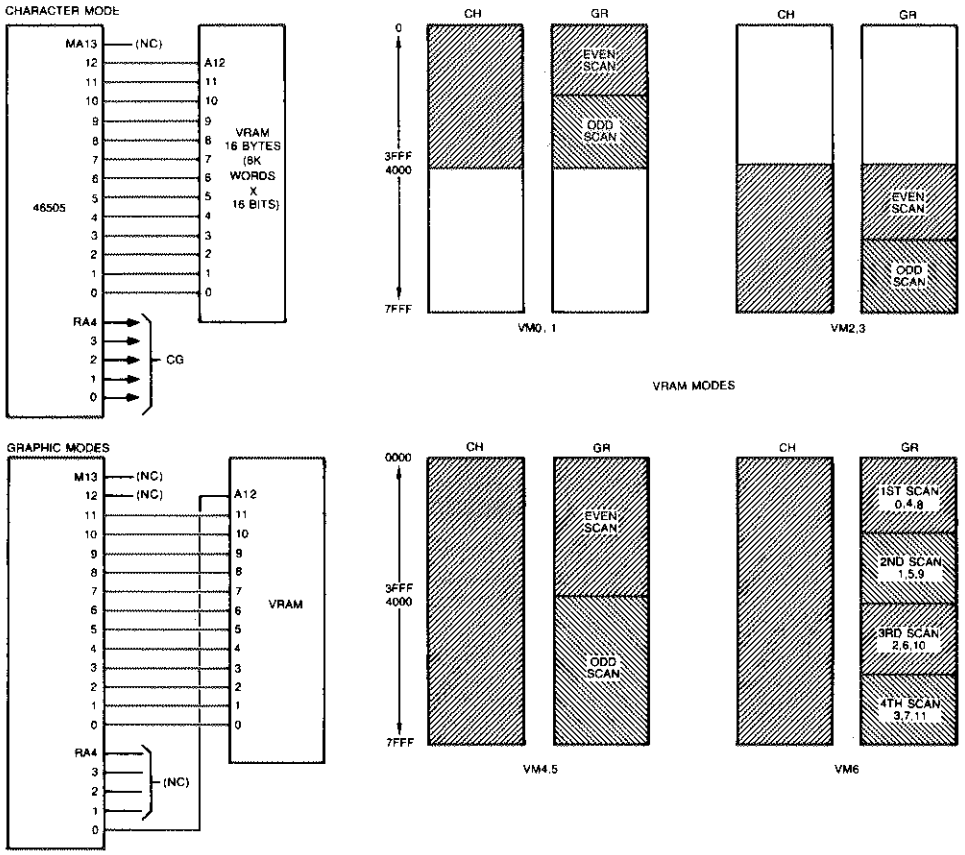


FIGURE 2-87. APX-ICRT VRAM MEMORY CONFIGURATION

2.5.6.1 Character Mode (Figure 2-88)

When the display is used in character mode, the graphics selection signal, GR, bit 1 of the mode register (03B8H in monochrome, 03D8H in color), must be set to 0, and the character generator provides character patterns to the GAIBVD gate array. In the two-byte character address data, the even numbered addresses (2n, Figure 2-88) store character codes and the odd numbered addresses (2n + 1) store attribute data.

The character generator stores three character sets: 7x12, 7x7, or 5x7 characters in corresponding 8x16 or 8x8 (for both 7x7 and 5x7) matrices. Character codes are supplied to the character generator on address lines A3-A10. The two upper address lines (A11, A12) select one of four character sets: the upper half of the 8x16 matrix, the lower half of the 8x16 matrix, the 7x7 font, or the 5x7 font. The upper and lower halves of the 8x16 matrix are selected by the 46505 raster address signal (RA3). The three lower raster address signals (RA0-RA2), connected to character generator address lines A0-A2, select the appropriate scan row for each character. The character dot patterns are then read by the GAIBVD and converted to video output signals.

Character matrices are determined by bits 4 (C16/8) and 3 (C77/C57) of the control register (03CEH), in conjunction with maximum raster address, programmed to register R9 of the 46505, as described below:

7x12 font (8x16 matrix area): 03CE bit 4 = 0, bit 3 is disregarded, and R9 = 0F. At the CG, A12 = 0, A11 = RA3, and 4K bytes CG ROM (0000-0FFF) are used. When a character matrix of more than 8 dots vertically is selected, the dot pattern for each character is divided and stored in two locations: 0000-07FF for the upper 8 dots, 0800-0FFF for the lower dots.

7x7 font (8x8 matrix area): 03CE bit 4 = 1, bit 3 = 0, and R9 = 07. At the CG, A12 = 1, A11 = 1, and 2K bytes CG ROM (1800-1FFF) are used.

5x7 font (8x8 matrix area): 3CE bit 4 = 1, bit 3 = 1, and R9 = 07. At the CG, A12 = 1, A11 = 0, and 2K bytes CG ROM (1000-17FF) are used.

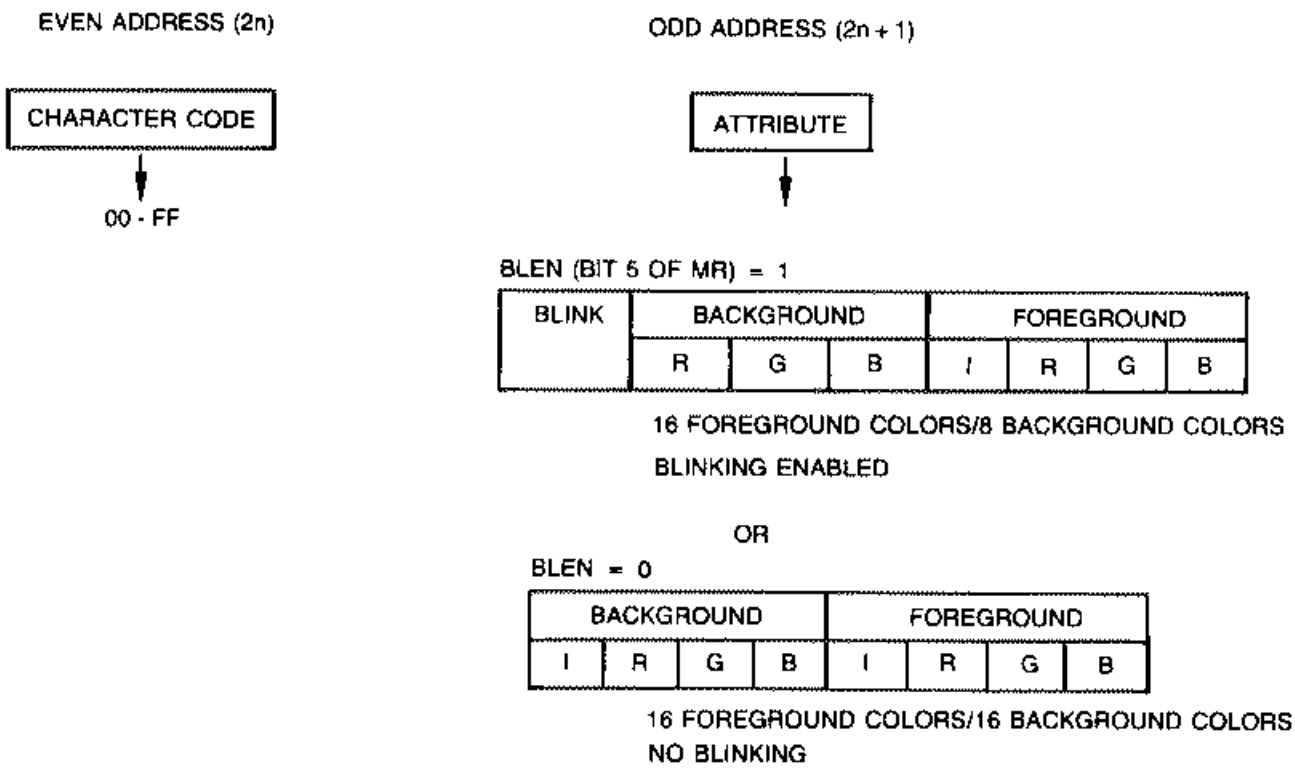


FIGURE 2-88. CHARACTER AND ATTRIBUTE DATA FORMAT

TABLE 2-47. APX-ICRT SAMPLE CHARACTER DISPLAY MODES

MODE		LOW-RES (LCH)	MODIFIED LOW-RES (LLCH)	HIGH-RES (HCH)	MODIFIED HIGH-RES (HHCH)
CRT TYPE (LINES)		200 / 400	200	200 / 400	400
CHARACTER COLUMNS/LINES		40 × 5	40 × 12	80 × 25	80 × 50
VRAM/PAGE		2K	1K	4K	8K
CONTROL REGISTER (03CEH)	Bit 4 (C16.C8)	1 / 0	0	1 / 0	1
	Character Matrix	8 × 8 / 8 × 16	8 × 16	8 × 8 / 8 × 16	8 × 8
46505 DATA REGISTER (03B5H, 03D5H)	R1 (Horizontal)	28H (40)	28H (40)	50H (80)	50H (80)
	R6 (Vertical)	19H (25)	0CH (12)	19H (25)	32H (50)
	R9 (Repeat)	07H (8) / 0FH (16)	0FH (16)	07H (8) / 0FH (16)	07H (8)
MODE REGISTER (03B8H, 03D8H)	Bit 0 (HCH)	0	0	1	1
	Bit 1 (GR)	0	0	0	0
	Bit 4 (HGR)	0	0	0	0
	Bit 5 (BLEN)	1	1	1	1

2.5.6.2 **Graphic Modes** (Figure 2-89)

To establish graphic mode, the GR signal, bit 1 of the mode register (03B8H in monochrome, 03D8H in color) must be 1. Graphics data are viewed in 2-bit pairs for low resolution displays and individually for high resolution displays.

Graphics includes seven video modes, distinguishable by display size and allocation of VRAM memory. Displays of 200 or 400 lines are selected by the setting of maximum raster address R9 of the 46505. R9 = 01 provides a 200 line display, and R9 = 03 provides a 400 line display. VRAM allocation is determined by bits 7, 6, and 5 of the control register (CNTR, at 03CEH), as follows:

CM/EX (bit 7) = 0: 16K bytes VRAM used
= 1: 32K bytes VRAM used

A/B (bit 6) = 0: Addresses 0000-3FFF are accessed.
= 1: Addresses 4000-7FFF are accessed.

G400/G200 (bit 5) = 0: With raster address R9 set to the maximum, 03, each display line is repeated, resulting in a 400 line display.

= 1: With raster address R9 set to 01, this produces a 200 line display. If a 400 line CRT is attached, the 200 lines will be compressed in the upper half of the screen.

The resulting display modes are identified as VRAM modes VM0-7; however, VM7 is the same as VM5 and is therefore not listed.

NOTE: *The lower half of the accessed address space is used for the even scan lines and the upper half for odd scans in all configurations except VRAM mode 6. (Refer to Figure 2-88.)*

VM0: Lower 16K bytes VRAM (0000-3FFF), with R9 = 03, causing each line to be displayed twice for a 400 line display.

VM1: Lower 16K bytes VRAM (0000-3FFF), with R9 = 01; each line is displayed once for a 200 line display.

VM2: Same as VM0, using the upper 16K bytes VRAM (4000-7FFF).

VM3: Same as VM1, using the upper 16K bytes VRAM (4000-7FFF).

VM4: Enables use of all 32K bytes VRAM by using 0000-3FFF for the even scan data and 4000-7FFF for the odd scans; R9 = 03, causing repeat scanning and a 400 line display.

VM5: Same as VM4 but with R9 = 01, resulting in a 200 line display.

VM6: 0000-7FFF; R9 = 03 and R6 (vertical display height) = 64. 32K bytes VRAM, 400 line display without repeat. Address space is split into 48K-byte blocks. The first scan uses raster data from the lowest address block, the second scan from the second block, the third scan from the third block, etc., and the cycle is repeated for subsequent scans. (Refer to Figure 2-87.)

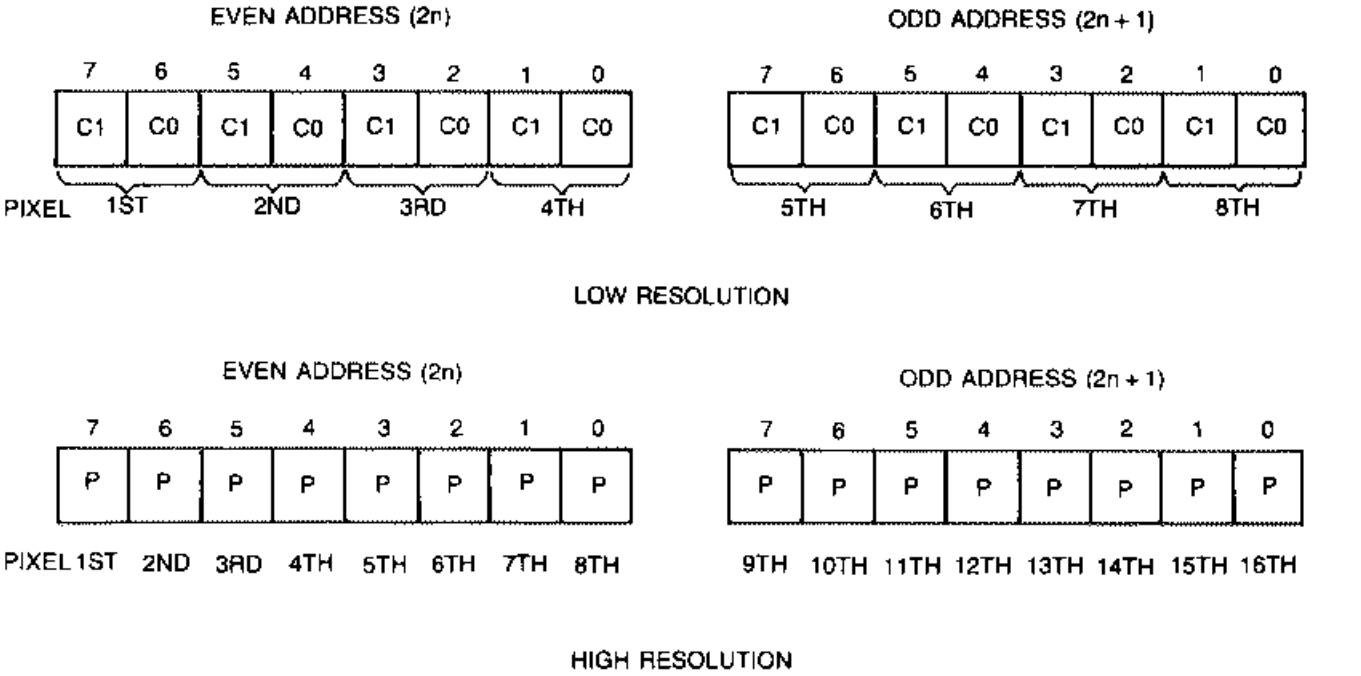


FIGURE 2-89. GRAPHIC DATA FORMAT

TABLE 2-48. APX-ICRT SAMPLE GRAPHIC DISPLAY MODES

MODE		LOW-RES (LCH)	MODIFIED LOW-RES (LLCH)	HIGH-RES (HCH)	MODIFIED HIGH-RES (HHCH)
CRT TYPE (LINES)		200 / 400	200	200 / 400	400
DISPLAY SIZE (PIXELS)		320 × 200 (Note 1)	160 × 100 (Note 2)	640 × 200 (Note 1)	640 × 400 (Note 3)
VRAM/PAGE		8K	16K	16K	32K
CONTROL REGISTER (03CEH)	Bit 5 (6400/6200)	1 / 0	0	1 / 0	1
	Bit 6 (*A/B)	—	·	·	1
	Bit 7 (CM/EX)	—	—	— / 0	1
46505 DATA REGISTER (03B4H, 03D4H)	R1 (Horizontal)	28H (40)	50H (80)	28H (40)	28H (40)
	R6 (Vertical)	64H (100)	64H (100)	64H (100)	64H (100)
	R9 (Repeat)	07H (8) / 0FH (16)	0FH (16)	07H (8) / 0FH (16)	07H (8)
MODE REGISTER (03B8H, 03D8H)	Bit 0 (HCH)	0	0	1	1
	Bit 1 (GR)	0	0	0	0
	Bit 4 (HGR)	0	0	0	0
	Bit 5 (BLEN)	1	1	1	1

NOTE. 1. The graphic data are duplicated to fill the display page.
2. LLGR is 16-color graphics derived from HCH mode. Both the underline enable, ENU, and monochrome/color selection, B/W, must be 0 in LLGR mode. (Refer to Chapter 6)
3. In HHGR mode, the display data is not duplicated. Refer to the description of VM6.

2.5.6.3 Monochrome/Color Display Modes

Monochrome/Color Selection

Bit 1 of the 46505 control register (B/W) is used to determine whether monochrome or color display mode is supported. If B/W = 1, a monochrome display is produced on either a monochrome or color monitor. If B/W = 0, the video signals are output as R, G, B, and I, and only a color monitor will produce an accurate display; monochrome monitors will display scrambled data. Table 2-49 lists the RGB and intensity signal combinations which produce the 16 possible display colors.

Color Selection and Blinking

Color data display methods vary according to whether high or low resolution character or graphic mode is in effect and whether a color or monochrome monitor is connected to the system. (Refer to the summary in Table 2-50.)

If a color display and character mode are used, the 8-bit attribute data is divided to establish background and foreground colors, intensity, and enabling or disabling of blinking (Figure 2-88). When the blinking enable signal, BLEN, bit 5 of the mode register, equals 1, blinking is controlled by bit 7 of the attribute data; bits 0-3 of the attribute data indicate the foreground color as described in Table 2-49, and bits 4-6 establish the background color. When BLEN = 0 and blinking is inactive, bit 7 of the attribute data is used as the background intensity signal.

Color graphic mode defines each pixel by consecutive pairs of bits, C1 and C0, for low resolution displays, and bit-by-bit for high resolution displays (Figure 2-89). In low resolution mode, the active color set is selected according to the CSEL and BACKI signals of the color register (03D9H). One of the four colors in each set is selected by the C0 and C1 pixels, as described in Table 2-51.

Color data may be displayed on a monochrome monitor when B/W = 1. To do so, the pixel is "white," or foreground, when C1 or C0 equals 1, with intensity determined by BACKI; when C1 and C0 are both 0, the pixel is "black," or background, with intensity determined by bit 3 of the color register. The foreground/background relationship is reversed when attribute bits 0-2 are all 0 and bits 4-6 are all 1.

TABLE 2-49. RGB/DISPLAY COLOR COMBINATIONS

COLOR	I	R	G	B
Black	0	0	0	0
Blue	0	0	0	1
Green	0	0	1	0
Cyan	0	0	1	1
Red	0	1	0	0
Magenta	0	1	0	1
Brown	0	1	1	0
White	0	1	1	1
Gray	1	0	0	0
Light Blue	1	0	0	1
Light Green	1	0	1	0
Light Cyan	1	0	1	1
Light Red	1	1	0	0
Light Magenta	1	1	0	1
Yellow	1	1	1	0
White (High Intensity)	1	1	1	1

TABLE 2-50. COLOR SETS BY MODE

MODE	FOREGROUND	BACKGROUND	BORDER
CHARACTER			
Low or High Resolution Color (LCHC, HCHC)	One of 16 colors derived from attribute bits 3-0.	16 colors non-blinking / 8 colors with blinking derived from attribute bit 6-4.	16 colors derived from CR (03D9H).
Low or High Resolution Monochrome (LCHM, HCHM)	White Intensity (I) derived from attribute bit 3.	Black I = 0	Black Intensity derived from color register, bit 3.
GRAPHIC			
Low Resolution Color (LGRC)	(Refer to Table 2-51)	16 colors C1, C0 = 0, 0 IRGB derived from color register (03D9H).	
Low Resolution Monochrome (LGRM)	White C1, C0 = 0, 0 Intensity derived from BACKI, bit 4 of color register.	Black Intensity derived from bit 3 of color register.	(Same as background)
High Resolution Color (HGRC)	One of 16 colors (bit = 1) IRGB derived from bits 3-0 of color register. (Refer to Table 2-49)	Black (bit = 0)	
High Resolution Monochrome (HGRM)	White (bit = 1) Intensity derived from bit 3 of color register.	Black (bit = 0)	

TABLE 2-51. LGRC MODE COLOR SETS

COLOR SET	0	1	2	3
CSEL	0	0	1	1
BACKI	0	1	0	1
C1, C0 = 0, 1	Green	*H.I. Green	Cyan	H.I. Cyan
C1, C0 = 1, 0	Red	H.I. Red	Magenta	H.I. Magenta
C1, C0 = 1, 1	Brown	Yellow	White	H.I. White
C1, C0 = 0, 0	One of 16 background colors. IRGB outputs determined by bits 3-0 of color register (03D9H).			

* H.I. = High Intensity
NOTE: I = Color Register bit 4 (BACKI). R = C1 G = C0, and B = CR bit 5 (CSEL).

2.5.6.4 Underlining, Cursor Selection, CRT Polarity

Underlining

The monochrome emulation mode of the APX-ICRT has an underline attribute which is enabled by writing a 1 to bit 2 (ENU) of the control register (CNTR, 03CEH). Character-by-character underlining is displayed when the attribute byte for the character has bit 2 = 0, bit 1 = 0, and bit 0 = 1.

The underline bar is displayed in the eighth line when an 8x8 character matrix area is selected, and on the sixteenth line when a 8x16 matrix is used

Cursor Attributes

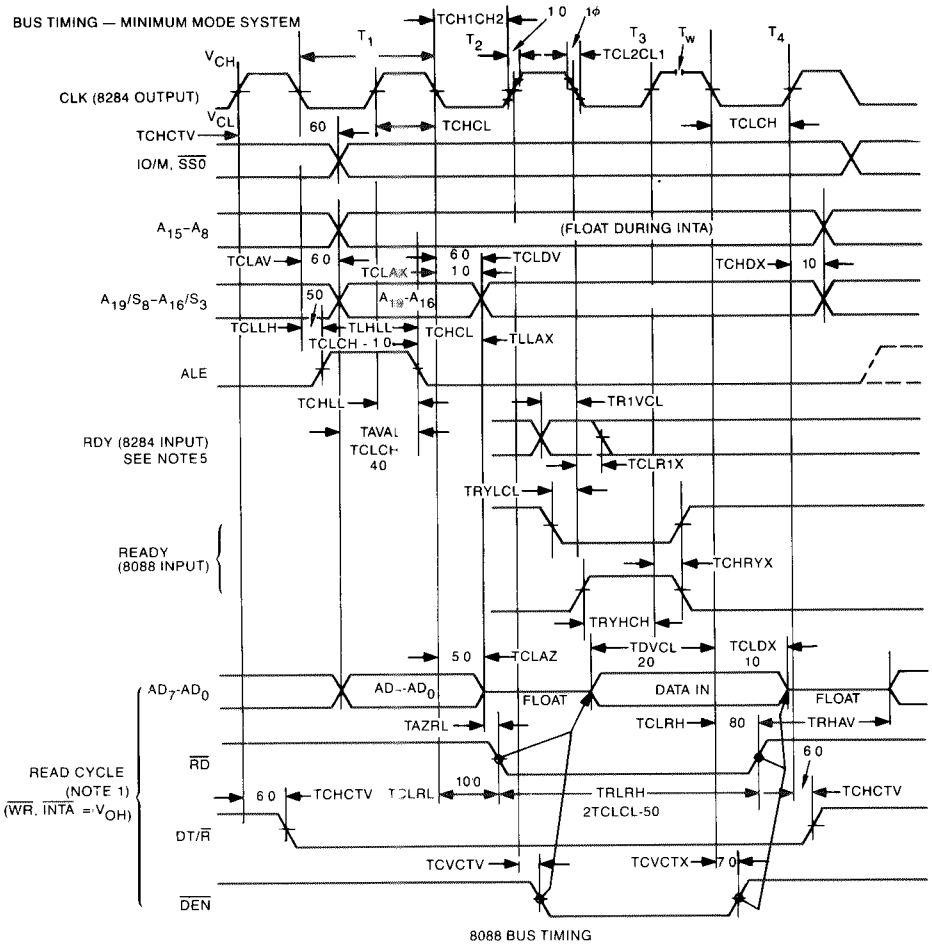
Cursor attributes are in effect only in character mode. Cursor blinking is turned on and off by bits 6 and 5 (B,P) of 46505 raster address R10. When both bits are 0, the cursor is displayed; when bit 5 = 1 and bit 6 = 0, the cursor is turned off. Bit 6 set to 1 enables the blinking function of the cursor. In standard operation, both bits are set to 0 and cursor blinking is controlled by the GAIBVD, which divides the VSYNC signal into 16 fields/ period for cursor blinking.

Cursor size and shape are set by the 46505. R10 and R11 specify the starting and ending scan rows for the cursor height, and R14 and R15 store the cursor address.

Sync Polarity

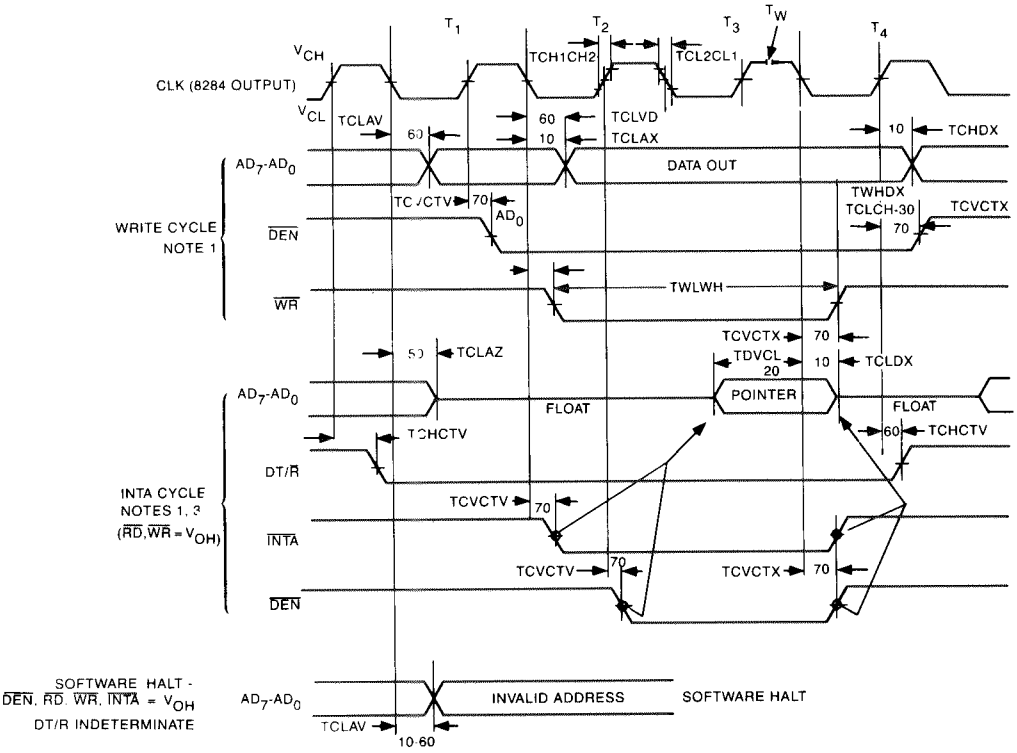
The VSYNC and HSYNC polarities may be set to positive or negative based on bit 0 (POL) of the control register. If bit 0 = 0, positive polarity is used on the CRT; if 1, negative polarity is in effect.

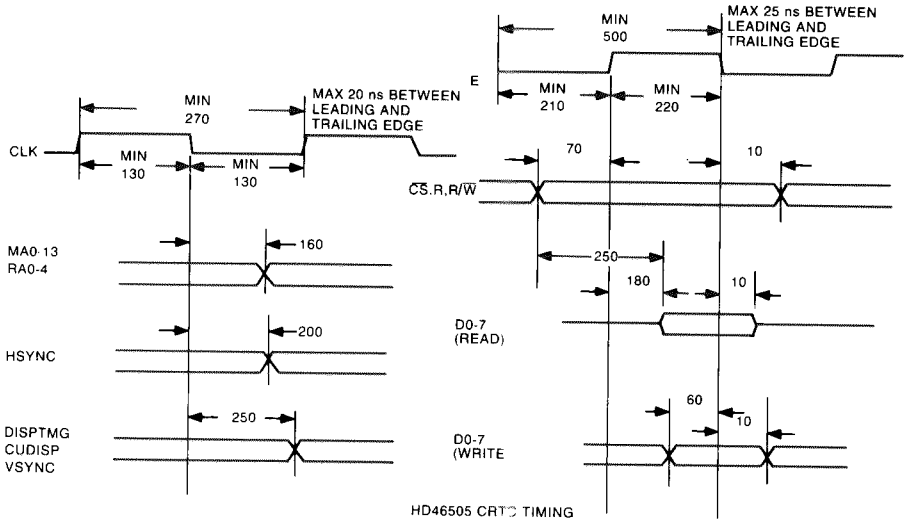
BUS TIMING — MINIMUM MODE SYSTEM



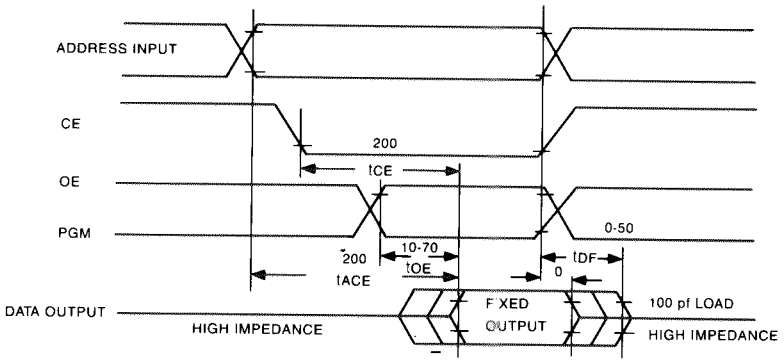
8088 BUS TIMING

NOTES: 1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
3. Two INTA cycles run back-to-back. The 8065 local address data is floating during both the INTA cycles. Control signals are shown for the second INTA cycle.
4. Signals at 8264 are shown for reference only.
5. All timing measurements are made at 1.5V unless otherwise noted.



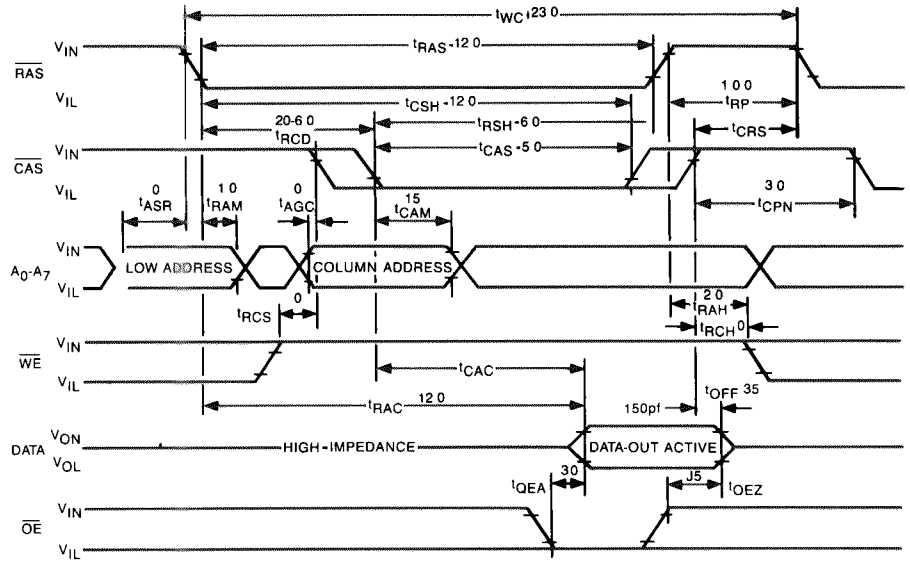


HD46505 CRTC TIMING

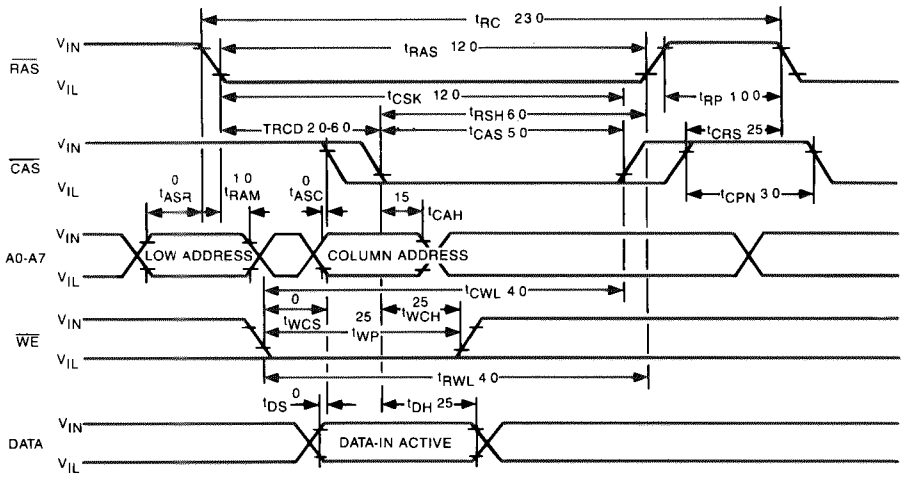


NOTE: t_{DF} is set by the leading edge of OE or CE, or the trailing edge of PGM, whichever is first.

27C64-20 TIMING



MB81416-10 READ TIMING



Note 1: OE does not depend on signal level.

2: After power is turned on, a 200 μs pause and 8 dummy cycles are needed.

MB81416-10 WRITE TIMING

FIGURE 2-90. APX-ICRT TIMING DIAGRAMS

2.6 SD-543 FLOPPY DISK DRIVE OPERATION

The SD-543 disk drive is very similar to Epson's SD-540, except it uses a mechanical head loading mechanism and a control board designed for use with the QX-16. The following is a brief summary of SD-543 operation, focusing on system use of the drives; for additional information on their basic mechanical construction, refer to the SD-540 technical manual.

2.6.1 FDD Main Control Board

The FDD main control board (refer to the schematic in Chapter 6) is composed of three basic circuits: a drive motor interface, which conveys drive select, motor phase, and sensor signals between the FDD motor control board and the APX-ISYM board; a write data circuit, which supplies side select, write, and erase signals to the heads; and a read amplifier circuit based on the MC3470 IC, which converts the peak of each AC differential signal received from the read/write heads to a digital signal for the APX-ISYM board (CN6 and CN7).

In the drive motor interface circuit, the $\overline{\text{MOTOR ON}}$ signal selects the active drive based on MTS0 and MTS1 signals from the GAFDDC (derived from DS0 and DS1 of the 765 FDC), and starts the drive motor. Phase signals ø1-ø4 drive the stepper motor. The stepper motor holding voltage is controlled by the SPM POW DOWN signal. The track 00 and write protect signals are also exchanged in this part of the circuit.

In the write portion of the FDD control circuit, the $\overline{\text{SIDE 1 SELECT}}$ signal activates the upper or lower head while WRITE 1 or WRITE 2 determines the drive to be written to. The ERASE GATE signal is used for write operations.

In the read amplifier circuit, the value of the $\overline{\text{SWITCH FILTER}}$ signal determines the constant of the differentiator circuit in the the read amp (0 = tracks 0-42; 1 = tracks 43-79).

2.6.2 Read/Write Head (Figure 2-91)

The SD-543 read/write head is flanked by two erase heads in a tunnel erase configuration. The upper and lower heads are gimballed to improve media contact and minimize disk wear. The head is loaded mechanically when the disk is inserted and moved track-to-track by a steel-band positioning mechanism.

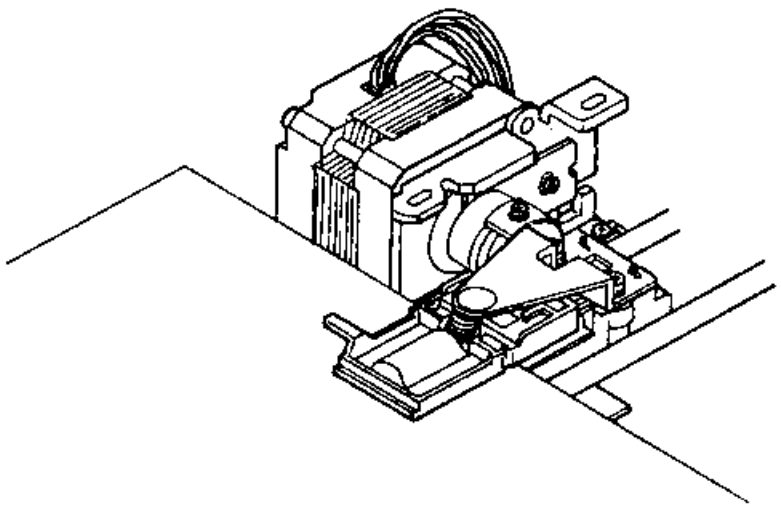


FIGURE 2-91. READ/WRITE HEAD

2.6.3 Disk Drive Motor and Motor Control Board (Figures 2-92 and 2-93)

A direct-drive spindle motor is built into the FDD motor control board. When the motor is activated by a low MOTOR ON signal (P3 pin 4), ICs 12 and 13 begin oscillation. IC 13, the motor driver IC, maintains a constant, 300 rpm disk-revolution rate (within 2.2%) based on signals received from the motor speed control chip, IC 12, a frequency-to-voltage converter. IC 12 compares the reference voltage, f2, established by VR2, R61, and C47, with the f1 voltage at the frequency generating coil of the circuit board, and adjusts the motor voltage accordingly: if motor rotation is too fast (f1 > f2), voltage is reduced; if motor speed is too slow (f2 > f1), voltage is increased. When the MOTOR ON signal goes high, Q6 turns on, oscillation is stopped, and the motor drive circuit turns off.

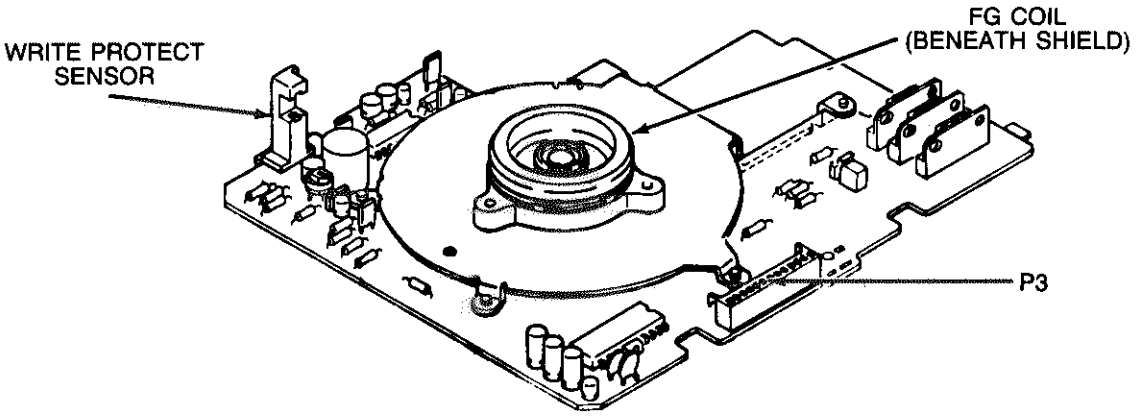


FIGURE 2-92. MOTOR CONTROL BOARD

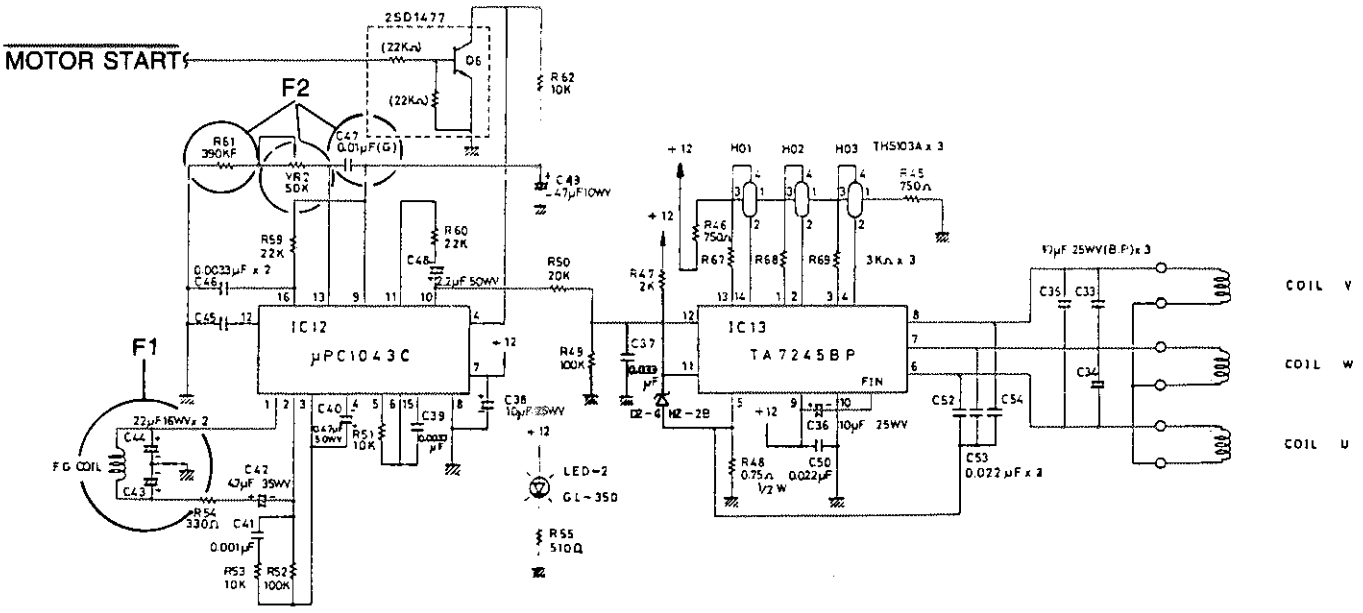


FIGURE 2-93. MOTOR SPEED CONTROL CIRCUIT

2.6.4 Stepper Motor (Figure 2-94)

The stepper motor moves the head one step in the direction specified by the transition of the ø1-ø4 signals supplied from the APX-ISYM board, using the steel belt connected to the motor shaft to translate the rotary movement to linear head movement. One complete rotation of the stepper motor equals 200 steps.

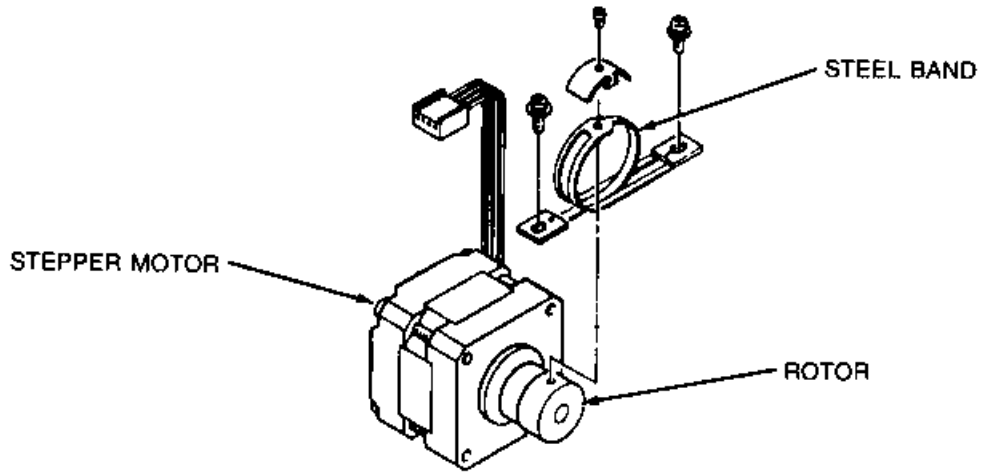


FIGURE 2-94. STEPPER MOTOR

2.6.5 Sensors

The index, write protect, and track 00 sensors are simple, LED-phototransistor detectors, which generate timing and reference signals used by the drive.

2.6.5.1 Index Sensor

The index sensor outputs a low signal each time the index hole of the disk passes over the phototransistor of the sensor. The trailing edge of the index pulse indicates the beginning of the track (Figure 2-95).

2.6.5.2 Track 00 Sensor

The track 00 sensor, located at the edge of the read/write area, determines the outermost position accessed by the read/write head. At power on, the read/write head returns automatically to track 00, initiating a low track 00 signal from which the location of subsequent tracks may be determined by the stepper motor.

2.6.5.3 Write Protect Sensor

When a write-protected disk is inserted in the drive, the write protect sensor outputs a low signal to the GAFDDC, which disables writing to the disk.

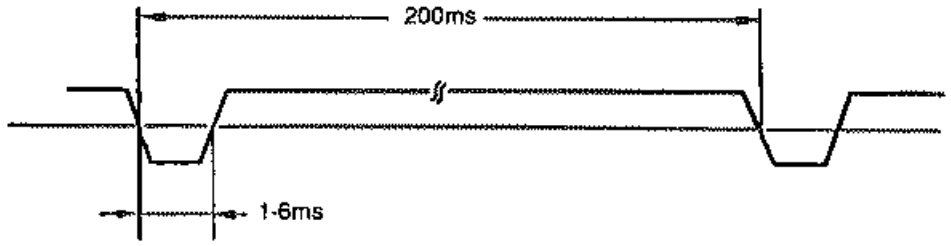


FIGURE 2-95. INDEX TIMING SIGNAL

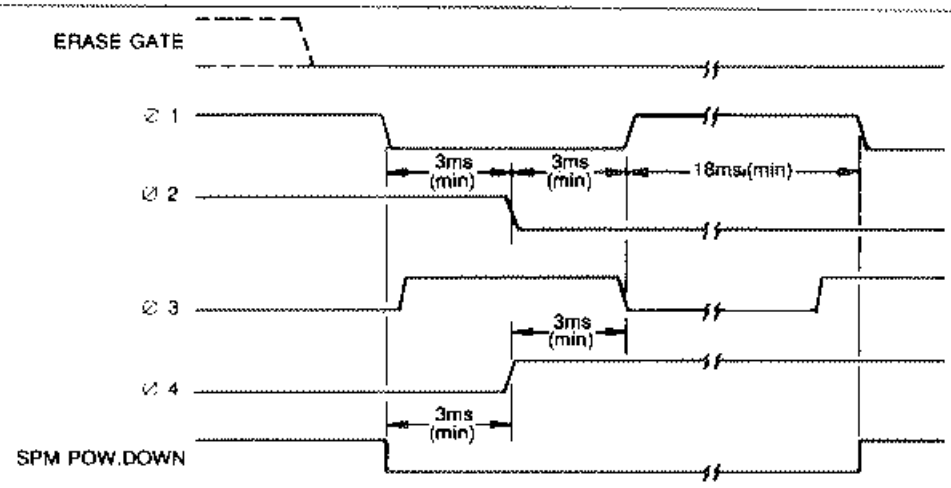


FIGURE 2-96. TRACK SEEK TIMING

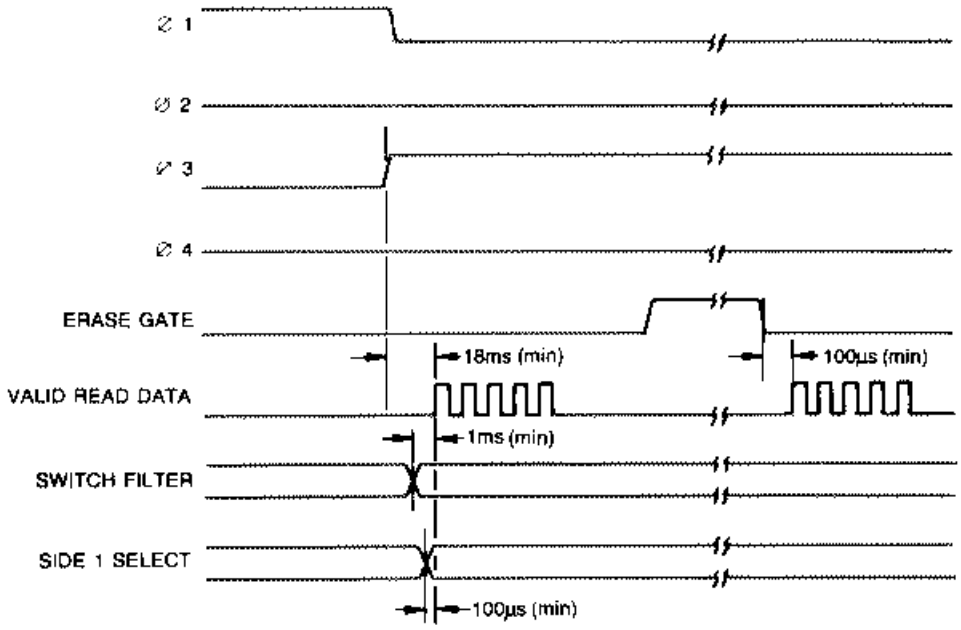


FIGURE 2-97. READ START TIMING

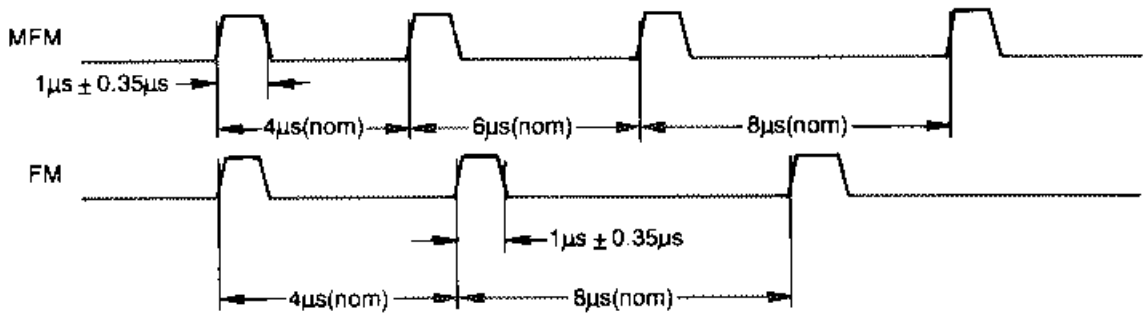


FIGURE 2-98. READ DATA TIMING

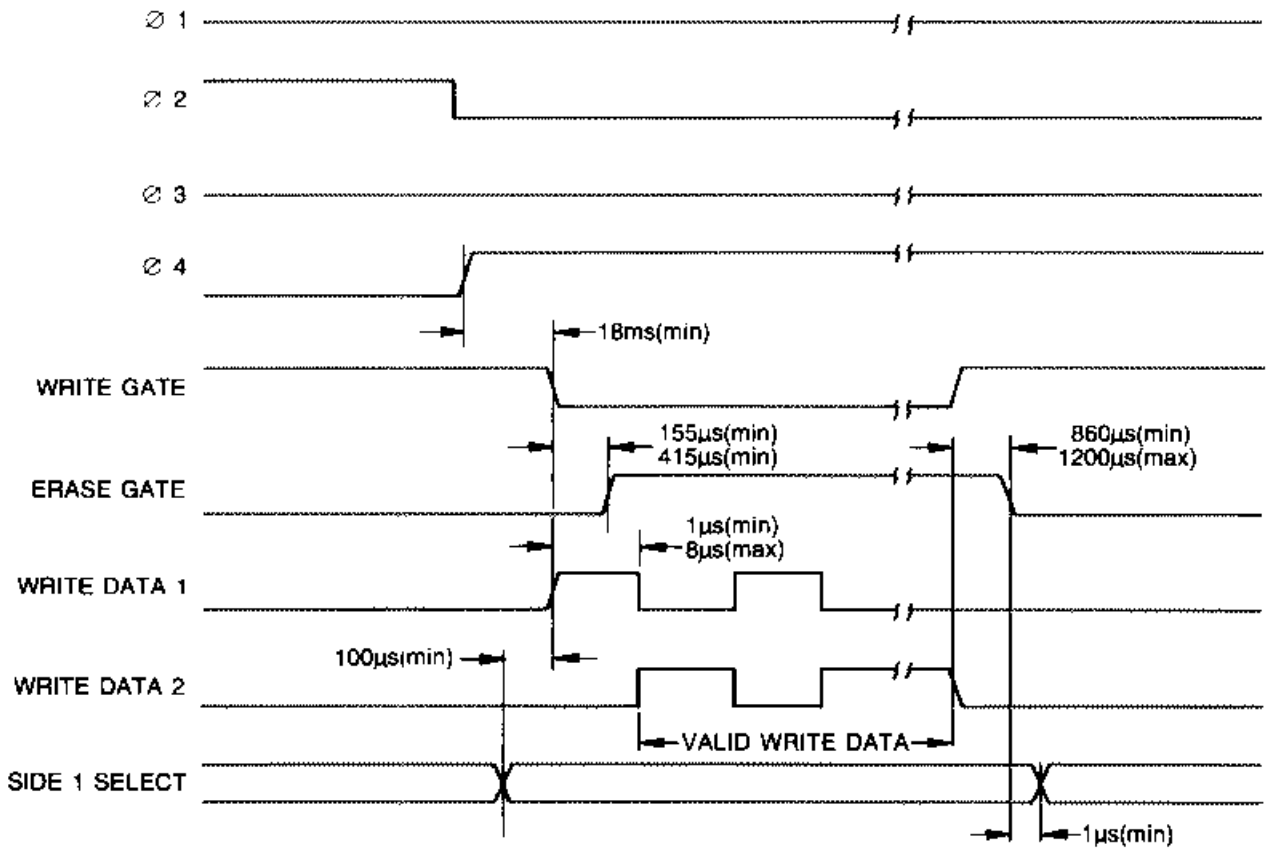


FIGURE 2-99. WRITE START TIMING

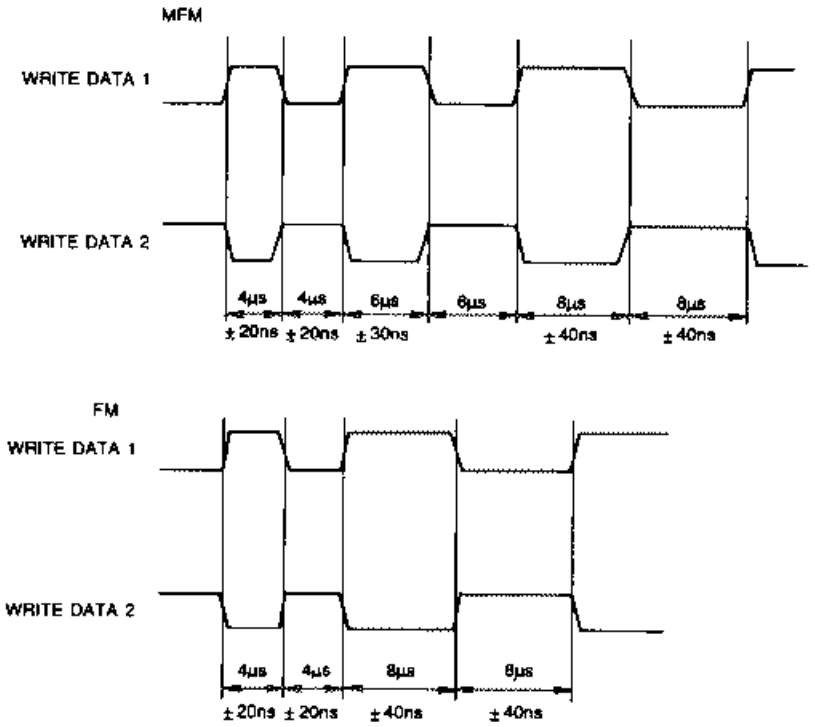


FIGURE 2-100. WRITE DATA TIMING

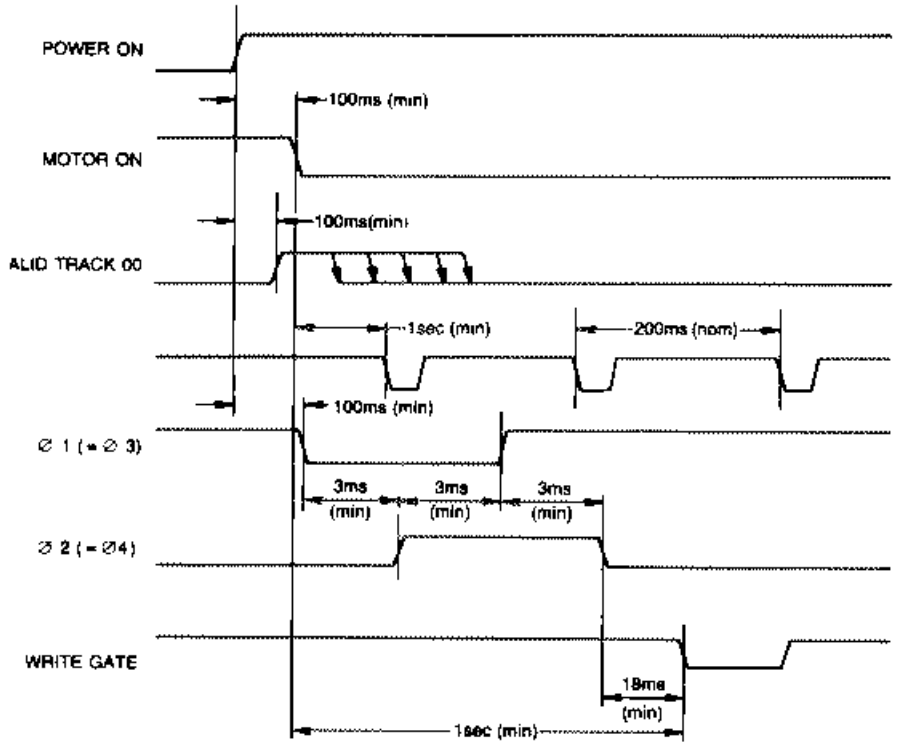


FIGURE 2-101. CONTROL DATA TIMING

2.7 KEYBOARD OPERATION (Figures 2-102 and 2-103)

The primary components of the keyboard are diagrammed below. Depression of any key on the keyboard unites a row signal with a column signal, enabling the T6830KB keyboard encoder IC to output a corresponding scan code to the 8049-020, which uses a synchronous format to serially transmit the keyboard codes to the main CPU. All keys except SHIFT, CRTL, and ALT have an automatic repeat function, which is activated if the key is depressed for longer than the programmed interval.

The keyboard clock signal, input to T0, is supplied from OUT1 of the 8253 programmable interval timer at 9C. The RxD data, input at the INT port (pin 6) of the 8049-020 via channel A of the 7201 multi-protocol serial controller, provides the reset signal, establishes key repeat intervals, and monitors the LEDs, as described in Chapter 6. The TxD data, output from the keyboard at P17 (pin 34) of the 8049-020, includes key codes, SHIFT, CRTL, and ALT switch data, and LED status signals. Data format for RxD and TxD is diagrammed in Figure 2-103; keyboard address corelates are listed in Table 2-52. Refer to Figure 2-52 for the keyboard timing diagram.

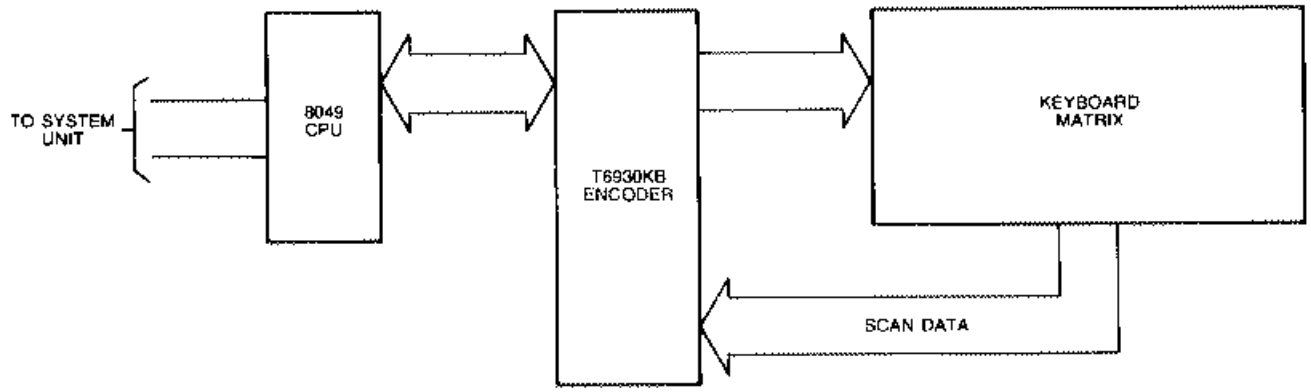


FIGURE 2-102. KEYBOARD BLOCK DIAGRAM

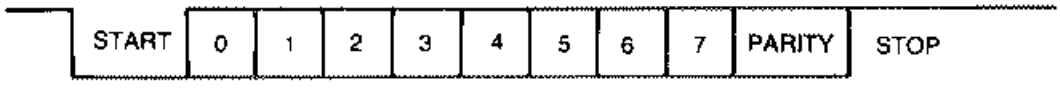


FIGURE 2-103. KEYBOARD DATA FORMAT

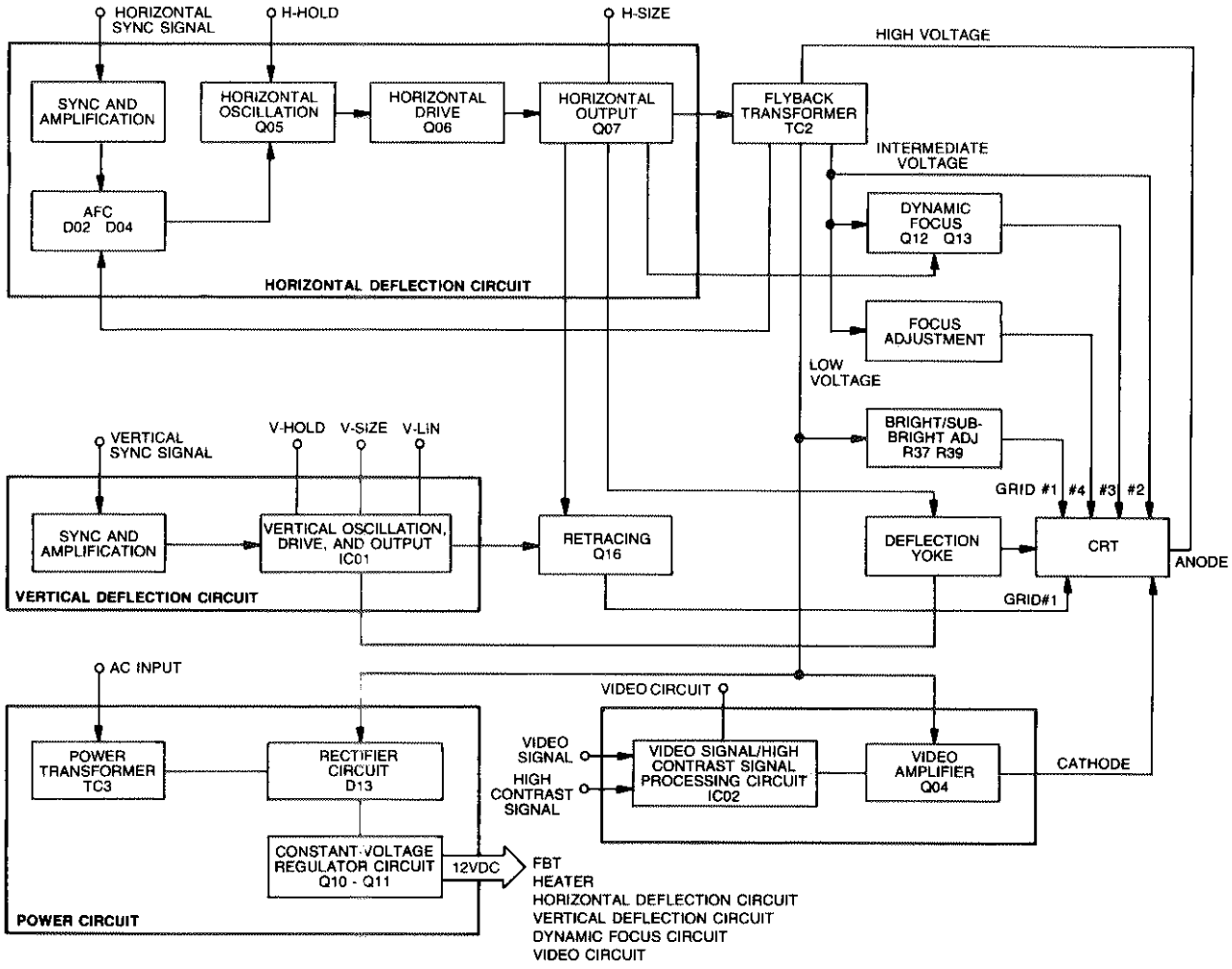
TABLE 2-52. KEY SCAN CODES

LOC	SYMBOL	DATA	LOC	SYMBOL	DATA	LOC	SYMBOL	DATA
F1	STOP	73H	F2	HELP	72H	F3	COPY DISK	71H
F4	UNDO	01H	F5	STORE	03H	F6	RETRIEVE	04H
F7	PRINT	05H	F8	INDEX	06H	F9	MAIL	07H
F10	MENU	09H	F11	EDIT	08H	F12	CALC	0AH
F13	SCHED	0BH	F14	DRAW	0CH	F15	BOLD	0EH
F16	ITALIC	0FH	F17	SIZE	1FH	F18	STYLE	1EH
E1	MAR REL	74H	E2	~	75H	E3	! 1	76H
E4	@ 2	61H	E5	# 3	62H	E6	$ 4	63H
E7	% 5	64H	E8	6	65H	E9	& 7	66H
E10	* 8	67H	E11	(9	68H	E12	) 0	69H
E13	_	6AH	E14	+ =	6BH	E15	|	6CH
E16	←	6DH	D1	← TAB →	77H	D2	Q	51H
D3	W	52H	D4	E	53H	D5	R	54H
D6	T	55H	D7	Y	56H	D8	U	57H
D9	I	55H	D10	O	59H	D11	P	5AH
D12	¼ ½	5BH	D13	[<	5CH	D14	>]	5DH
C1	TAB REL	41H	C2	SHIFT ALPHA	42H	C3	A	43H
C4	S	44H	C5	D	45H	C6	F	46H
C7	G	47H	C8	H	48H	C9	J	49H
C10	K	4AH	C11	L	4BH	C12	: ;	4CH
C13	" '	4DH	C14	RETURN	4EH	B1	TAB SET	78H
B2	(Lt) SHIFT*	87H,86H	B3	Z	33H	B4	X	34H
B5	C	35H	B6	V	36H	B7	B	37H
B8	N	38H	B9	M	39H	B10	, ,	3AH
B11	. .	3BH	B12	? /	4FH	B13	(Rt) SHIFT*	85H,84H
A1	CTRL	8BH,8AH	A2	(SP)	32H	A3	ALT	8DH,8CH
A4	CTRL	8FH,8EH	E17	⌫	6EH	E18	LINE	6FH
D15	INSERT [PRT SC]	5EH	D16	WORD [SCL LK]	5FH	C15	[PRIOR PAGE]	3CH
B14	– [–]	3DH	B15	→ [→]	3EH	A5	[NEXT PAGE]	3FH
E19	DEC TAB	2FH	E20	÷	2EH	E21	×	2DH
E22	+/–	1CH	D17	7	2BH	D18	8	2AH
D19	9	29H	D20	–	2CH	C16	4	1BH
C17	5	1AH	C18	6	19H	C19	+	28H
B16	1	27H	B17	2	26H	B18	3	25H
B19	ENTER =	15H	A6	0	17H	A7	.	16H

*In the ALT, CTRL,and SHIFT key rows. the first data is a MAKE code and the second is a BREAK code.

2.8 MONITOR OPERATION (Figure 2-104)

The model Q602 monitor is a monochrome, raster scan display with the internal circuitry diagrammed in Figure 2-104: a power supply circuit and flyback transformer; video sync and processor circuitry, vertical and horizontal deflection circuits; blanking; and dynamic focus. Timing diagrams for the CRT are included in Figures 2-109 through 2-111, at the end of the monitor section.



▲ FIGURE 2-104. MONOCHROME MONITOR BLOCK DIAGRAM

2.8.1 **Video Circuit** (Figure 2-105)

The video circuit consists of a video processing circuit and a video amplifier circuit.

In the video processing circuit, there are four possible signal combinations, described in Table 2-53, which determine the voltage level at point A in Figure 2-105. The four combinations produce two possible display modes: one in which the display contrast is variable and one in which maximum brightness is set.

On the video amplifier circuit board, transistor Q04 amplifies the signal according to the value at A. Resistor R10 is the load resistor for Q04; diode D01 protects Q04; and C03 is the capacitor for high-pass compensation.

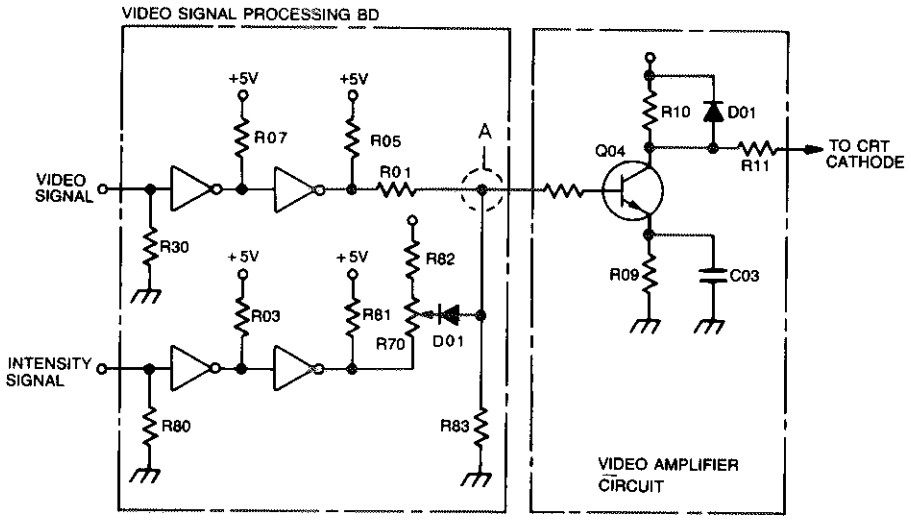


FIGURE 2-105. VIDEO/INTENSITY CIRCUIT

TABLE 2-53. VIDEO INTENSITY SIGNALS

STATUS	VIDEO SIGNAL	INTENSITY SIGNAL	EXPLANATION
1	0	0	Point A is low and there is no display.
2	0	1	Diode D01 causes point A to go low, and there is no display.
3	1	0	Point A is variable according to the position of the contrast potentiometer, R70.
4	1	1	When both the video and high contrast signals are high, the voltage is equal at both ends of R70 and point A goes high, resulting in a high intensity display.

2.8.2 Horizontal Deflection Circuit (Figure 2-106)

TTL horizontal sync signals are inverted twice, then amplified at IC02 and input to the AFC circuit via R12. Horizontal blanking pulses from the flyback transformer (T02) become sawtooth waves at R26 and C14, and are also input to the AFC circuit, passing through R20 before becoming AFC output. Horizontal oscillation is generated by the circuit including Q05, C12, C13, and L01; the inductance value of L01 changes with horizontal hold adjustment. Oscillation output passes through R25 to Q06, and combines with T01 to supply sufficient base voltage to switch horizontal output transistor Q07, controlling the horizontal deflection current flowing to the CRT yoke and supplying the blanking pulses required for high voltage generation at the FBT.

NOTE: *The horizontal width adjustment, L03, is connected in series with deflection yoke (DY) and is adjusted by moving its core.*

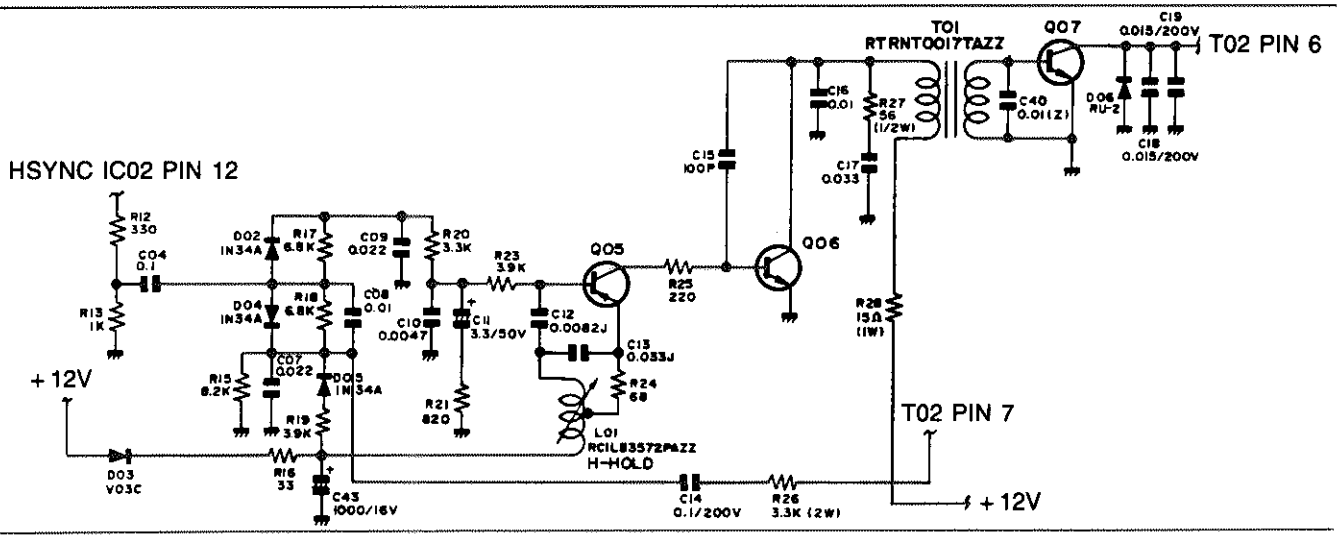


FIGURE 2-106. HORIZONTAL DEFLECTION CIRCUIT

2.8.3 Vertical Deflection Circuit (Figure 2-107)

TTL vertical sync signals are inverted twice, then amplified at Q01 and Q08 before being input to pin 5 of IC01, the vertical deflection IC. The internal circuitry of the IC is diagrammed below. When SYNC signals are input at pin 5, vertical oscillation begins and is input to the sawtooth wave block. Vertical hold is controlled at pin 6 of the oscillator block, and vertical size adjustment is controlled at pin 6 of the sawtooth wave block. The output signals are input to the amplifier before being received at the the deflection yoke at pin 1, generating a flow of deflection current.

NOTE: *Linearity correction is adjusted by R53 (the V LIN resistor) to control the extent of duplication of the sawtooth waves at pin 4.*

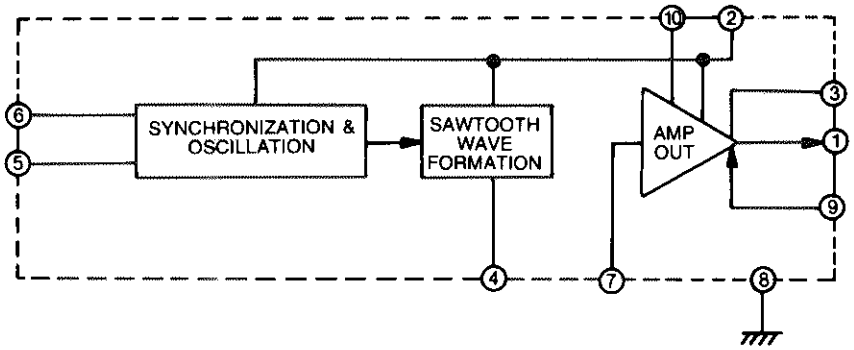


FIGURE 2-107. VERTICAL DEFLECTION CIRCUIT

2.8.4 Monitor Power Circuit (Figure 2-108)

The AC supply voltage is lowered at T03, then rectified at diode bridge D13, and 16VDC is output. At the constant voltage regulator circuit of Q10 and Q11, the voltage is converted to a 12VDC wave (with little ripple) which powers the FBT, CRT, heater, horizontal and vertical deflection circuits, dynamic focus, and video circuits.

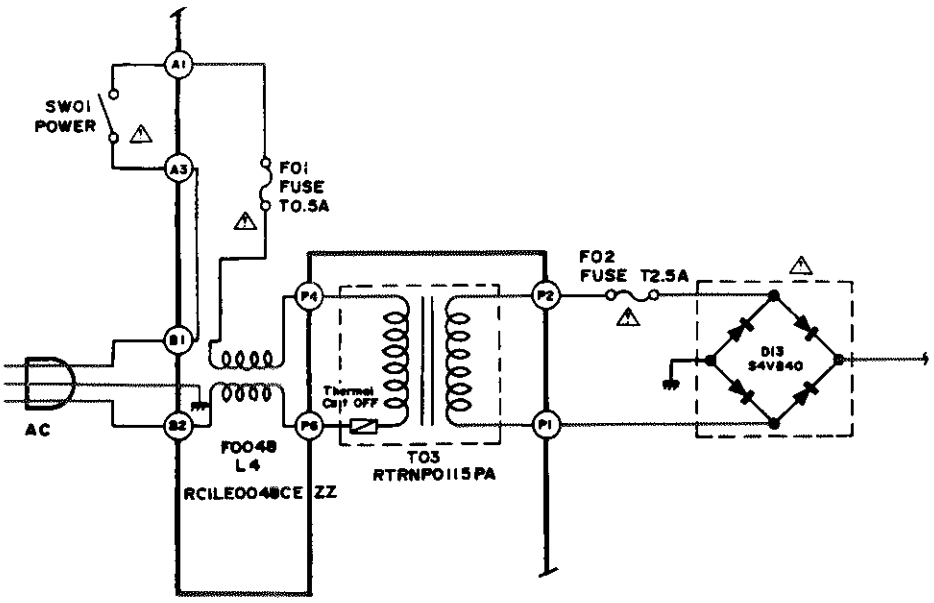


FIGURE 2-108. MONITOR POWER SUPPLY

2.8.5 Flyback Transformer (FBT)

The blanking pulse from the horizontal output transformer is input to the FBT and raised to approximately 13.5V, which is supplied to the CRT anode. A second tap of the transformer generates approximately 485VDC, which is supplied to CRT grid #3 via the FOCUS resistor and CRT grid #2. A voltage of 44VDC is supplied to the video, constant voltage regulator, and bright/sub-bright circuits from a third transformer tap.

2.8.6 Dynamic Focus Circuit

The dynamic focus circuit uses transistors Q12 and Q13 to create differing convergence points for beams applied to the center and edges of the CRT. A scatter-shaped waveform from the horizontal sync circuit is input to Q13, inverted, amplified, and supplied to CRT grid #4 to increase the voltage of signals applied to the screen edges.

2.8.7 Blanking Circuit

Horizontal and vertical blanking pulses are input to the base of Q16, inverted, amplified, then supplied to CRT grid #1. The voltage of grid #1 goes low between vertical and horizontal blanking pulses, darkening the screen and preventing viewing of the raster lines.

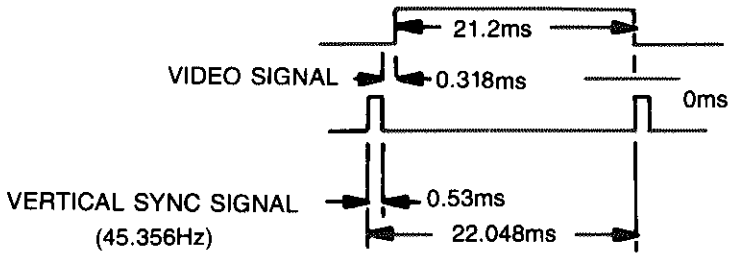


FIGURE 2-109. VERTICAL SYNC SIGNAL

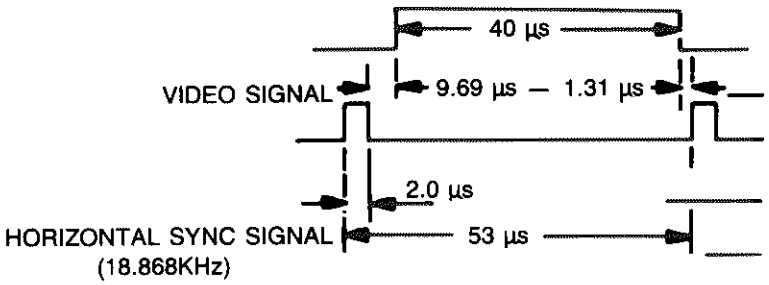


FIGURE 2-110. HORIZONTAL SYNC SIGNAL

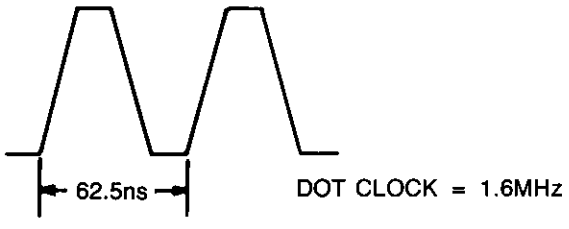


FIGURE 2-111. VIDEO SIGNAL