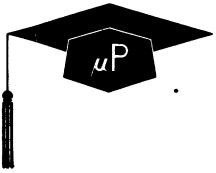


SSB-MPF

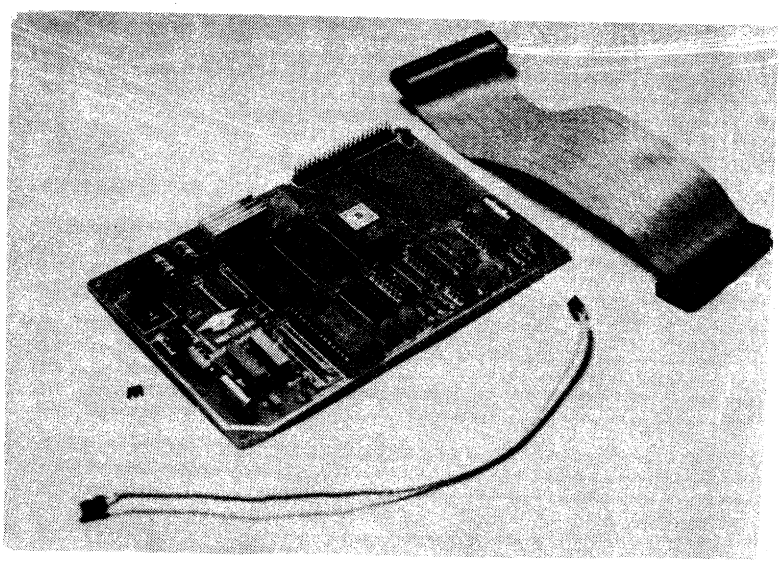
SPEECH SYNTHESIZER BOARD OPERATION MANUAL

TABLE OF CONTENTS

CONGRATULATIONS

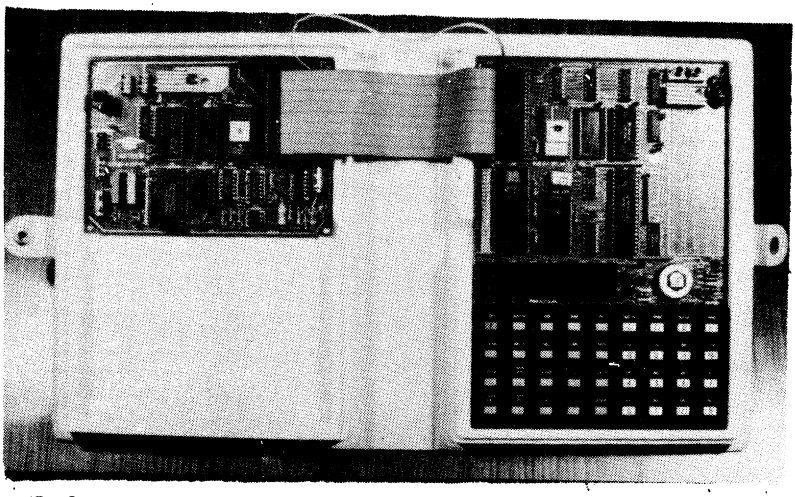
Your SSB-MPF will help you discover the mystery of speech synthesis. Unpacking your SSB-MPF package, you will find:

1) The SSB-MPF board, a complete speech synthesis system
2) Operation Manual
3) A 40-pin double-head female cable connector
4) An audio jumper wire
5) A two-pin male connector
6) A 9V, 200mA power adaptor



I . INTRODUCTION

SSB-MPF is a Speech Synthesizer Board especially designed to be used with MPF-I. It is a low-cost, programmable printed circuit board based on Texas Instruments' Voice Synthesis Processor TMS5200 or TMS5220. However, SSB-MPF itself is a complete speech synthesis system.



Before we go into details of our SSB-MPF, we would like to introduce briefly the principles on how speech synthesis system works and what is a speech synthesis system.

The diagram below shows a speech synthesis system. Varying air pressure of sound and voices, after being received by the microphone, is transformed into varying voltages and frequency. Varying electrical voltages frequencies are further converted through a converter to digital signals which afterwards go through the digital speech analyzer and a coding process, and are eventually stored in the Read Only Memory(ROM). To reproduce the sound signals stored in the ROM, the data in the ROM should go through a decoding process, a digital speech synthesizer before being converted into analog electrical voltages and frequencies which activate a speaker.

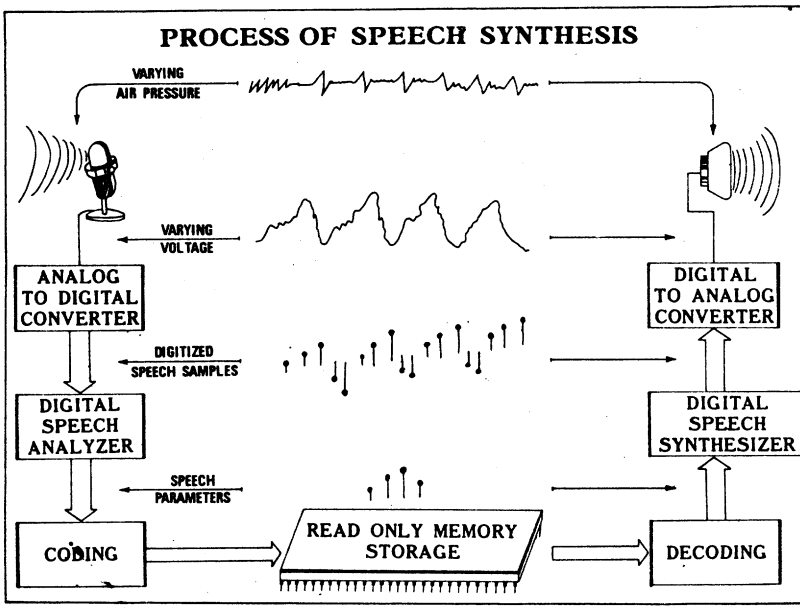


Figure 1-1 Process of Speech Synthesis

In short, a speech synthesis board is a printed circuit board which can reproduce different voices and sounds. The Multitech SSB-MPF is a typical speech synthesis board with these functions.

Users can easily operate the SSB-MPF after connecting the SSB-MPF to MPF-I with a flat 40-pin female double-head cable.

The technology of speech synthesis, first commercially introduced by TI for use on automobile gadgetry, has been used for applications on modern daily life for some time. The Multetich SSB-MPF speech board will lead you discover the interesting and mysterious world of "speaking" boards at the lowest possible cost.

II. FEATURES

The most outstanding feature of SSB-MPF is that it is a basic as well as complete speech synthesis system. Therefore, a beginner can use the system with ease to understand every aspect about speech synthesis systems. Yet, the simplicity in design of the SSB-MPF makes the machine highly reliable and cost-efficient. The major features of the SSB-MPF are as follows:

A. Structure: (See Figure 2-1)

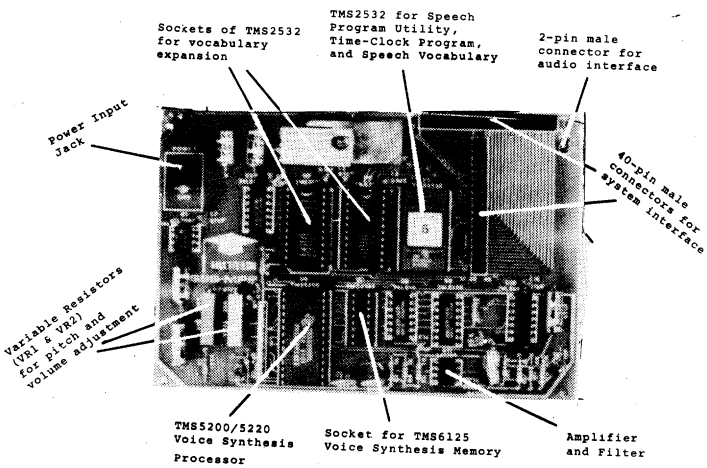
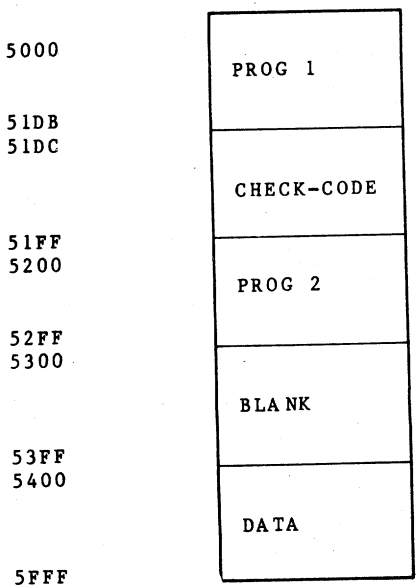


Figure 2-1

B. System Control Unit
   1) TI's TMS5200 or TMS5220 Voice Synthesis Processor is the speech synthesizer of the speech synthesis system.
   2) The host controller of the system (SSB-MPF) is the Z-80 CPU on MPF-I.

C. Memory: featuring strong vocabulary expansion ability.
   1) The memory chip TMS2532 on the board is used to store speech data and utility programs for demonstration purpose.



PROG 1 : Time-clock program
CHECK-CODE: For self-test purpose. Press Key (ADDR) 51DC and Key (GO), you will hear the system "speak" all the vocabulary stored in it.
PROG 2 : Speech program utility
BLANK : Storage area for users' data or program
DATA : Speech vocabulary

2) The two sockets, U3 and U4, are reserved for two optional memory chips of TMS2532 to expand SSB-MPF vocabulary.
3) A socket (U7) is reserved for TMS6125, the 32K bits ROM, which functions as the advanced Voice Synthesis Memory (VSM) for storing speech data.

D. System input/output devices:
   1) The data input device of the speech synthesis system is the keyboard of the MPF-I.
   2) The data output devices of the system are the speaker and a six-digit display panel above the keyboard.
   3) An external speaker can be connected to the SSB-MPF with audio jumper wire, Jumper 2.

E. System power supply: It only needs 5V, 200mA to operate.

F. System interface: Two 40-pin male double-head cable connectors are used for any possible external connection such as interfacing with MPF-I or with our EPB-MPF (EPROM Programmer Board).

Ⅲ. *FUNCTIONAL DESCRIPTION*

The major functional units of the SSB-MPF are shown in figure 3-1 and described below:

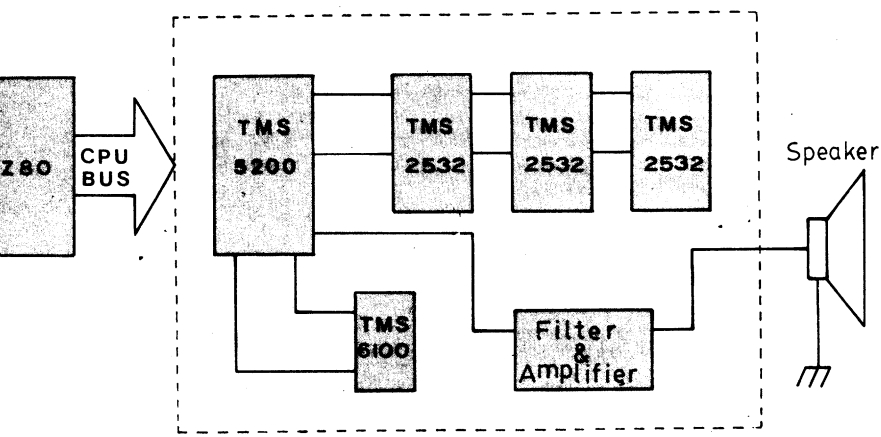


Figure 3-1 Block Diagram of SSB-MPF

1) Voice Synthesis Processor:

a) TI's solid state speech chip (TMS5200 or TMS5220) is used as VSP of the unit. It can fetch speech data and programs stored in memory chips such as TMS2532, and reproduce or synthesize human voice through filter/amplifier and speaker.

b) The TMS5200 or TMS5220 VSP operates on Linear Predictive Coding (LPC) method, which converts analog speech data to digital data that are suitable for processing by VSP. The TMS5200 can access LPC-encoded data stored in memory and convert the data into sound signal of specific pitch and amplitude.

2) Speech Data EPROM: The maximum memory capacity of the system can be expanded to 12K bytes by adding two more additional TMS2532 memory chips to the system. The speech data is encoded in LPC which provides a speech quality comparable to that of voices generated by Pulse-Coded Modulation (PCM) system. Furthermore, it only takes 1200 bits to memorize the speech data that is produced in one second in the LPC system. In the PCM system, it takes 64,000 bits to memorize the speech data that is produced in one second.

3) System Z-80 Controller: The Z-80 CPU on the MPF-I is used as speech synthesis system controller. It accepts the commands from MPF-I keyboard and fetches the speech programs.

4) Filter: A low-pass filter is used to generate smooth and clear speech signal.

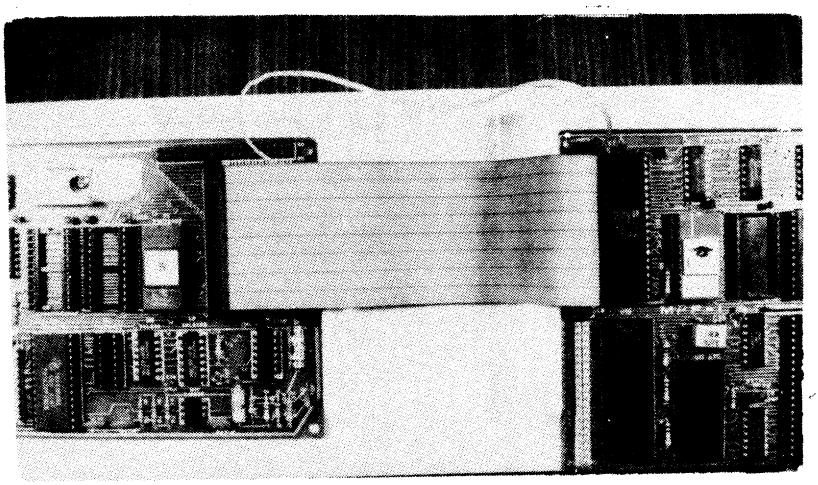
5) Amplifier: An audio amplifier is used to drive the 8 Ohm speaker.

Ⅳ. *INSTALLATION PROCEDURES*

1) Make sure that the SSB-MPF and MPF-I are not plugged to electricity power sources before connecting the SSB-MPF and MPF-I.

2) Connect the SSB-MPF to MPF-I with a 40-pin female double-head cable connector.

3) Connection of the speech synthesis system with audio data output devices should be done in the following steps:
   A. If the system is to use the speaker of the MPF-I: Scratch out the printed circuit of Jumper 2 at the back of the MPF-I, and then plug the jumper wire of the system. Both ends of the jumper wire are fitted with a two-pin female double-head plastic socket. Plug one end of the jumper wire to the two pins in the upper right corner of the SSB-MPF and the other end to the two pins marked with Jumper 2 in the upper left corner of the MPF-I.



B. If the system is to use an external speaker: Connect the audio jumper wire of SSB-MPF to the external speaker.

4) Connect the SSB-MPF and MPF-I to power sources:
   A. An adaptor (9V, 600mA, Output) is plugged to the power socket in the upper right corner of MPF-I.
   B. An adaptor (9V, 200mA, Output) is, then, plugged to the power socket in the upper left corner of the SSB-MPF.
   Note: The power source for the SSB-MPF can ONLY be connected after the power source for MPF-I has been connected.

Now, we have completed the installation procedures, and will proceed to test our speech synthesis system, SSB-MPF.

V. OPERATION PROCEDURES

Once your SSB-MPF have been interfaced, the system is ready for test run. To test run the system, our Time-clock Program is used for you to familiarize with the operations of the system. The running of our Time-clock Program is as easy as adjusting the time of a digital watch.

Before running the Time-clock Program on the system, you have to set the time of the system to the current time. After you have keyed in the time, press key (ADDR) 5000 and key (GO). The system will start displaying time on its six-digit display panel, and it will announce the time in English in an interval of one minute. For example, if the display panel of the system shows 09:21:58, the system will announce in English "Nine, twenty-two" after two seconds, while the display panel showing 09:22:00. A full sentence --"It is X o'clock AM (or PM)"--will be heard each hour as long as the Time-clock Program is kept on.

If the current time is 9:53 a.m., the steps you have to follow in executing the Time-clock Program are as follows:

Step 1: Set SECOND: (ADDR) 1A00 (DATA) 00
Step 2: Set MINUTE: (ADDR) 1A01 (DATA) 53
Step 3: Set HOUR: (ADDR) 1A02 (DATA) 09
Step 4: Set (AM/PM): (ADDR) 1A11 (DATA) 00
Step 5: Press Key (ADDR) 5000 and Key (GO) for program execution

Note: We use bit 0 of memory chip address 1A11 for AM/PM. If bit 0 is 0, it indicates AM; otherwise, it indicates PM.

You will be amazed at how the system works. If it doesn't work, please check if the SSB-MPF is operated correctly and try again.

Ⅵ. *VOICE VOLUME AND PITCH ADJUSTMENT*

Sound reproduced by the system can be easily adjusted for desirable effects.

A. the Adjustment of VR-1:

1) To lower the voice pitch, turn the adjusting screw of VR-1 (variable resistor-1) clockwise.

2) To increase the voice pitch, turn the adjusting screw of VR-1 counterclockwise. This may require more than one or two turns, depending on the efficiency of the speaker used.

B. The Adjustment of VR-2:

1) To lower the voice volume, turn the adjusting screw of VR-2 clockwise.

2) To increase the voice volume, turn the adjusting screw of VR-2 counterclockwise.

This also may require more than one or two turns, depending on the efficiency of the speaker used.

Ⅶ. SPECIFICATIONS

1) Power Requirement: +5V, ±5%, 200mA

2) Connector : D-Connector double-head 40 holes

3) Size : Width - 10.9 cm
Length - 15.8 cm

4) Environment : Operating temperature 0°C to 40°C
Storage temperature 125°C to 80°C
Relative Humidity
Noncondensing up to 90%

Ⅷ. *APPENDICES*

I. SCHEMATIC

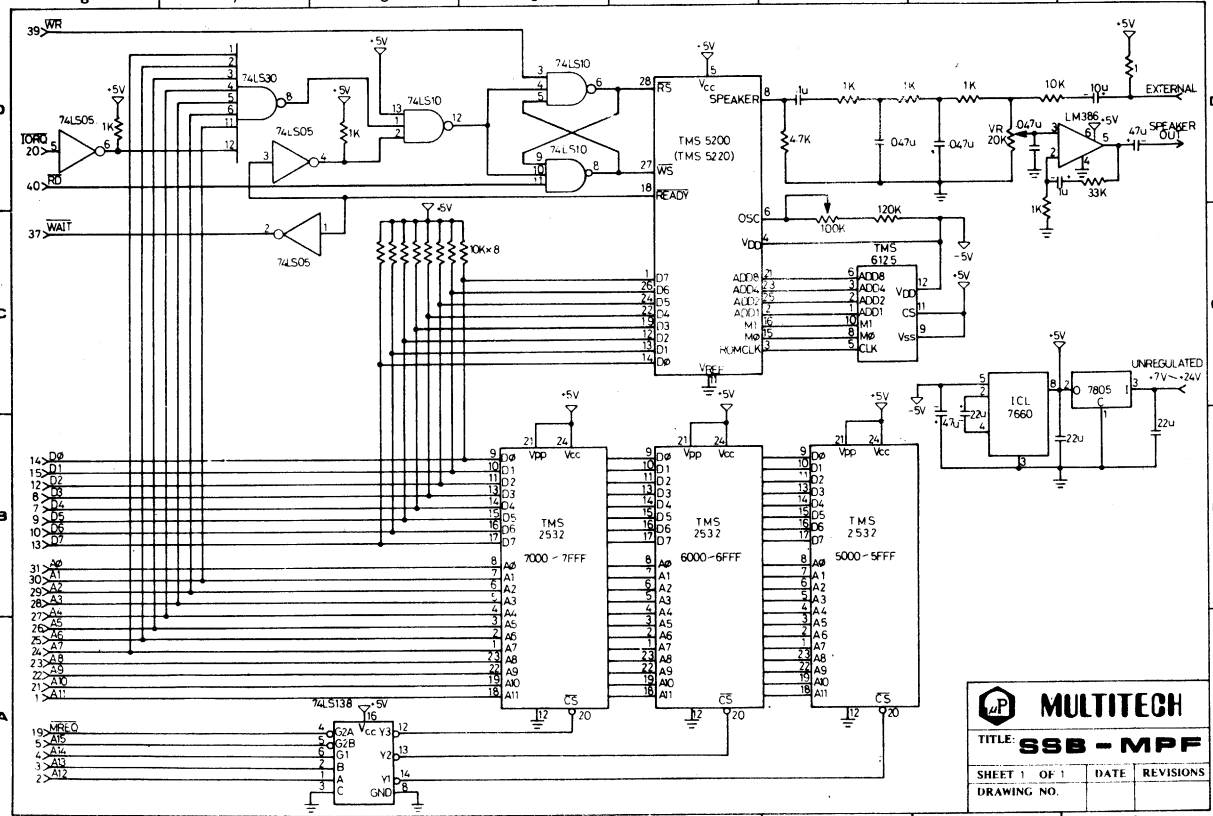
1) Standard vocabulary: A memory chip, TMS2532, with standard vocabulary is installed in the system which is a standard memory device.

2) Optional Vocabulary:

   a) A total of eight optional EPROM memory chips available in eight standard packages is offered by Multitech.

   b) The optional memory chips are offered for your vocabulary expansion.

   c) You can acquire these optional memory chips from local Multitech distributors.


WR
IORQ
RD
WAIT
74LS05
74LS30
74LS10
TMS 5200
(TMS 5220)
RS
WS
READY
SPEAKER
EXTERNAL
SPEAKER OUT
LM386
OSC
VDD
TMS 6125
ADD8
ADD4
ADD2
ADD1
M1
MØ
CLK
HUMCLK
10K×8
TMS 2532
7000 - 7FFF
6000 - 6FFF
5000 - 5FFF
74LS138
MREQ
ICL 7660
7805
UNREGULATED
+7V ~ +24V
MULTITECH
SSB - MPF
SHEET 1 OF 1
DRAWING NO.
DATE
REVISIONS

2. TIME-CLOCK PROGRAM

```
                        1  ;
                        2  ;       **********************************
                        3  ;       *   SSB-MPF   CLOCK_ENGLISH.S    *
                        4  ;       **********************************
                        5  ;
                        6  ;COPYRIGHT, MULTITECH INDUSTRIAL CORP. 1982.
                        7  ;Written by Yung Jui Chen, R&D department.
                        8  ;Routine address is 5000H
                        9  ;Demo program of SSB-MPF. Talking clock in English.
                       10  ;This program is to tell you the current time.
                       11  ;Before you run this program, set the time buffer
                       12  ;including SECOND, MINUTE, HOUR, and AM PM flag.
                       13  ;For example:      buffer adds        time indicate
                       14  ;         SECOND       1A00H              58
                       15  ;         MINUTE       1A01H              55
                       16  ;         HOUR         1A02H              10
                       17  ;         AM/PM        1A11H              BIT0 *
                       18  ;If bit 0 is 0 then AM, otherwise is PM.
                       19  ;
                       20  SCAN1    EQU     0624H    ;Utility Subroutine of MPF-1
                       21  PORT     EQU     0FEH     ;I/O port of SSB-MPF
                       22  HEX7SG   EQU     066DH    ;Utility Subroutine of MPF-1
5000                   23           ORG     5000H
5000   F3              24           DI               ;Disable interrypt,which affects
                       25                            ;timing
5001   DD21031A R      26           LD      IX,OUTBF
                       27  ;
                       28  ;ONESEC loop takes one second to execute,include
                       29  ;three Subroutine and one delay loop2 for addition
                       30  ;process.
                       31  ;
5005   0664            32  ONESEC   LD      B,100
5007   CD2406          33  LOOP1    CALL    SCAN1    ;SCAN1  total execution time
                       34                            ;is about 9.95 ms
500A   10FB            35           DJNZ    LOOP1
500C   CD1750   R      36           CALL    TMUPDT
500F   CD3651   R      37           CALL    BFUPDT
                       38  ;
                       39  ;LOOP2 is used as addition delay.
                       40  ;
5012   00              41  LOOP2    NOP
5013   10FD            42           DJNZ    LOOP2
5015   18EE            43           JR      ONESEC
                       44  ;
                       45  ;TMUPDT is time-buffer updata
                       46  ;routine.
                       47  ;
5017   218751   R      48  TMUPDT   LD      HL,MAXTAB
501A   11001A   R      49           LD      DE,SEC
501D   0603            50           LD      B,3
501F   37              51           SCF                          ;set carry flag, to
                       52                                        ;force add 1
                       53  ;
                       54  ;TMINC compare with data in MAX-TABLE if result
                       55  ;is less than the following loop is null.
                       56  ;
5020   1A              57  TMINC    LD      A,(DE)
5021   CE00            58           ADC     A,0
```

```
5023  27            59          DAA
5024  12            60          LD      (DE),A
5025  96            61          SUB     (HL)            ;compare with max_table
5026  3801          62          JR      C,COMPL
5028  12            63          LD      (DE),A
                    64  COMPL
5029  3F            65          CCF                     ;complement carry flag
502A  23            66          INC     HL
502B  13            67          INC     DE
502C  10F2          68          DJNZ    TMINC
502E  3A021A    R   69          LD      A,(HOUR)
5031  A7            70          AND     A
5032  200C          71          JR      NZ,CONT         ;if reach max force
                    72                                  ;add 1
                    73                                  ;if not reach count
                    74                                  ;continue
5034  3C            75          INC     A
5035  32021A    R   76          LD      (HOUR),A
5038  3A111A    R   77          LD      A,(APMFLG)
503B  EE01          78          XOR     01H
503D  32111A    R   79          LD      (APMFLG),A
5040  3A001A    R   80  CONT    LD      A,(SEC)         ;One minute is up ?
5043  A7            81          AND     A
5044  CC4850    R   82          CALL    Z,SPEAK
5047  C9            83          RET
                    84  ;
                    85  ;SPEAK routine is executed when every minute
                    86  ;is reach. It include many subroutines as the
                    87  ;following:
                    88  ;           1. APMDEC- AM or PM decision
                    89  ;           2. CHANGE- AM or PM status
                    90  ;                      exchange each other
                    91  ;           3. CHKOCK- check the o'clock
                    92  ;                      time
                    93  ;           4. SETPM - set PM flag
                    94  ;           5. SPKPM - speak PM and save
                    95  ;                      the speech address
                    96  ;           6. GO*   - tell time routine
                    97  ;           7. CNTMIN- check and count the
                    98  ;                      updated time
                    99  ;
                   100  ;
5048  08           101  SPEAK   EX      AF,AF'
5049  D9           102          EXX
504A  3E02         103          LD      A,2
504C  32001A    R  104          LD      (SEC),A         ;compensate timing
                   105                                  ;lose during the
                   106                                  ;speech routine
504F  218A51    R  107          LD      HL,HOUR_MIN
5052  3A021A    R  108          LD      A,(HOUR)
5055  87           109          ADD     A,A
5056  5F           110          LD      E,A
5057  1600         111          LD      D,0
5059  19           112          ADD     HL,DE
505A  22091A    R  113          LD      (TLKHOR1),HL
                   114  APMDEC                          ;this routine decide AM
                   115                                  ;or PM
505D  3A111A    R  116          LD      A,(APMFLG)      ;define bit0=0,AM
```

```
LOC   OBJ CODE  M STMT SOURCE STATEMENT
                  117                                   ;       bit0=1,PM
5060  CB47        118         BIT     0,A
5062  200B        119         JR      NZ,SETPM          ;set PM
5064  21D451    R 120         LD      HL,AM_
5067  E5          121         PUSH    HL
5068  FD21D551  R 122         LD      IY,PM_
506C  C37750    R 123         JP      CHANGE            ;change AM to PM
                  124                                   ;or PM to AM
506F  21D551    R 125 SETPM   LD      HL,PM_
5072  E5          126         PUSH    HL
5073  FD21D451  R 127         LD      IY,AM_
5077  FDE3        128 CHANGE  EX      (SP),IY
5079  E1          129         POP     HL
507A  FD7E00      130         LD      A,(IY)
507D  CB47        131         BIT     0,A
507F  2009        132         JR      NZ,SPKPM          ;PM is speaking
5081  2ACE51    R 133         LD      HL,(AMADDS)
5084  220F1A    R 134         LD      (APMTLK),HL       ;APMTLK choice talk
                  135                                   ;AM or PM
5087  C39050    R 136         JP      CHKOCK
508A  2AD051    R 137 SPKPM   LD      HL,(PMADDS)
508D  220F1A    R 138         LD      (APMTLK),HL
5090  3A011A    R 139 CHKOCK  LD      A,(MIN)           ;check the o'clock
5093  FE00        140         CP      0                 ;time
5095  2021        141         JR      NZ,CNTMIN         ;if minute is not
                  142                                   ;zero check the
                  143                                   ;actual minute no.
                  144 ;
                  145 ;GO routine is to tell o•clock time
                  146 ;include AM,PM
                  147 ;GO* routine save all the update time
                  148 ;HOUR and MINUTE. Speech routine is
                  149 ;called now.
                  150 ;
                  151 GO
5097  21CA51    R 152         LD      HL,IT
509A  CD4E51    R 153         CALL    START             ;speak "it"
509D  21CC51    R 154         LD      HL,IS
50A0  CD4E51    R 155         CALL    START             ;speak "is"
50A3  2A091A    R 156         LD      HL,(TLKHOR1)
50A6  CD4E51    R 157         CALL    START
50A9  21D251    R 158         LD      HL,JUST
50AC  CD4E51    R 159         CALL    START             ;speak "o•clock"
50AF  210F1A    R 160         LD      HL,APMTLK
50B2  CD4E51    R 161         CALL    START             ;speak AM or PM
50B5  D9        162         EXX
50B6  08        163         EX      AF,AF'
50B7  C9        164         RET
                  165
                  166 ;
                  167 ;CNTMIN routine to count the updata minutes
                  168 ;for the GO routine to tell actual time reach
                  169 ;including hour and minutes.
                  170 ;
50B8  3A011A    R 171 CNTMIN  LD      A,(MIN)
50BB  FE10        172         CP      10H
50BD  3839        173         JR      C,CNTMN2
50BF  FE20        174         CP      20H
```

```
LOC   OBJ CODE  M STMT SOURCE STATEMENT

50C1  3858        175            JR      C,CNTMN1
50C3  3A011A    R 176  CNTMN3    LD      A,(MIN)
50C6  E60F        177            AND     0FH
50C8  218A51    R 178            LD      HL,HOUR_MIN
50CB  87          179            ADD     A,A
50CC  85          180            ADD     A,L
50CD  6F          181            LD      L,A
50CE  220D1A    R 182            LD      (TKMIN2),HL
50D1  3A011A    R 183            LD      A,(MIN)
50D4  0F          184            RRCA
50D5  0F          185            RRCA
50D6  0F          186            RRCA
50D7  0F          187            RRCA
50D8  E60F        188            AND     0FH
50DA  21BE51    R 189            LD      HL,TXBLE_MIN
50DD  87          190            ADD     A,A
50DE  85          191            ADD     A,L
50DF  6F          192            LD      L,A
50E0  220B1A    R 193            LD      (TLKMIN1),HL
                  194  ;
                  195  ;GO3 routine is to tell minute time
                  196  ;above 20.
                  197  ;
50E3  2A0B1A    R 198  GO3       LD      HL,(TLKHOR1)
50E6  CD4E51    R 199            CALL    START
50E9  2A0B1A    R 200            LD      HL,(TLKMIN1)
50EC  CD4E51    R 201            CALL    START
50EF  2A0D1A    R 202            LD      HL,(TKMIN2)
50F2  CD4E51    R 203            CALL    START
50F5  D9          204            EXX
50F6  08          205            EX      AF,AF'
50F7  C9          206            RET
50F8  3A011A    R 207  CNTMN2    LD      A,(MIN)
50FB  E60F        208            AND     0FH
50FD  218A51    R 209            LD      HL,HOUR_MIN
5100  87          210            ADD     A,A
5101  85          211            ADD     A,L
5102  6F          212            LD      L,A
5103  220D1A    R 213            LD      (TKMIN2),HL
                  214  ;
                  215  ;GO2 routine is to tell time
                  216  ;range from 01 to 09 minutes.
                  217  ;
5106  2A091A    R 218  GO2       LD      HL,(TLKHOR1)
5109  CD4E51    R 219            CALL    START           ;speak HOUR
510C  21D651    R 220            LD      HL,OH           ;speak word "OH"
510F  CD4E51    R 221            CALL    START
5112  2A0D1A    R 222            LD      HL,(TKMIN2)
5115  CD4E51    R 223            CALL    START           ;speak minute
5118  D9          224            EXX
5119  08          225            EX      AF,AF'
511A  C9          226            RET
511B  3A011A    R 227  CNTMN1    LD      A,(MIN)
511E  218A51    R 228            LD      HL,HOUR_MIN
5121  87          229            ADD     A,A
5122  85          230            ADD     A,L
5123  6F          231            LD      L,A
5124  220D1A    R 232            LD      (TKMIN2),HL
```

```
                    233  ;
                    234  ;GO1 routine is to tell minute time
                    235  ;range between 10 to 19.
                    236  ;
5127  2A091A    R   237  GO1       LD      HL,(TLKHOR1)
512A  CD4E51    R   238            CALL    START
512D  2A0D1A    R   239            LD      HL,(TKMIN2)
5130  CD4E51    R   240            CALL    START
5133  D9          241            EXX
5134  08          242            EX      AF,AF'
5135  C9          243            RET
                    244  ;
                    245  ;BUFPDT--- display time buffer is updataed here
                    246  ;It takes 914 cycles.
                    247  ;
5136  21031A    R   248  BFUPDT   LD      HL,OUTBF
5139  11001A    R   249            LD      DE,SEC
513C  0603        250            LD      B,3
513E  1A          251  PUTBF     LD      A,(DE)
513F  CD6D06      252            CALL    HEX7SG
5142  13          253            INC     DE
5143  10F9        254            DJNZ    PUTBF
5145  2B          255            DEC     HL
5146  2B          256            DEC     HL
5147  CBF6        257            SET     6,(HL)          ;set decimal point of
                    258                                    ;hour
5149  2B          259            DEC     HL
514A  2B          260            DEC     HL
514B  CBF6        261            SET     6,(HL)          ;set decimal point of
                    262                                    ;minute
514D  C9          263            RET                     ;return when B=0
                    264  ;
                    265  ;START is speech routine of TMS 5200
                    266  ;
514E  4E          267  START:    LD      C,(HL)
514F  23          268            INC     HL
5150  46          269            LD      B,(HL)
5151  C5          270            PUSH    BC
5152  E1          271            POP     HL
5153  0610        272            LD      B,10H
5155  3EFF        273  RESET     LD      A,0FFH          ;reset TMS 5200
5157  D3FE        274            OUT     (PORT),A
5159  CD8051    R 275            CALL    DELY
515C  10F7        276            DJNZ    RESET
515E  3E60        277            LD      A,60H           ;activate TMS 5200
5160  D3FE        278            OUT     (PORT),A
5162  CD8051    R 279            CALL    DELY
5165  7E          280  SEND1    LD      A,(HL)          ;send the speech data
5166  D3FE        281            OUT     (PORT),A
5168  CD8051    R 282            CALL    DELY
516B  23          283            INC     HL
516C  DBFE        284            IN      A,(PORT)
516E  CB7F        285            BIT     7,A             ;check the status of
                    286                                    ;TMS 5200
5170  28F3        287            JR      Z,SEND1
5172  7E          288  SEND2    LD      A,(HL)
5173  D3FE        289            OUT     (PORT),A        ;continue to send
                    290                                    ;speech data
```

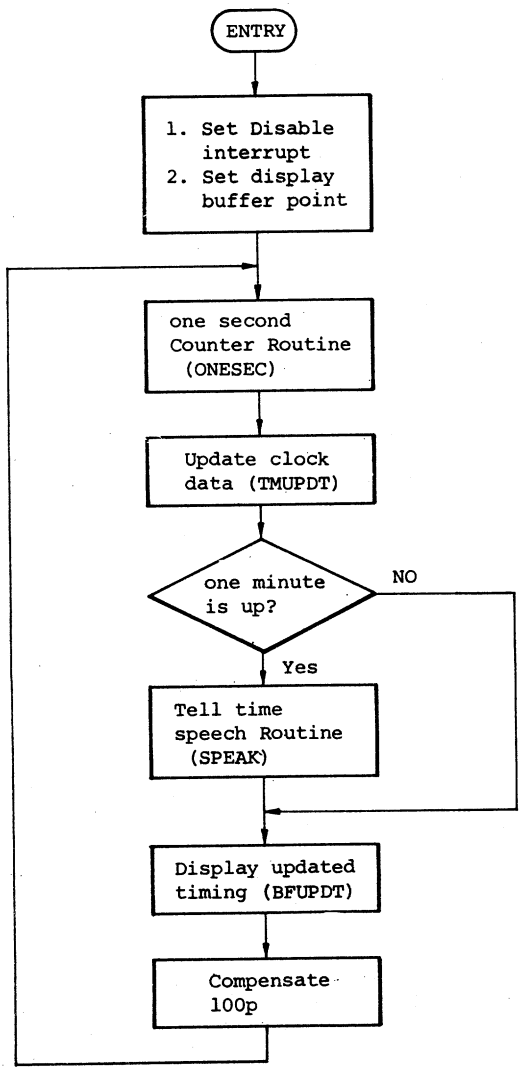
```
LOC   OBJ CODE M STMT SOURCE STATEMENT

5175  CD8051   R  291          CALL    DELY
5178  23          292          INC     HL
5179  DBFE        293          IN      A,(PORT)
517B  CB7F        294          BIT     7,A
517D  20F3        295          JR      NZ,SEND2
517F  C9          296          RET
5180  C5          297  DELY    PUSH    BC              ;delay loop for
                  298                                  ;speech routine.
5181  06FF        299          LD      B,0FFH
5183  10FE        300          DJNZ    $
5185  C1          301          POP     BC
5186  C9          302          RET
                  303
                  304
                  305
5187  60          306  MAXTAB  DEFB    60H
5188  60          307          DEFB    60H
5189  13          308          DEFB    13H
                  309  HOUR_MIN                       ;table used in both
                  310                                 ;HOUR and MINUTE
518A  B05F        311          DEFW    5FB0H          ;PAUSE
518C  0054        312          DEFW    5400H          ;ONE
518E  5854        313          DEFW    5458H          ;TWO
5190  E856        314          DEFW    56E8H          ;THREE
5192  9854        315          DEFW    5498H          ;FOUR
5194  2855        316          DEFW    5528H          ;FIVE
5196  E854        317          DEFW    54E8H          ;SIX
5198  A055        318          DEFW    55A0H          ;SEVEN
519A  F055        319          DEFW    55F0H          ;EIGHT
519C  2056        320          DEFW    5620H          ;NINE
519E  B85F        321          DEFW    5FB8H          ;NULL (A)
51A0  B85F        322          DEFW    5FB8H          ;NULL (B)
51A2  B85F        323          DEFW    5FB8H          ;NULL (C)
51A4  B85F        324          DEFW    5FB8H          ;NULL (D)
51A6  B85F        325          DEFW    5FB8H          ;NULL (E)
51A8  B85F        326          DEFW    5FB8H          ;NULL (F)
51AA  A056        327          DEFW    56A0H          ;TEN
51AC  B858        328          DEFW    58B8H          ;ELEVEN
51AE  6858        329          DEFW    5868H          ;TWELVE
51B0  3857        330          DEFW    5738H          ;THIRTEEN
51B2  1859        331          DEFW    5918H          ;FOURTEEN
51B4  B859        332          DEFW    59B8H          ;FIFTEEN
51B6  205C        333          DEFW    5C20H          ;SIXTEEN
51B8  885B        334          DEFW    5B88H          ;SEVENTEEN
51BA  205B        335          DEFW    5B20H          ;EIGHTEEN
51BC  A85A        336          DEFW    5AA8H          ;NINETEEN
                  337  TXBLE_MIN
51BE  B85F        338          DEFW    5FB8H          ;NULL
51C0  A056        339          DEFW    56A0H          ;TEN
51C2  1058        340          DEFW    5810H          ;TWENTY
51C4  D057        341          DEFW    57D0H          ;THIRTY
51C6  185A        342          DEFW    5A18H          ;FORTY
51C8  605A        343          DEFW    5A60H          ;FIFTY
                  344  IT                             ;word "it" address
51CA  105E        345          DEFW    5E10H
                  346  IS                             ;word "is" address
51CC  485E        347          DEFW    5E48H
                  348
```

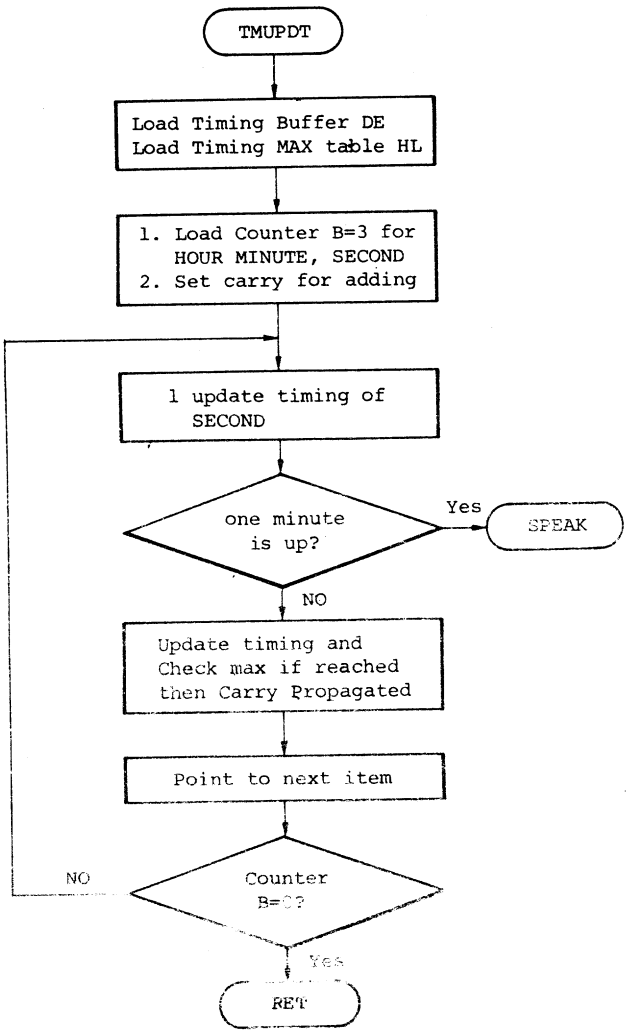
```
LOC   OBJ CODE M STMT SOURCE STATEMENT

                  349 AMADDS
51CE  A85C        350         DEFW    5CA8H   ;AM data address
                  351 PMADDS
51D0  F85C        352         DEFW    5CF8H   ;PM data address
                  353 JUST
51D2  605D        354         DEFW    5D60H   ;o'clock data
                  355 AM_
51D4  00          356         DEFB    0
                  357 PM_
51D5  01          358         DEFB    1
                  359 OH
51D6  E05D        360         DEFW    5DE0H   ;speech data "OH"
                  361 ;
                  362 ;RAM Buffer starting address
                  363 ;
1A00              364         ORG     1A00H
                  365 TMBF                    ;Time Buffer for HOUR,
                  366                         ;MINUTE and SECOND.
1A00              367 SEC     DEFS    1
1A01              368 MIN     DEFS    1
1A02              369 HOUR    DEFS    1
1A03              370 OUTBF   DEFS    6
1A09              371 TLKHOR1 DEFS    2
1A0B              372 TLKMIN1 DEFS    2
1A0D              373 TKMIN2  DEFS    2
1A0F              374 APMTLK  DEFS    2
1A11              375 APMFLG  DEFS    1
                  376         END
```

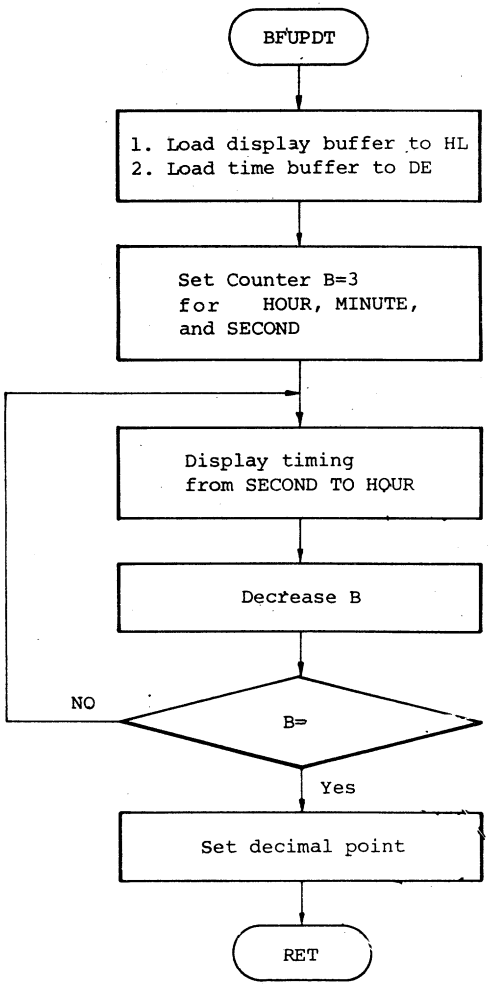
CLOCK-ENGLISH.S
Flowchart



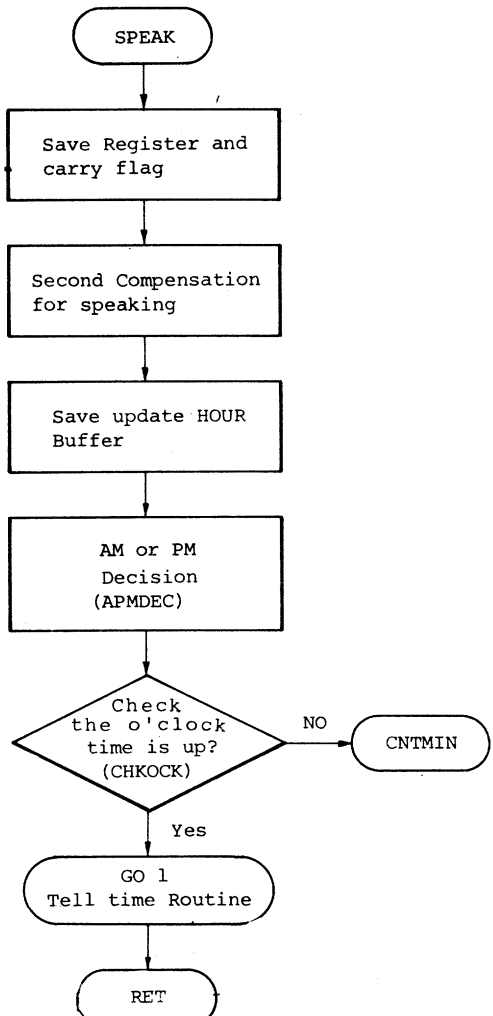
Time Buffer Update
Flowchart



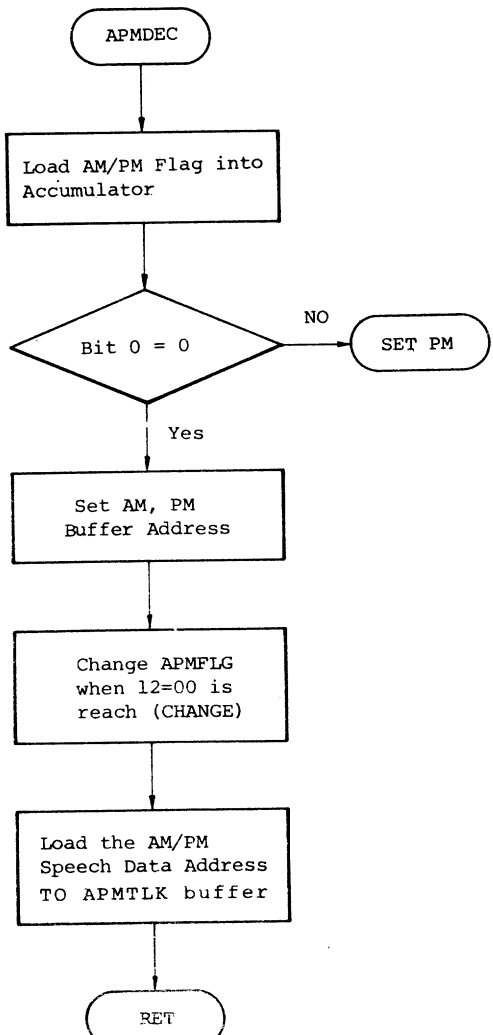
Update Display Buffer
Flowchart



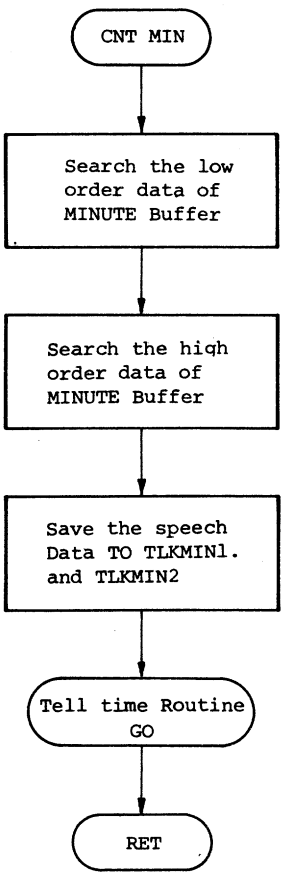
Speech Routine
Flowchart



AM. PM. Decision
Flowchart

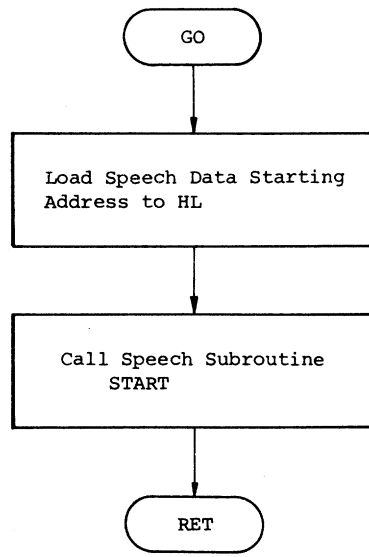


Count MINUTE Buffer
Flowchart



Tell Time Routine
Flowchart

GO & GO1



SUBROUTINE START is the same as DEMO-SUBROUTINE.S

3. TMS5200 VOICE SYNTHESIS PROCESSOR

DATA MANUAL

TABLE OF CONTENTS

APPENDICES

LIST OF ILLUSTRATIONS

LIST OF TABLES

1. INTRODUCTION

1.1 SCOPE

This manual describes in detail the functional characteristics of a linear predictive coding (LPC) speech synthesis device, the TMS 5200. In addition to this document, the user may wish to refer to the TMS 6100 128K bit ROM electrical specification.

1.2 KEY FEATURES

- High-quality voice communication from a microcomputer system
- Low-data-rate LPC encoding
- Low cost P-channel MOS technology
- +5 V and −5 V supplies only
- Interrupt-based service requests
- TTL compatible

1.3 DEVICE OPERATION

The TMS 5200 Voice Synthesis Processor (VSP) enables verbal communication with a microcomputer based system. The VSP is fabricated using P-channel MOS technology and is TTL compatible.

Speech data that has been compressed using pitch-excited linear predictive coding (LPC), is supplied to the VSP either by the CPU or by direct serial access of a Voice Synthesis Memory (VSM). The VSP decodes this data to construct a time-varying digital filter model of the vocal tract. This model is excited with a digital representation of either glottal air impulses (voiced sounds) or the rush of air (unvoiced sounds). The output of this model is passed through an eight-stage digital-to-analog converter to produce a synthetic speech waveform.

The VSP has been designed to minimize the data rate required to produce synthetic speech and to simplify the interface with the host CPU. The CPU may service the device either in a polled fashion, by monitoring device status, or by responding to interrupt service requests generated by the VSP. A simplified block diagram of the VSP is shown in Figure 1.

2. SYSTEM CLOCK

This manual describes all VSP timing based on an 8-kHz sample rate (limiting the output frequency to 4 kHz) and a 40-Hz frame rate (the rate at which new speech data is fetched and processed). This requires the internal RC oscillator in the VSP to run at 640 kHz. The user has the mask-programmable option of balancing the internal oscillator with a resistor (completing the RC network) or with a ceramic resonator (see Appendix A).[1]

The 640-kHz clock is divided by four to produce two major phases, PHI-1 and PHI-2, with corresponding precharge clocks, PHI-3 and PHI-4 (see Appendix A). All control and timing operations within the VSP occur on one of the two 6.25-microsecond major phases. Twenty of these 6.25-microsecond bit times comprise each sample period (8-kHz sample rate). Twenty-five of these 125-microsecond sample periods make up one 3.25 millisecond interpolation interval, eight of which (IC0-IC7) make up the 25-millisecond frame period. During IC0, new speech data is transferred to the Synthesizer, at a 40-Hz frame rate.

3. CPU INTERFACE

The CPU interface consists of an eight-bit bidirectional data bus (D0-D7), separate selects for read operations and write operations ($\overline{RS}$ & $\overline{WS}$), a ready line for synchronization ($\overline{READY}$) and an interrupt line ($\overline{INT}$) to indicate a status change on the VSP that requires CPU attention.

[1]When using a ceramic resonator, the internal oscillator runs at one half the rate of the RC Network. A divide-by-two instead of a divide-by-four RC Network is used to generate system clock signals.

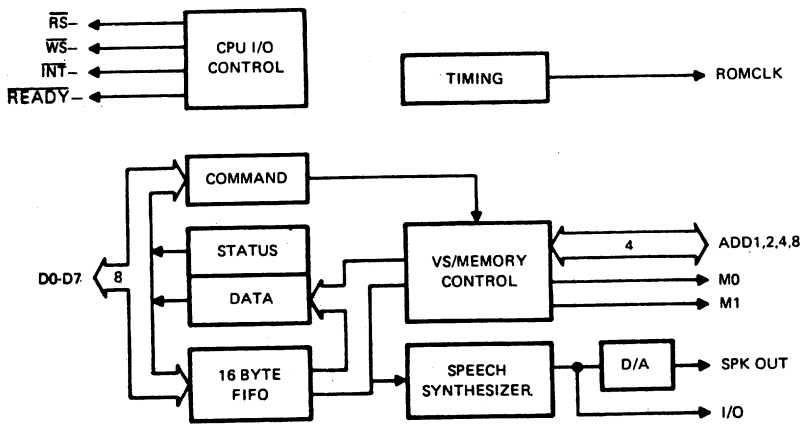


FIGURE 1 – VOICE SYNTHESIS PROCESSOR BLOCK DIAGRAM

3.1 $\overline{RS}$ AND $\overline{WS}$

VSP activity on the memory data bus is controlled by the select lines as shown below.

TABLE 1 – $\overline{RS}$ AND $\overline{WS}$ FUNCTION

$\overline{RS}$	$\overline{WS}$	BUFFER CONDITION
H	H	High impedance state
H	L	Input to VSP. Some other device must be driving the bus (typically the CPU)
L	H	Output from VSP. No other device should be driving the bus at this time.
L	L	Illegal condition. Results not predictable.

It is important to note that no device can successfully complete a Read cycle (from the VSP) while $\overline{WS}$ is active (low) nor can a successful Write cycle (to the VSP) be carried out while $\overline{RS}$ is active (low).

3.2 $\overline{\text{READY}}$

The VSP is a "Slow Memory"[2] device requiring wait states from the CPU to successfully complete a memory cycle. The effect of inserting wait states into memory access cycles is to extend the minimum allowable access time by one clock period from each wait state. The VSP controls the number of wait states executed by the CPU with the $\overline{\text{Ready}}$ signal. The logic timing for typical read and write cycles to the VSP is shown in Figure 2.

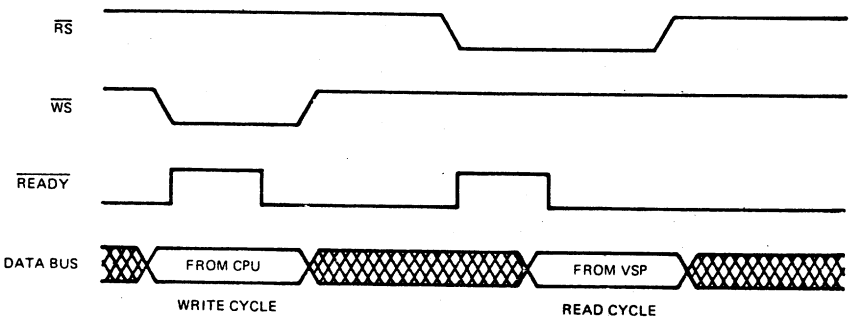


FIGURE 2 – READ & WRITE CYCLES TO THE VSP

The $\overline{\text{Ready}}$ line on the VSP goes high immediately when $\overline{\text{RS}}$ or $\overline{\text{WS}}$ goes active (low) to let the CPU know that the data transfer cycle cannot yet be completed. When the VSP has established stable data on the data bus (in the case of $\overline{\text{RS}}$) or has completed latching data in from the data bus (in the case of $\overline{\text{WS}}$), the $\overline{\text{Ready}}$ line will go low indicating that the CPU may complete the data transfer cycle.

3.3 INTERRUPTS

The interrupt line ($\overline{\text{INT}}$) indicates changes in the status of the VSP that may require CPU attention. $\overline{\text{INT}}$ goes active (low) when any of the following occur:

- Talk Status (TS) makes a one-to-zero transition indicating the end of speech processing.
- Buffer Low (BL) makes a zero-to-one transition indicating that more phrase data needs to be supplied to the FIFO for Speak External Command.
- Buffer Empty (BE) makes a zero-to-one transition indicating that the CPU failed to supply data fast enough for a Speak External Command.[3]

$\overline{\text{INT}}$ goes inactive (high) when the Status Register is read, or if the Reset instruction is executed.

4. VOICE SYNTHESIS MEMORY (VSM) – (TMS 6100)

In addition to receiving speech data from the CPU, the VSP may directly access up to 16 TMS 6100's (128K-bit serial ROM) with no external hardware required. This is accomplished with a four-bit parallel bus (ADD8,4,2,1), (ADD8 is multiplexed as the Data Out line), two control lines (M0, M1), and a synchronizing clock (ROMCLK).

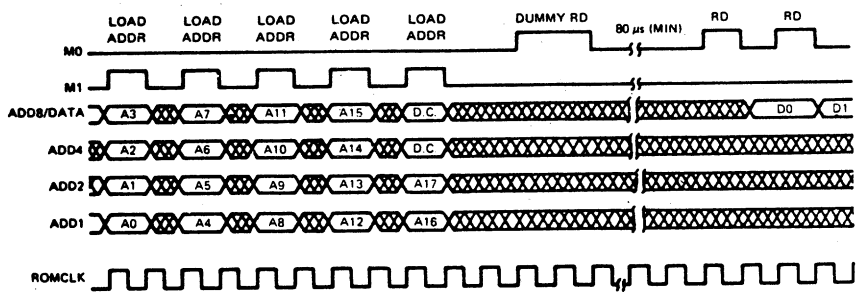
[2]Slow Memory devices are those devices that cannot properly respond to system memory cycles within the minimum access time as determined by the CPU clock rate.

[3]An interrupt will be generated at the initiation of a Speak External Instruction if BE was previously low.

The TMS 6100 is a mask programmable 128K-bit-Read-Only Memory internally organized as 16K words of eight bits; externally it appears as 128K X 1. Once the 20-bit address (14 bits to select a byte within the device, four chip select bits, two bits ignored) is loaded through ADD1, ADD2, ADD4, and ADD8 in five Load Address sequences, data is read out bit-wise by toggling a control pin (M0). The ROM contains an on-chip address counter which is incremented every eight bits (eight toggles of M0). The four internal chip select bits are a mask programmable option, and allow parallel connection of up to 16 ROMs (about 30 minutes of speech) without the need of external select circuitry.

M0	M1	FUNCTION
L	L	Idle – The passive NOP state of TMS 6100
L	H	Load Address – The four bits of data on ADD8,4,2,1 are loaded to the internal address register at the location indicated by the TMS 6100 Load Pointer. After each Load Address function, the Load Pointer is advanced to the left by four bit positions to allow the next most-significant nibble of the address to be properly loaded. The first read function[4], following a Load Address function, resets the Load Pointer to the LS bit and initiates a ROM access to fetch the address data byte. This is the only function of this "Dummy Read". No data is transferred out of VSM until the second read function following a Load Address.
H	L	Read – When the addressed data byte has been fetched and stored in the VSM Data Register, it is ready to serially transferred out starting with the MSB. Each successive read function causes the next least-significant bit to be driven on the Data Out line of the VSM that is currently selected. The next data byte is being fetched at the same time the serial transfer is taking place so that when the last bit of the current byte is transferred, the VSM Data Register can be reloaded without delay. When the Read function immediately follows a Load Address function, it is treated as a "Dummy Read". No data is transferred, but the Load Pointer is reset and ROM access is
H	H	initiated. Read & Branch – Starting at the current address, two bytes are fetched from ROM to form a 16-bit word. The 14 low-order bits of this word replace the 14 low-order bits of the Address Register. The Load Pointer is then reset and a ROM access initiated to fetch the byte at this new address.*

Figure 3 shows a typical sequence of loading the Address Register and reading two data bits back. For more critical timing constraints, consult the TMS 6100 Electrical Specification.



NOTE: A0 is the LSB in 6100 address.

FIGURE 3 – TMS 6100 FUNCTION TIMING

[4]A minimum of two Load Address instructions are required to change the VSM address.
*Read & Branch will not work with multiple VSM systems. Bus contention will occur.

5. I/O STRUCTURE

The VSP has two input holding registers, a Command Register and a 128-bit FIFO Buffer, and two output holding registers, the Data Register and the Status Register. On a Write cycle from the CPU, when $\overline{WS}$ becomes active (low), the control logic of the VSP routes data from the Memory Data Bus to either the FIFO Buffer (if a Speak External command is executing) or the Command Register (all other cases). Once this data has been latched in, the VSP signals completion of the data transfer to the CPU by lowering the $\overline{Ready}$ Line to its active (low) condition. Similarly, on a Read cycle, when $\overline{RS}$ goes active (low), the VSP puts either the contents of the Data Register on the bus (if the preceding command was a Read Byte command) or the contents of the Status Register (all other cases).

5.1 COMMAND REGISTER

The Command Register receives command data from the Memory Data Bus and holds it for the Controller to interpret and execute. The VSP behaves as an attached processor to the host CPU and performs its synthesis tasks when appropriate commands are sent by the host CPU. For details on available commands and format, see Section 6.

5.2 FIFO BUFFER

The 128-bit FIFO Buffer is organized as a 16-byte parallel-in, serial-out buffer. This buffer is used to hold speech data passed from the CPU to be processed by a Speak External command in the VSP. As required by the synthesis section, data is shifted out serially starting with the LSB from the "First-In" byte. When this byte has been exhausted, the stack ripples down one byte and begins shifting out bits from the new "First-In" byte. A Stack Pointer keeps track of the location of the "Last-In" byte and data from the CPU is always loaded just above this location. When the stack becomes less than half full (i.e., eight byte locations are void of data), the buffer-low status condition (BL) becomes true. This signals the CPU that more data should be provided to the VSP. Under worst-case conditions, the buffer will be completely empty in two more frame periods (50 milliseconds), and invalid data will be processed as external speech data. As a Fail-Safe measure, if the buffer does reach such a condition, the buffer empty status (BE) becomes true and the Talk Status Latch is reset causing speech to terminate immediately. To resume speech with data provided by the CPU, another Speak External command must be issued.

5.3 DATA REGISTER

The eight bit Data Register is organized as a serial-in, parallel out Holding Register. This register is used by the VSP to formulate a byte of data from serial data fetched from the VSM during the execution of a Read Byte command. Data is loaded to the Data Register so that the last bit loaded is in the least-significant bit location (D7). When the Data Register has been loaded and $\overline{RS}$ goes active (low), this byte is transferred to the Memory Data Bus (D0 = MSB). The $\overline{Ready}$ Line goes low when the data is stable.

5.4 STATUS REGISTER

The three bits of the Status Register provide up-to-date information to the CPU on the state of the VSP. The Status Register may be read at any time except immediately after passing a Read Byte command to the VSP. When $\overline{RS}$ goes active (low) the VSP routes the status data to the Memory Data Bus (D0 = TS; D1 = BL; D2 = BE) and lowers the $\overline{Ready}$ Line to indicate the data is stable.

TS – Talk Status is active (high) when the VSP is processing speech data. Talk Status goes active at the initiation of a Speak command or after nine bytes of data are loaded into the FIFO following a Speak External command. It goes inactive (low) when the stop code (Energy = 1111) is processed, or immediately by a buffer empty condition or a reset command. Audio output is interpolating to zero during this frame and is terminated on the next frame boundary.

BL – Buffer Low is active (high) when the FIFO Buffer is more than half empty. Buffer Low is set when the "Last-In" byte is shifted down past the half-full boundary (becomes the eight data byte) of the stack. Buffer Low is cleared when data is loaded to the stack so that the "Last-In" byte lies above the half-full boundary and becomes the ninth data byte of the stack.

BE – Buffer Empty is active (high) when the FIFO Buffer has run out of data while executing a Speak External command. Buffer Empty is set when the last bit of the "Last-In" byte is shifted out to the Synthesis Section. This causes Talk Status to be cleared. Speech is terminated at some abnormal point and the Speak External command execution is terminated. Data from the Memory Data Bus is once again routed to the Command Register.

6. DESCRIPTION OF COMMANDS

The VSP operates under the control of the CPU to a minimal degree. The CPU passes commands to the VSP which initiate an activity but the CPU is not involved in carrying out that activity. Commands available to the CPU and the format for commands are shown below:

TABLE 2 – VSP COMMANDS & COMMAND FORMAT

DATA BUS COMMAND CODE (D0-D7)*	OPERATION
X000XXXX	NOP
X001XXXX	READ BYTE
X010XXXX	NOP
X110XXXX	SPEAK EXTERNAL
X011XXXX	READ & BRANCH
X100AAAA	LOAD ADDRESS
X101XXXX	SPEAK
X111XXXX	RESET

*A = Address
X = Don't Care

When $\overline{WS}$ becomes active (low), assuming a Speak External command is not presently executing, the data on the memory data bus is latched into the command register. Once the transfer has been completed, the VSP activates (low level) the $\overline{Ready}$ line to release the CPU and begins interpreting and executing the command. Command execution for each instruction is described below.

If the user tries to pass a command to the VSP while another command is executing, the new command will not be accepted until the previous command is completed. The VSP keeps the CPU executing wait states until it is ready to accept a new command. Appendix C lists execution times for each command.

6.1 READ BYTE

The Read Byte command allows the CPU to access data stored in the TMS 6100 VSM. Read Byte causes the next eight bits to be read from the VSM (ignoring byte boundaries). These bits are packed into the data register so that the last bit read from VSM is in the least-significant-bit position (D7). When $\overline{RS}$ goes active (low), and before initiation of a new instruction, this data byte is placed on D0-D7.

This eight-bit transfer from the VSM requires 80 microseconds. If $\overline{RS}$ should become active before the data register is completely loaded and ready to be transferred, the VSP keeps the CPU executing wait states (by not lowering the $\overline{Ready}$ line) until the data transfer from VSM is complete and the Data Byte is stable on the Memory Data Bus. At this time the $\overline{Ready}$ line is activated and the CPU may accept the Data Byte to complete the memory cycle.

6.2 READ AND BRANCH

The Read & Branch command causes the VSP to initiate a Read and Branch function on the VSM (see VSM description). The VSP is not able to access the VSM for 240 microseconds after executing this command.

6.3 LOAD ADDRESS

The Load Address command allows the CPU to alter the Address Register of the TMS 6100 to point to new speech data. Load Address causes the VSP to load the four address bits from the VSP Address Register to one nibble of the VSM Address Register by initiating a VSM Load Address function (see VSM description). If the next command following is a Read Byte, Speak, or Reset command, a dummy Read function is passed to the VSM before that next command is executed. Bit D7 is loaded into ADD1 which is the LSB of the VSM address. Bit D4 is loaded into ADD8.

6.4 SPEAK

The Speak command allows speech to be generated from phrase data stored in the VSM. The Speak command generates an internal signal that immediately causes Talk Status to be set and initiates speech synthesis calculations using the next available data from the VSM. Audio output begins on the following frame boundary. The VSP continues to fetch data from the VSM and generates speech output until a stop code (Energy = 1111) is received and recognized. At such time the audio output begins to interpolate down to the zero energy level. On the next frame boundary, speech has ended and the Talk Status is cleared. This completes execution of the Speak command. Execution of the Speak command may also be halted by the execution of Reset command. This causes audio output to halt immediately (without waiting for a frame boundary) and Talk Status to be cleared.

6.5 SPEAK EXTERNAL

The Speak External command allows the CPU to supply speech data to the VSP from some memory other than the VSM. Upon receipt of a Speak External command, the VSP purges the FIFO buffer (BL and BE becomes active [high]) and directs data written to the VSP to this buffer. The VSP idles waiting for the CPU to fill the buffer before speech begins. When the buffer low status becomes false (by the CPU loading a minimum of nine bytes to the FIFO), Talk Status is set and speech synthesis calculations begin using data from the FIFO. Data continues to be taken from the FIFO until a stop code is encountered or the buffer empty abnormal termination occurs. While the Speak External command is executing, all data written to the VSP is routed to the FIFO Buffer. A Reset command is not recognized as a command.

6.6 RESET

The Reset command allows the CPU to halt the Speak command and to put the VSP into a known state. Reset clears Talk Status, halting speech activity immediately. The 128-bit FIFO Buffer is purged (BL and BE become active [high]) and the I/O paths are set to their default condition (Memory Data Bus → Command Register; Status Register → Memory Data Bus). A Load Address function is given to the VSM (using dummy address data) followed by a "Dummy Read" function.

The Reset command cannot halt the Speak External command. Flow diagrams for each instruction are given in Appendix B. System timing diagrams may be found in Appendix C.

7. POWER-UP CLEAR

The VSP contains internal circuitry to ensure a clear condition 95 percent of the time upon power-up, provided the $V_{SS} - V_{DD}$ rise time to +10 volts is less than 2 milliseconds. The Power-Up Clear sequence is finished 15 milliseconds after $V_{SS} - V_{DD}$ reaches +10 volts. The events caused by the Power-Up Clear sequence are similar to the Reset Command and are noted below:

- Talk Status is cleared and any speech activity is halted.
- The T State Counter is Reset.
- The FIFO is purged (BL & BE go active [high]) possibly causing the $\overline{INT}$ line to become active (low).
- I/O multiplexers are set to allow data to be written to the Command Register, and Data Read from the Status Register.
- The TMS 6100 assumes a known state by issuing a Load Address (using arbitary address data) followed by a "Dummy Read"

If the user requires higher reliability in securing initialization, he should execute his own initialization sequence. A 100 percent assurance can be given that the VSP is in a clear state by writing eight bytes of all "ones" to the VSP, followed by a Reset command.

8. SPEECH SYNTHESIS

As previously mentioned, speech data fed to to the VSP is encoded using pitched-excited LPC. The process of recovering this data is described briefly here and in more detail in the following sections. (This information is intended solely for the reader's information. Proper application of the VSP does not depend on a thorough understanding of the process). A simplified block diagram of the speech synthesis element of the VSP is given in Figure 4.

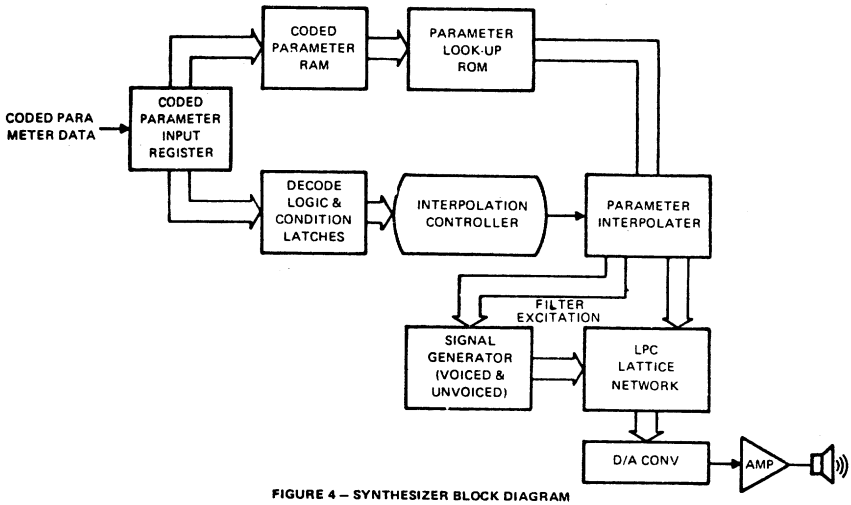


FIGURE 4 – SYNTHESIZER BLOCK DIAGRAM

Coded speech parameter data is fed serially from either the VSM or the FIFO buffer to the Parameter Input Register. Here the Controller unpacks the data and performs various tests (i.e., is the repeat bit set, is pitch zero, is energy zero). Once unpacked the coded parameter data is stored in RAM to be used as the index value to select the appropriate value from the Parameter Look-Up ROM. The outputs of the Parameter Look-Up ROM are the target values for the interpolation logic to reach in this frame period. During each of the eight interpolation periods the interpolation logic sends new pitch and energy parameters to the signal generator which produces the filter excitation sequence, and new K-parameter values to the LPC lattice network. So, at the end of each sample period there is a new value of digitized synthetic speech available to the D/A converter.

8.1 CODED SPEECH PARAMETERS

The 12 synthesis parameters (pitch, energy and reflection coefficients K1-K10), are stored in the VSM in coded form. Each parameter occupies between 3-6 bits. These coded values select a 10-bit actual parameter from the parameter Look-Up ROM. Depending on the influence of each parameter on speech quality, between 8 and 64 possible values are stored in the Look-Up ROM for decoding and use in synthesis calculations. Table 3 summarizes parameter coding for the TMS 5200.

TABLE 3 – PARAMETER CODING

PARAMETER	LEVELS	CODE BITS
ENERGY	15	4
PITCH	64	6
K1	32	5
K2	32	5
K3	16	4
K4	16	4
K5	16	4
K6	16	4
K7	16	4
K8	8	3
K9	8	3
K10	8	3
12	247	49 + REPEAT = 50 BITS

A full set of coded parameters for each frame would require a data rate of 40 Hz X 50 bits = 2000 bits per second. Three special cases, in which a full frame is not necessary, allow the data rate to be considerably reduced:

(1) Since the vocal tract changes shape relatively slowly, it is often possible to repeat previous reflection coefficient data. To facilitate the repeat feature, a control bit has been added to each frame (an additional bit following energy). If the repeat bit is 1, only energy and pitch data are accessed from the VSM and the previous K1-K10 values are retained.

(2) Unvoiced speech requires fewer filter reflection coefficients. When Pitch = 0, only K1-K4 are fetched from the VSM and stored in the Parameter RAM. K5-K10 are zeroed.

(3) When Energy = 0, no other data is required. Energy = 0 during interword or intersyllable pauses. The combination of these three cases has reduced average data rate for male speech to approximately 1200 bits per second.

Figure 5 shows the four possibilities of frame data string lengths.

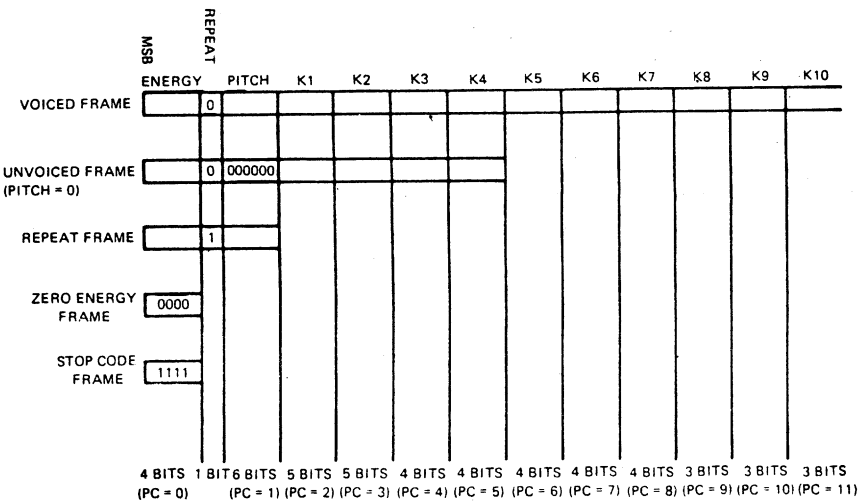


FIGURE 5 – FRAME DATA STRING LENGTHS

One complete set of parameters (12), used as target values during interpolation, is stored in coded form in the synthesizer. The storage medium is a 50-bit RAM of variable word length, e.g., six bits for pitch, three bits for K10. Data is supplied to the RAM via the parallel outputs of a serial shift register which accepts data from some VSM. The Parameter RAM outputs are used as inputs for the Parameter ROM.

8.2 D/A CONVERSION

The VSP contains an eight-bit digital-to-analog converter with ½ LSB resolution. Every 100 microseconds the most-significant 10 bits of the 14-bit lattice filter output are sampled. From this sample, the seven low-order bits and the sign bit (MSB) are sent to the D/A converter. The remaining two bits are combined logically with the sign bit and used to clip the driver to either a full ON or full OFF condition. Table 4 shows the analog output from the D/A converter for various inputs from the lattice filter.

TABLE 4 – DIGITAL-TO-ANALOG CONVERTER OUTPUT

NO.	Y LATCH OUTPUT				D/A INPUT	ANALOG OUTPUT (μA)
	Y_{L13}	Y_{L12}	Y_{L11}	Y_{L10}–Y_{L4}		
	0	1	1	X	11111111	0
>+127	0	1	0	X	11111111	0
	0	0	1	X	11111111	0
127	0	0	0	1111111	11111111	0
126	0	0	0	1111110	11111110	5.86
			–			
			–			
			–			
+1	0	0	0	0000001	10000001	738
0	0	0	0	0000000	10000000	744
*–1	1	1	1	1111111	01111111	750
–2	1	1	1	1111110	01111110	755.8
			–			
			–			
			–			
–128	1	1	1	0000000	00000000	1500
<–128	1	1	0	X	00000000	1500
	1	0	1	X	00000000	1500
	1	0	0	X	00000000	1500

*No output, resting level.

8.3 AUDIO OUTPUT

The output of the D/A converter (see Table 4) is a current source designed to deliver 0 to 1.5 milliampere with resolution to 5.9 microamperes. This output has been optimized to drive the EXT AUD input of the SN76489AN sound generator chip. With a 1.8-kilohm resistor in series, the VSP delivers 3 volts (I = 1.5 milliamperes) when the Y latch output is less than –128. When the Y latch output is greater than +127, the audio output is clipped to zero volts. When no speech generation is taking place, the Y latch output is –1 making the audio output drive 750 microamperes. (Speaker output must be ac-coupled to audio amplifier.)

9. ELECTRICAL CHARACTERISTICS

9.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Supply voltage, V_{DD} . . . . . –20 to +0.3 V
Supply voltage V_{SS} . . . . . –20 to +0.3 V
Operating temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –30°C to 125°C
Power Dissipation . . . . . 600 mW

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

9.2 RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{SS}	4.5	5	5.5	V
Supply voltage, V_{REF}	–0.8	0	+0.6	V
Supply voltage, V_{DD}	–4.5	–5	–5.5	V
High level input voltage, V_{IH}	V_{SS}–0.6		V_{SS}	V
Low level input voltage, V_{IL} (see Note 1)		0	V_{SS}–4	V
Operating free-air temperature, T_A	0		70	°C

NOTE 1: The algebraic convention where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic voltages levels only.

9.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

	PARAMETER	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage, (I_{OH} = −0.4 mA)	2.4		V_{SS}	V
V_{OL}	Low level output voltage, (I_{OL} = 1.6 mA)	(V_{REF}−0.5)	0	(V_{REF}+0.5)	V
I_{REF}	Supply current from V_{REF}		3	5	mA
I_{DD}	Supply current from V_{DD}		10	35	mA
C_i	Input capacitance, (except data bus)		15		pF
C_o	Output capacitance, (except data bus)		15		pF
C_{db}	Data bus load capacitance	25		300	pF

9.4 STATIC DISCHARGE PROTECTION

All inputs and outputs are guarded against electrostatic damage by state-of-the-art protection devices incorporated on the chip.

10. ENVIRONMENTAL

10.1 TEMPERATURE RANGE

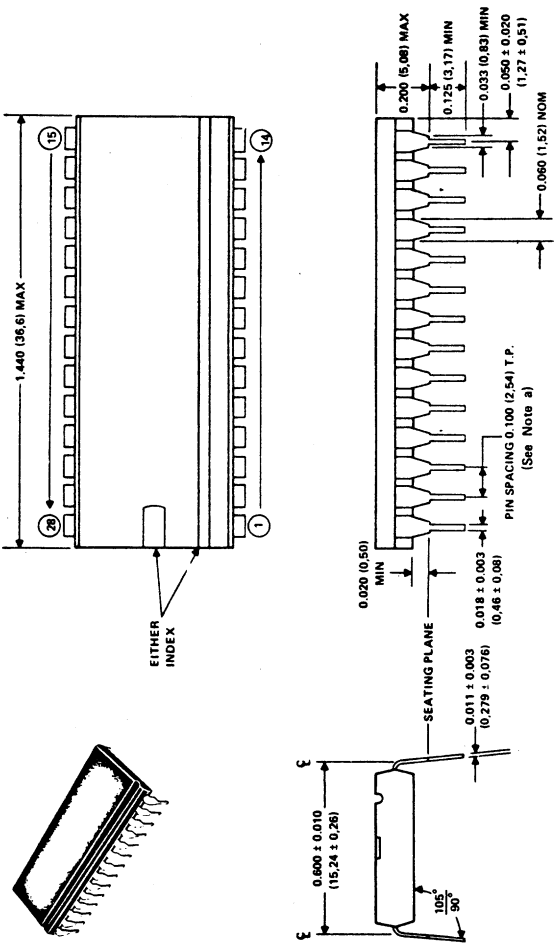
Operating: 0°C to 70°C
Storage: −40°C to 70°C

10.2 HUMIDITY

Operating: 85% Relative Humidity at 35°C
Storage: 95% Relative Humidity at 55°C

11. MECHANICAL DATA

11.1 28-PIN 600-MIL PLASTIC PACKAGE (100-MIL PIN SPACING)

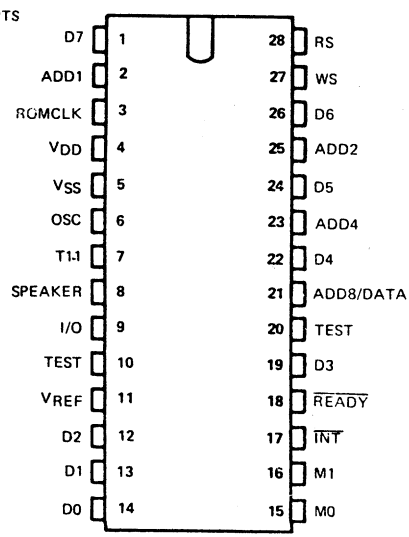


NOTES: a. Each pin centerline is located within 0.010 inch (0,26 millimeters) of its true longitudinal position.
b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

11.2 PIN ASSIGNMENTS AND FUNCTIONS

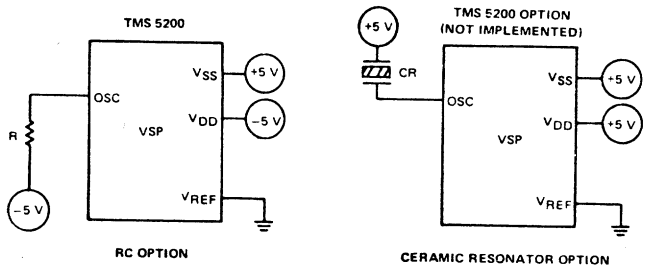
PIN	NAME	IN/OUT	FUNCTION
1	DBUS 7	I/O	Memory data bus (LSB)
2	ADD1	O	Address bus to VSM (LSB)
3	ROMCLK	O	Clock to VSM
4	V_{DD}	I	Drain supply voltage (−5 V NOM)
5	V_{SS}	I	Substrate supply voltage (+5 V NOM)
6	OSC	I	Oscillator input
7	T11		Sync
8	SPEAKER	O	Audio output
9	I/O	O	Serial data out
10	TEST		Testing use only
11	V_{REF}	I	Ground reference voltage (0 V NOM)
12	DBUS 2	I/O	Memory data bus
13	DBUS 1	I/O	Memory data bus
14	DBUS 0	I/O	Memory data bus (MSB)
15	M0	O	Command bit 0 to VSM
16	M1	O	Command bit 1 to VSM
17	$\overline{INT}$	O	Interrupt (active low)
18	$\overline{READY}$	O	Transfer cycle W/CPU complete
19	DBUS 3	I/O	Memory data bus
20	TEST		Testing use only
21	ADD8/DATA	I/O	Address to VSM & serial data in (MSB)
22	DBUS 4	I/O	Memory data bus
23	ADD 4	O	Address bus to VSM
24	DBUS 5	I/O	Memory data bus
25	ADD 2	O	Address bus to VSM
26	DBUS 6	I/O	Memory data bus
27	$\overline{WS}$	I	Write select (active low)
28	$\overline{RS}$	I	Read select (active low)

11.3 TERMINAL ASSIGNMENTS



APPENDIX A

SYSTEM CLOCKS



TYPICAL VALUES:

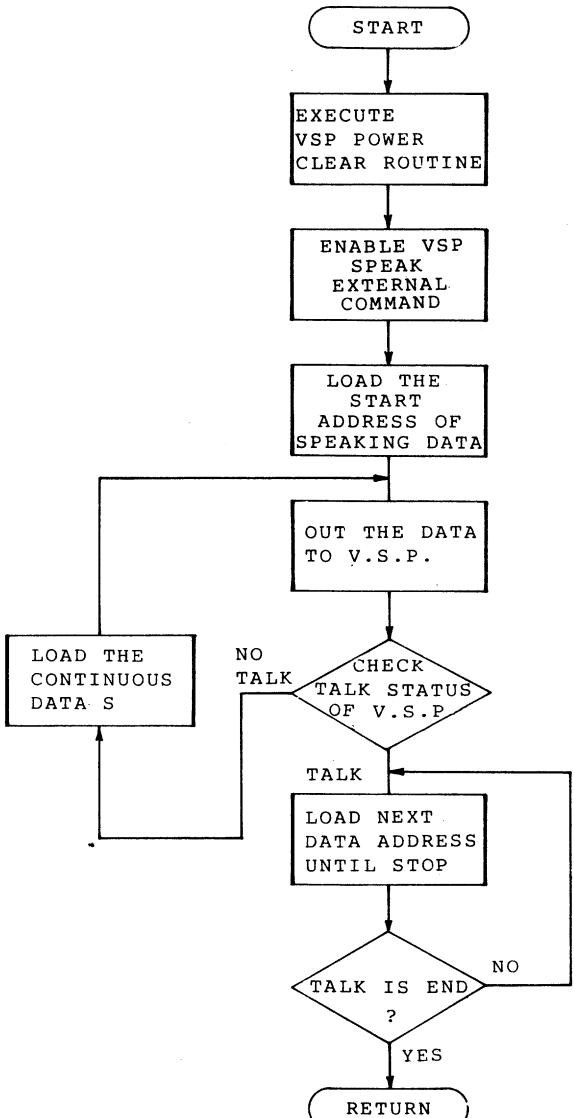
SAMPLE FREQUENCY	R	CERAMIC RESONATOR
10 kHz	R = 80-100 kΩ	CR = 400 kHz
8 kHz	R = 120-200 kΩ	CR = 320 kHz

FIGURE A-1 – TMS 5200 OSCILLATOR OPTIONS

4. SPEECH PROGAM UTILITY

```
LOC   OBJ CODE M STMT SOURCE STATEMENT

                    1  ;
                    2  ;       ***********************************
                    3  ;       *   SSB-MPF   DEMO_SUBROUTINE.S   *
                    4  ;       ***********************************
                    5  ;
                    6  ;COPYRIGHT,MULTITECH INDUSTRIAL CORP. 1982
                    7  ;Written by Yung Jui Chen, R&D department.
                    8  ;Routine address is 5200H
                    9  ;Speech subroutine utility
                   10  ;User give speech data address then call
                   11  ;this routine
                   12  ;For example,  LD       HL,6000H
                   13  ;              CALL     START
                   14  ;         or   CALL     5200H
                   15  ;     then it will speak the word at address 6000H
                   16  ;
                   17  PORT    EQU     0FEH            ;I/O address of SSB-MPF
5200               18          ORG     5200H           ;assembly program start
                   19                                  ;address
5200  0610       20  START   LD      B,10H           ;reset counter
5202  3EFF       21  RESET   LD      A,0FFH          ;TMS 5200 reset code is
                   22                                  ;*111****
5204  D3FE       23          OUT     (PORT),A        ;send the reset command
5206  CD2E52   R 24          CALL    DELY
5209  10F7       25          DJNZ    RESET           ;reset routine
520B  3E60       26          LD      A,60H           ;enable speak external
                   27                                  ;command
520D  D3FE       28          OUT     (PORT),A        ;VSP is ready
520F  CD2E52   R 29          CALL    DELY
5212  7E         30  SEND1   LD      A,(HL)          ;fetch speak data
5213  D3FE       31          OUT     (PORT),A        ;send data to TMS 5200
5215  CD2E52   R 32          CALL    DELY
5218  23         33          INC     HL              ;next data
5219  DBFE       34          IN      A,(PORT)        ;read the status of VSP
521B  CB7F       35          BIT     7,A             ;check talking status
521D  28F3       36          JR      Z,SEND1         ;need more data to VSP
521F  7E         37  SEND2   LD      A,(HL)          ;load the next data of
                   38                                  ;send1 loop
5220  D3FE       39          OUT     (PORT),A        ;send data continue
5222  CD2E52   R 40          CALL    DELY
5225  23         41          INC     HL              ;next address
5226  DBFE       42          IN      A,(PORT)        ;check the talk status
                   43                                  ;activate or not
5228  CB7F       44          BIT     7,A             ;get the stop code?
522A  C21F52   R 45          JP      NZ,SEND2        ;if no,send the rest
                   46                                  ;data and check
522D  C9         47          RET                     ;if yes,complete progra
                   48                                  ;return to main prog.
522E  C5         49  DELY    PUSH    BC              ;delay routine
522F  06FF       50          LD      B,0FFH          ;delay counter
5231  10FE       51          DJNZ    $-
5233  C1         52          POP     BC
5234  C9         53          RET
                   54
```


START
EXECUTE VSP POWER CLEAR ROUTINE
ENABLE VSP SPEAK EXTERNAL COMMAND
LOAD THE START ADDRESS OF SPEAKING DATA
OUT THE DATA TO V.S.P.
CHECK TALK STATUS OF V.S.P
NO TALK
LOAD THE CONTINUOUS DATA S
TALK
LOAD NEXT DATA ADDRESS UNTIL STOP
TALK IS END ?
NO
YES
RETURN

5. SPEECH VOCABULARY LIBRARY

****
* SPEECH VOCABULARY LIBRARY *
****

I. Speech Vocabulary Library for Standard Memory Chip

VOCABULARY	ADDRESS
ONE	5400H
TWO	5458H
THREE	56E8H
FOUR	5498H
FIVE	5528H
SIX	54E8H
SEVEN	55A0H
EIGHT	55F0H
NINE	5620H
TEN	56A0H
ELEVEN	58B8H
TWELVE	5868H
THIRTEEN	5738H
FOURTEEN	5918H
FIFTEEN	5988H
SIXTEEN	5C20H
SEVENTEEN	5B88H
EIGHTEEN	5B20H
NINETEEN	5AA8H
TWENTY	5810H
THIRTY	57D0H
FORTY	5A18H
FIFTY	5A60H
IT	5E10H
IS	5E48H
AM	5CA8H
PM	5CF8H
O'CLOCK	5D60H
OH	5DE0H
GOOD	5E90H
MORNING	5EB8H
AFTERNOON	5F28H
PAUSE	5F80H
NULL	5FB8H

II. Speech Vocabulary Library for Optional Memory Chips

FILE NAME : SSB-E1

ADDRESS	WORD	ADDRESS	WORD	ADDRESS	WORD
000	0	54B	ALL	9DE	CONSOLE
046	1	574	AM	A27	CONNECTED
099	2	5BA	AN	A8F	COMPUTER
0D7	3	5F0	AND	AE6	COMPLETED
124	4	657	ASSUME	B4D	COMPLETE
16E	5	694	AT	BA9	CYAN
1E5	6	6B1	B	BEC	COURSE
225	7	6D3	BACK	C2A	D
274	8	6FE	BASE	C63	DEVICE
2A1	9	74D	BE	CCC	DECIDE
321	A	76F	BETWEEN	D35	DATA
33D	A1	7D8	BLACK	D8D	DOING
351	ABOUT	81B	BLUE	DE1	DOES
3A6	AFTER	847	BOTH	E18	DO
3E2	AGAIN	87B	COMES	E4B	DISKETTE
444	ANSWER	8D2	COME	E9E	DIFFERENT
493	ANY	905	COMMAND	F07	DID
4D8	ARE	95C	COMMA	F65	DOWN
50A	AS	999	CORRECT	FA4	DOUBLE

FILE NAME : SSB-E2

ADDRESS	WORD	ADDRESS	WORD	ADDRESS	WORD
000	DONE	52E	FIFTEEN	A91	GAMES
05B	DRAWING	589	FINISH	AF5	GO
0BE	DRAW	5C2	FINE	B2A	GIVES
114	E	5FF	FIND	B99	GIVE
139	END	646	FIT	BEE	GOOD
1AA	ELSE	670	FIRST	C12	GOING
1E9	ELEVEN	6AD	FINISHED	C6F	GOES
246	EIGHTY	6F0	FORTY	CB7	GOT
27C	EIGHT	731	FOR	CE8	GOODBYE
2A9	EACH	77B	FIVE	D3F	#GOOD WORK#
2DC	ERROR	7F2	FOURTH	D8E	GUESS
324	ENTER	84D	FOURTEEN	DD0	GREEN
366	ENDS	8E7	FOUR	E31	GRAY
3AD	EXACTLY	931	FRONT	E7D	HAND
415	EYE	960	FROM	EC3	HAD
451	F	9A8	G	F0D	H
474	FIGURE	9E5	GETTING	F3C	HAVE
4EB	FIFTY	A63	GET	F7E	HAS

FILE NAME : SSB-E3

ADDRESS	WORD	ADDRESS	WORD	ADDRESS	WORD
000	#HANDHELD UNIT#	54F	IT	A18	LIKES
086	HIGHER	583	IS	A83	LIKE
0E2	HERE	5CB	INSTRUCTIONS	ABE	LET
117	HEAD	640	INSTRUCTION	AE5	LESS
170	HOME	6B2	L	B3B	LONG
1BB	HIT	6F3	KNOW	BA5	LOAD
1EF	HURRY	733	KEYBOARD	C2D	LINE
22B	HUNDRED	799	KEY	CA3	LOWER
293	HOW	7C9	K	CFF	LOOKS
2F9	IF	7F8	JUST	D45	LOOK
31B	#I WIN#	836	LARGEST	D99	MAGENTA
39C	I	8AD	LARGER	E19	MADE
3D8	INCHES	8FB	LARGE	E60	M
429	INCH	944	LEFT	E94	MESSAGES
4B1	JOYSTICK	97E	LEARN	F0E	MESSAGE
510	J	9D8	LAST	F79	MEMORY

FILE NAME : SSB-E4

ADDRESS	WORD	ADDRESS	WORD	ADDRESS	WORD
000	MEAN	55F	#NICE TRY#	A40	OTHER
048	ME	608	NEXT	A8A	ORDER
088	MAKE	654	NOT	AE0	PARTS
0D7	MODULE	683	NO	B30	P
13A	MIGHT	6C3	NINETY	B69	OVER
186	MIDDLE	720	O	BC5	PLAYS
1C8	MOVE	75D	OF	C2B	PLAY
226	MOST	7B6	NUMBER	C73	PERIOD
272	MORE	813	NOW	CD7	PRINT
2C3	NAME	859	ON	D14	PRESS
336	N	8A3	OH	D50	POSITIVE
370	MUST	8E0	OFF	DCE	POSITION
3B9	NEGATIVE	91E	OR	E39	POINT
436	NEED	966	ONLY	E95	PLEASE
492	NEAR	9B7	ONE	EEE	PROBLEMS
4DF	NINE	A0A	OUT	F7C	PROBLEM

FILE NAME : SSB-E5

ADDRESS	WORD	ADDRESS	WORD	ADDRESS	WORD
000	PRINTER	5F5	REMEMBER	B27	SEVEN
04F	PUTTING	663	S	B76	SHORT
0C5	PUT	6AA	ROUND	BBF	SHIFT
0F8	PROGRAM	742	RIGHT	BF4	SHAPES
181	RANDOMLY	797	SAY	C3D	SIXTY
233	R	7D4	SAVE	C93	SIX
265	Q	84A	SAID	CD3	SIDES
2B3	#READY TO START#	898	SECOND	D25	SIDE
345	READ1	8FB	SCREEN	D80	SHOULD
385	READ	95B	SAYS	DC9	SHORTER
3E6	REFER	9B5	SET	E48	SMALLEST
446	RED	9EA	SEE	EAA	SMALLER
486	RECORDER	A3D	SEES	EED	SMALL
502	REWIND	A99	SHAPE	F2B	SPACE
58A	RETURN	AD2	SEVENTY	F62	SORRY

FILE NAME : SSB-E6

ADDRESS	WORD	ADDRESS	WORD	ADDRESS	WORD
000	SO	4AC	#THAT IS INCORRECT#	AE6	THIRTEEN
044	SQUARE	594	THAT	B77	THROUGH
08D	SPELL	5F4	THAN	BBA	THREW
0F4	SPACES	64F	THE	BFD	THREE
163	STOP	691	#THAT IS RIGHT#	C4A	TRY
18F	STEP	707	THERE	C9E	TQP
1C1	START	773	THEN	CCC	TONE
20A	#SUPPOSED TO#	804	THE1	D3A	TOGETHER
275	SUPPOSED	82F	THING	DA9	TO
2DB	SUM	8AE	THEY	DE7	TIME
30A	TAKE	8F7	THESE	E2E	TWELVE
33E	T	960	THIRD	E79	TURN
378	SURE	9B5	THINK	EB5	#TRY AGAIN#
3D5	TEN	9FE	THINGS	F38	TYPE
41D	TELL	A62	THIS	F86	TWO
468	TEEN	AAA	THIRTY		

FILE NAME : SSB-E7

ADDRESS	WORD	ADDRESS	WORD	ADDRESS	WORD
000	TWENTY	5A8	WANTS	B71	Z
057	UPPER	604	WHEN	BAC	YOUR
097	UP	63A	#WHAT WAS THAT#	BF8	#YOU WIN#
0BB	UNTIL	6C6	WHAT	C6A	YOU
12B	UNDERSTAND	6F3	WHO	CA0	YET
1BD	UNDER	73E	WHITE	CE2	CASSETTE
215	U	783	WHICH	D19	CENTER
24B	WANT	7B3	WHERE	D54	CHECK
28D	W	7FC	WON	D74	CHOICE
30A	VERY	84F	WITH	DB8	CLEAR
360	VARY	88F	WILL	DF2	COLOR
3A3	V	8E9	WHY	E26	BOTTOM
3E1	USE	946	YELLOW	E5C	BUT
427	WERE	9A6	Y	E84	BUY
487	WELL	9EC	X	EC2	BY
4CC	WEIGHT	A11	WRITE	F00	BYE
50E	WE	A66	#TEXAS INSTRUMENTS#	F5E	C
541	WAY	B2B	ZERO		

FILE NAME : SSB-E8

ADDRESS	WORD	ADDRESS	WORD	ADDRESS	WORD
000	#LEON THINKS IT ABNORMAL FOR A GIRAFFE TO ROLL ON THE GROUND#	9C2	BIG	CBD	MONKEY
38E	#YOU'RE RIGHT#	9FA	CAKE	D13	CLOWN
401	#LOOK AGAIN#	A39	CAN'T	DB7	COW
4A2	ROMEO	A79	CANNOT	DD4	DOG
565	TWENTY	AEA	CAR	E2B	DRUM
5DE	ZEBRA	B3E	CHILDREN	E77	DUCK
800	ANIMALS	BA1	CHOOSE	EB7	EATS
85A	ASTRONAUT	BF9	FUNNY	EEF	ELEPHANT
90D	SEES	C6A	BAR	F69	FAST
967	BEFORE				

Remarks:
Above are SSB-MPF's SPEECH vocabulary library, available in January 1982.

宏碁電腦股份有限公司
MULTITECH INDUSTRIAL CORPORATION

OFFICE: 977 MIN SHEN E. ROAD, TAIPEI, 105 TAIWAN, R.O.C.
TELEX: "19162 MULTIIC" and "23756 MULTIIC"
TEL: (02) 769-1225 (10 LINES)
FACTORY: 5, TECHNOLOGY ROAD III,
HSINCHU SCIENCE-BASED INDUSTRIAL PARK.
HSINCHU, TAIWAN, 300, R.O.C. TEL: (035) 775102 (3 LINES