LNW RESEARCH

SYSTEM EXPANSION USER MANUAL

LNW RESEARCH
P.O. Box 16216
IRVINE, CA 92714

PART NO. M22103-2

OCTOBER 1979

TABLE OF CONTENTS

		PAGE
SECTION 1:	INTRODUCTION	1
SECTION 2:	PARTS LIST	2
2.1	Parts List by Section	5
2.2	Parts List by Number	7
2.3	Composite Parts List	10
SECTION 3:	ASSEMBLY	12
3.1	General Assembly Notes	12
3.2	Specific Assembly Instructions	13
3.3	Inital Test	15
SECTION 4:	SYSTEM CONFIGURATION.	17
4.1	Installing Memory.	17
4.2	Connecting to the TRS-80*	17
4.3	Connecting to Centronic/Radio Shack Parallel Printer	17
4.4	Connecting to Minifloppy Drives	19
4.5	Connecting to the 40 Pin Screen Printer Bus .	19
4.6	Dual Cassette Configuration	19
4.7	Serial Interface Configuration	20
4.7A	Configuring Jumpers E1,E2,E3,E4	20
4.7B	Baud Rate Configuration	20
4.7C	Programming Parity, Word Length and Number of Stop Bits	21
4.7D	Connecting to the DB25 Connector J2	22
4.7E	Software Driver Programs	24

		PAGE
SECTION 5:	SYSTEM TEST	25
5.1	Memory Test	25
5.2	Minifloppy Test.	25
5.3	Parallel Printer Test.	25
5.4	Serial Interface Test.	25
5.5	Real Time Clock Test	26
5.6	Dual Cassette Control Test	26
SECTION 6:	PARALLEL TO SERIAL MODIFICATION	27
6.1	Modification Instruction	27
6.2	Test and Operation	29
SECTION 7:	IN CASE OF PROBLEMS	32
SECTION 8:	CIRCUIT DESCRIPTION	33
8.1	Memory Expansion	33
8.2	Minifloppy Disk Interface	33
8.3	Parallel Line Printer Port	34
8.4	Serial Interface	35
8.4A	Crystal Drivers and Dividers for Baud Rate Generation	35
8.4B	TR1602B UART	35
8.4C	EIA RS232C and 20mA Level Shifters and Drivers	35
8.4D	Handshake Latch	37
8.4E	Modem Status Buffer	37
8.4F	Configuration Sense Jumpers	37
8.4G	Decoding and Control Logic	37
8.5	Real Time Clock	39
8.6	Dual Cassette Port	39

PAGE

8.7 Power Supply 40

8.7A +5V Supply 40

8.7B -5V Supply 40

8.7C +12V Supply. 40

8.7D -12V Supply. 40

8.7E Overvoltage Crowbar 41

SECTION 9: APPENDIX. 42

TR1602B Data Sheet

Serial Interface Driver Listing

FD1771B-01 Data Sheet

SECTION 10: SCHEMATICS

****

WARRANTY 67

SECTION 1: INTRODUCTION

LNW Research thanks you for choosing the System Expansion Board to upgrade your Level II, 16k TRS-80* System. We believe that it combines the most desired features with the highest level of performance of any interface available.

SECTION 2: PARTS LIST

The following parts lists have been prepared to allow construction of the System Expansion Board according to your current as well as future needs. The modular design of the interface allows you to build only the sections that you need, thus, allowing a custom designed interface at the lowest possible cost. To make parts gathering easier, we have divided the parts list into three main sections.

The first list is entitled "Parts List by Section" and it lists the symbolic names (i.e. R11, C24, U20) of all the parts required for each circuit. A separate list is provided for the power supply, memory expansion, dual cassette relay driver, and those parts required for all sections.

The second list is entitled "Parts List by Number" and lists every part used in the System Expansion by symbolic name, value, and description.

The third list is called "Composite Parts List" which lists parts by value and the quantity required to build the entire System Expansion Board.

Provided for your convenience, also, are blank parts lists to allow you to create your final complete parts list. This is done by deciding which features you need (floppy controller, serial interface, etc.). Then starting with resistors, copy the symbolic name from the section you need, find it in the parts list by number and copy its value and description on your blank parts list. Place a check in the box provided on the parts list by number so that if a different section calls out for that part it will not be duplicated. Now go back to the list for the section you want and repeat the procedure with the next symbolic part number. If a part has the same value and description as a part you have already listed, simply add a comma and insert the new symbolic name after the one that is already there. Complete all the resistors for the sections you want before continuing on to capacitors. This will make for an easier-to-follow parts list when done.

Once you have completed listing all the symbolic names, values, and descriptions on the blank lists provided, count the symbolic names for each value and description and mark this number in the box marked QTY (quantity). Now you will know what quantity of that specific part you will need in building your interface.

PARTS LIST (Example)

Qty	Symbolic Names	Value/Description
4	R16, 17, 18, 19	150 ohm 1/4 watt

PARTS LIST

Qty.	Symbolic Names	Value/Description

PARTS LIST

Qty.	Symbolic Names	Value/Description

Section 2.1: Parts List By Section

REQUIRED FOR ALL SUPPLIES

T-1 Radio Shack Computer Wall Transformer

+5VDC SUPPLY

R-1,2,3,4,5,32
C-1,8,9,60,66,67
CR-1,5,6,10
Q-1
SCR-1
U62,66

Miscellaneous

2-T0220 Heatsinks (#276-1363)[1] (Ref U62,66)
1 Fuseholder (#270-739)[1]
F-I-2A Fast blow fuse

+12VDC SUPPLY

R-6,7,8,9
C-2,10,11
CR-7,8
Q-2
SCR-2
U-63,64

Miscellaneous

1-T0220 Heatsink (#276-1363) (Ref U63)
F-2-.75A Fast blow fuse

-5VDC SUPPLY

R-10
C-3,4
CR-2

-12VDC SUPPLY

R-11
C-5,6,7
CR-3,4
U-65

REQUIRED FOR ALL SECTIONS

C15-63,65 Bypass Caps,
R34-57,68,69 Termination Resistors

FLOPPY DISC CONTROLLER (+5,+12,-5)

R-12,13,14,15,16,17,18,19,27,28,29, 30,31,66
C-12,15,63
U-1,2,3,6,7,8,9,11,13,14,15,18,19, 20,21,22,23,29,30,31,36

Miscellaneous

Y-1

REAL TIME CLOCK (+5)

R-27,28,29,30,31
C-15
U-1,3,9,10,12,18,19,20,21,22,24,25, 29,30,31

Miscellaneous

Y-1

SERIAL INTERFACE (without 20mA or 110 Baud) (+5,+12,-12)

R-26,27,28,29,67
C-15
U-10,16,18,23,24,25,26,28,32,33,39, 40,41,51,52,61

Miscellaneous

Y-1

For 20mA option add R-23,24,25 and U-50

For 110 Baud option add U-17

Enclosed area not needed when used with LNW80.

[1]Radio Shack Part Number.

*If floppy section is not installed connect U23 pin 9 to ground.
Note: U14 must not be installed.

32K BYTE MEMORY EXPANSION
(+5,+12,-5)

R-58-65
C-14
U-11,29,30,31,34,35,36,37,38

Miscellaneous

16-16 pin DIP sockets

1st 16k RAM add U42-49

2nd 16k RAM add U53-60

LINE PRINTER INTERFACE (+5)

R-20,21,22
C-13
U-3,4,5,7,19,20,30,31,36

DUAL CASSETTE SWITCH (+5,+12)

CR-9
U-20,27,50
4 Pole Double Throw Relay +5V, 100mA Max, Coil Current

Section 2.2: Parts List By Number

RESISTORS

(1/4 watt, 5% unless other wise indicated)

☐	R# 1	3.3 Ω	1 watt	10%	(Radio Shack Part #(RS#)271-075)
☐	2	33	1/2 watt	10%	
☐	3	1k			
☐	4	8200			
☐	5	1k			
☐	6	10	1/2 watt	10%	
☐	7	100	1/2 watt	10%	
☐	8	1k			
☐	9	8.2k			
☐	10	220	1/2 watt	10%	
☐	11	22	1/2 watt	10%	
☐	12	10k			
☐	13	10k			
☐	14	1k			
☐	15	200k			
☐	16	150			
☐	17	150			
☐	18	150			
☐	19	150			
☐	20	4.7k			
☐	21	4.7k			
☐	22	20k			
☐	23	220			
☐	24	220			
☐	25	47			
☐	26	3k			
☐	27	150			
☐	28	680			
☐	29	680			
☐	30	1k			
☐	31	1k			
☐	32	3.3	1 watt	10%	(RS# 271-075)
	33	Not Used			
☐	34-45	220			
☐	46-51	1k			
☐	52	430			
☐	53	1k			
☐	54	430			
☐	55	1k			
☐	56	430			
☐	57	430			
☐	58-65	100			
☐	66	33			
☐	67	10k			
☐	68	220			
☐	69	1k			

CAPACITORS

(All caps are 25VDC ±20% unless otherwise indicated)

C#	1	10,000 ufd. electrolytic 16VDC
	2	3,300 ufd. electrolytic
	3	220 ufd. electrolytic
	4	.1 ufd. ceramic
	5	220 ufd. electrolytic
	6	220 ufd. electrolytic
	7	25 ufd. electrolytic axial
	8	6.8 ufd. tantalum
	9	.1 ufd. ceramic
	10	25 ufd. electrolytic axial
	11	.1 ufd. ceramic
	12	33 ufd. electrolytic axial 6VDC
	13	220 pf ceramic
	14	220 pf ceramic
	15	27 pf ceramic
	16-33	.1 ufd. ceramic
	34,35	6.8 ufd. tantalum
	36,38,40,42-52,54,56,58,61,62,63	-.1 ufd. ceramic
	37,39,41,53,55,57,59,60,65	-6.8 ufd. tantalum
	C66,C67	.1 ufd. ceramic
	64	Not Used

DIODES

CR#	1	4A 50PIV Inline Bridge Diode (RS#276-1146)
	2	1N5231B 5.1 5%
	3	1N4001 50 PIV 1A
	4	1N4001 50 PIV 1A
	5	6.2V 5% Zener IN5234B (500 mw)
	6	1N914 (or similar)
	7	14V 5% Zener (500 mw) IN5244B
	8	1N914
	9	1N914
	10	1N4001 50 PIV 1A

SCR's

SCR#1		6A 50VRMS SCR (RS#276-1067)
	2	6A 50VRMS SCR (RS#276-1067)

TRANSISTORS

☐	Q-1	MPU131 Programmable Unijunction Transistor
☐	-2	MPU131 Programmable Unijunction Transistor

INTEGRATED CIRCUITS

☐	U- 1	7438
☐	2	7438
☐	3	74LS367
☐	4	74LS175
☐	5	74LS175
☐	6	7438
☐	7	74LS123
☐	8	74LS240
☐	9	7492
☐	10	7493
☐	11	74LS08
☐	12	7490
☐	13	74LS175
☐	14	FD1771B-01 Western Digital
☐	15	74LS240
☐	16	74LS155
☐	17	7493
☐	18	74S04
☐	19	74LS155
☐	20	74LS14
☐	21	74LS74
☐	22	74LS74
☐	23	74LS08
☐	24	74LS161 or 74LS163
☐	25	74LS161 or 74LS163
☐	26	74LS175
☐	U-27	74LS00
☐	28	74LS367
☐	29	74S32
☐	30	74LS139
☐	31	74LS30
☐	32	74LS14
☐	33	74LS367
☐	34	74LS244
☐	35	74LS244
☐	36	74LS244
☐	37	74LS241
☐	38	74LS241
☐	39	74LS244
☐	40	TR1602-B Western Digital
☐	41	74LS30
☐	42-49	4116, 2117 or equivalent (Not 2116)
☐	50	75452 Dual Peripheral Driver
☐	51	1489 EIA Receiver
☐	52	1489 EIA Receiver
☐	53-60	4116, 2117 or equivalent (Not 2116)
☐	61	1488 EIA Driver
☐	62,63	7805 T0220 Regulator
☐	64	7812 T0220
☐	65	7912 T0220
☐	66	7805 T0220

Misc. Y1 4.000 MHZ Crystal
Wire 24" Solid Hookup wire 24 AW insulated
1-RS-232-C Connector PC Mount Right Angle
Male-Amp #206604-1, or #206604-2.
(or)Female-Amp #206584-1, or #206584-2
2-40 pin DIP IC Sockets
16-16 pin DIP IC Sockets
8-20 pin DIP IC Sockets
13-16 pin DIP IC Sockets
21-14 pin DIP IC Sockets
1-8 pin DIP IC Sockets
2-40 pin Edge Card Connectors (termination or solder)
1-(<) 12" 40 Conductor Ribbon Cable
1-Floppy Cable
1-5 Cond DIN Jack for TRS-80 XFMER
1-T-1 TRS-80 Computer Tranformer (Cat No. 4000007)
3-T0220 Heatsinks (RS#276-1363)
2-Fuseholders (RS#270-739)
1-2A Fast Blow Fuse
1-.75A Fast Blow Fuse

Section 2.3: Composite Parts List

RESISTORS

All resistors are in ohms 1/4 w 5% unless otherwise specified.

Description	Quantity	Symbolic Names
3.3 1w 10%	2	R1,R32
10 1/2w 10%	1	R6
22 1/2w 10%	1	R11
33 1/2w 10%	1	R2
33	1	R66
47	1	R25
100 1/2w 10%	1	R7
100	8	R58-R65
150	5	R16-R19,R27
220 1/2w 10%	1	R10
220	15	R23,R24,R34-R45,R68
430	4	R52,R54,R56,R57
680	2	R28,R29
1k	15	R3,R5,R8,R14,R30,R31,R46-51, R53,R55,R69
3k	1	R26
4.7k	2	R20,R21
8.2k	2	R4,R9
10k	3	R12,R13,R67
20k	1	R22
200k	1	R15

CAPACITORS

All capacitors are 20% 25V unless otherwise specified.

Description	Quantity	Symbolic Names
27 pfd ceramic	1	C15
220 pfd ceramic	2	C13,C14
.1 ufd ceramic	43	C4, 9,11,16-33,36,38,40,42-52, 54,56,58,61-63,66,67
6.8 ufd tantalum	12	C34,35,37,39,41,53,55,57,59,65,60,8
25 uf electrolytic axial lead	2	C7,C10
33 uf electrolytic axial lead 6V	1	C12
220 uf eletrolytic	3	C3,C5,C6
3300 uf electrolytic	1	C2
10,000 uf electrolytic 16V	1	C1

INTEGRATED CIRCUITS

Description	Quantity	Symbolic Names
74LS00	1	U27
74S04	1	U18
74LS08	2	U11,23
74LS14	2	U20,32
74S32	1	U29
74LS30	2	U31,41
7438	3	U1,2,6
7490	1	U12
7492	1	U9
7493	2	U10,U17
74LS74	2	U21,U22
74LS123	1	U7
74LS139	1	U30
74LS155	2	U16,U19
74LS175	4	U4,U5,U13,U26
74LS161 or 74LS163	2	U24,25
74LS240	2	U8,U15
74LS241	2	U37,38
74LS244	4	U34,35,36,39
74LS367	3	U3,U28,33
7805 T0220	3	U62,63,66
7812 T0220	1	U64
7912	1	U65
FD1771B-01	1	U14
TR1602-B Western Digital	1	U40
MK4116,2117 or equivalent	16	U42-49,U53-60
75452 Dual Peripheral Driver	1	U50
1488 EIA Driver	1	U61
1489 EIA Receiver	2	U51,U52

DIODES

Description	Quantity	Symbolic Names
Inline Bridge diode 4A, 50 PIV (RS#276-1146)	1	CR1
1N5231B: 5.1v ± 5% zener	1	CR2
1N5234B: 6.2v ± 5% zener	1	CR5
1N5244B: 14v ± 5% zener	1	CR7
1N914	3	CR6,CR8,CR9
1N4001	3	CR3,CR4,CR10

MISCELLANEOUS SEMICONDUCTORS

Description	Quantity	Symbolic Names
6A 50v RMS SCR (RS#276-1067)	2	SCR1,2
MPU131 Programmable Unijunction Transistor	2	Q1,2

SECTION 3: ASSEMBLY

Due to the density and complexity of the System Expansion Circuit Board, etch and circuit pad widths are quite small and very delicate. Good soldering and assembly practices must be followed explicitly. Use high quality electronic solder, or preferably multicore, resin core solder. Do not use greater than a 30 watt pencil iron, constantly keeping the tip cleaned and tinned. Avoid using excess heat on the board. If parts must be removed while heating the component with the iron, gently tug or rock the lead out of the hole. Since the holes are plated through, the plating will be removed with the component lead if care is not exercised.

Section 3.1: General Assembly Notes

Due to the modular design of the System Expansion, a detailed step-by-step Assembly Manual would be impossible and since the assembly of the circuit board assumes a certain degree of ability on the part of the builder, topics, such as: How to install a resistor, transistor, or I.C., will not be discussed. What the assembly instructions will include are general and specific construction hints that we felt would be useful in making your expansion board as easy and simple to build as possible.

Although sockets for the I.C.'s are not required, we feel it is imperative you use them. The circuit pads are delicate and the removal of I.C.'s can cause serious damage to the board. For this reason, we make the following recommendations:

Use high quality I.C. sockets, inspect them visually for defects before installation, and take great care not to bend pins under while inserting the sockets into the board. Before soldering the pins of the socket, make sure that all the pins make it through the holes. All components (except for male right angle RS232 connectors) are to be installed on the component side with the silkscreened legend.

When installing the transistors, SCR's and IC Regulators, make sure that the correct part is being installed the proper way. Also, make sure all diodes, electrolytic and tantalum capacitors have been installed with the proper polarity.

We, at LNW Research, cannot possibly recommend parts substitution. Let it suffice to say that if the parts called out for in the parts list are used exclusively, flawless operation will result. We cannot guarantee operation if substitute parts are used. We also realize that there are those who for one reason or another will find it necessary to substitute parts. The following paragraph is written for these individuals:

There are some common sense guidelines to follow when you are looking to substitute parts. Make sure you consider all the possible differences the part may possess compared to the part called out originally. For example: Do not substitute a 74123 for a 74LS123 at U7. Although, speed and low power are not considerations, the fact is, a 74123 cannot use as high a value of a timing resistor. If the 74123 part is substituted, strange floppy motor activity will surely result. Be sure to consider power consumption when substituting IC's. If 74TTL was substituted for 74LSTTL at every spot on the board, it would draw more than three times the power from the five volt supply. In the worst extreme, some parts are not pin for pin compatible between 74TTL and 74LSTTL families.

Section 3.2: Specific Assembly Instructions

Before installing parts on the circuit board, check the circuit board and RS232 connector mounting holes. These holes may need redrilling or enlarging to accommodate your mounting requirements. If drilling is required for component holes, be sure that you take every precaution to protect the board from accidental damage, and solder both the component and solder side of the PC Board.

Begin assembly by installing the IC sockets. Install the resistors (except R34-57), capacitors (except C66,67), diodes, SCR's, transistors, and IC regulators U62-66. Next, install the fuse holders, fuses, and power connector at J1. The right angle RS232 connector can be installed in two different fashions. If the PC mount connector is a male, it mounts underneath the circuit board (solder side) and the leads are soldered on the component side. If your connector is a female, it will mount on the top of the board (component side) and will be soldered from the solder side. Most connectors have the pins numbered on the plastic body near the right angle pins. Check to make sure they correspond to the pin numbers on the board.

The termination resistors at R34-57 are to be installed standing straight up. Before soldering them to the board, insert R46-57 in their designated spots (pads at connector J3). Solder a bus wire to the free end of each resistor and connect the bus wire to the hole near R69 (+5V, unmarked). Now solder the individual resistor leads to the circuit board. Trim excess lead lengths above the resistors and on the soldering side. Repeat this procedure with R34-45 but connect the bus wire to the point marked GND near pin 39 of J3. Refer to the drawing on the next page.

The instructions in the enclosed area need not be followed when used with the LNW80.

Now install the following jumpers:

1. Jumper from one of the points marked GND (ground) near J3 to the point marked GND at C33 (near U26). This jumper, as with the others, can be done on either the component side or the solder side.

2. From the other point marked GND at C33 (near U33) to the point marked GND at C65 (bottom of the memory array).

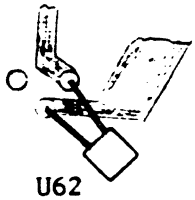
3. From JP13 (near C1) to JP14 (near U9).

Do not install any other jumpers at this time. Do not install the IC's at this time.

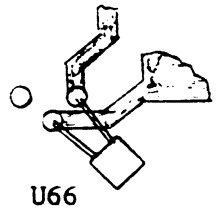
4. Install the TO220 heatsinks at U62, U63 and U66.

5. Install Y1. The 4.0 MHZ crystal, leaving ½" lead length.

6. Install .1uf ceramic capacitors C66 and C67 between the IN and GND designation of the +5V regulators at U62 and U66. C66 and C67 should be installed on the solder side of the board. Note the drawing below.

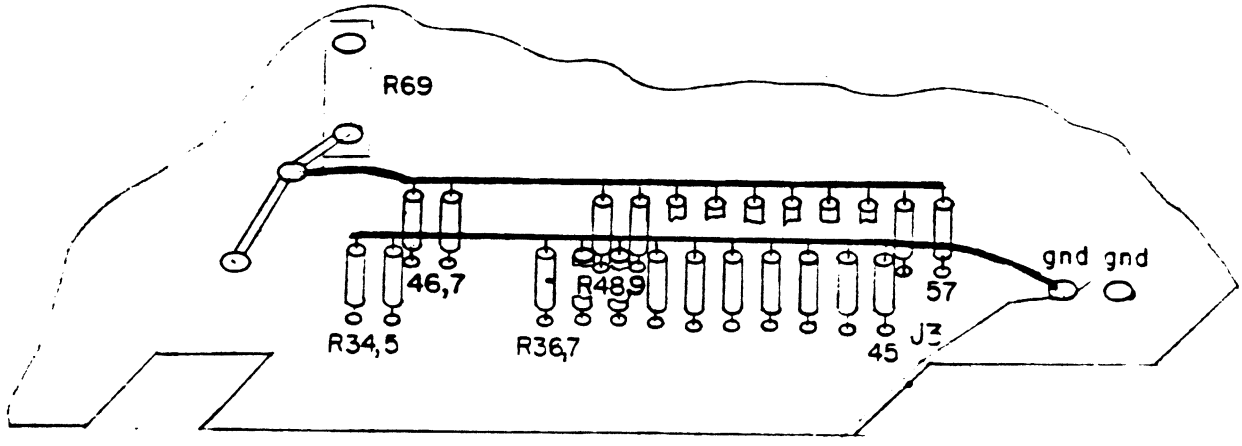


U62
Solder Side



U66
Solder Side

Before preceding to the section on Test and Operation, inspect your completed board carefully. Check for cold, unsoldered, or shorted connections. Also, check for stray component leads that are shorting or that haven't been cut off. Double check to make sure that IC's, diodes electrolytic and tantalum capcitors, SCR's and transistors have been installed correctly.



TERMINATION RESISTORS

Section 3.3: Initial Test

This section describes the intial power up procedure and tests.

Care should be taken to exercise the following steps to ensure a successful interface:

1. Supplies that are being used (page, 5 , Parts List by Section) should be measured to guarantee proper DC voltage. The table below indicates voltage measuring points with reference to ground.

Voltage	Measurement Points
+ 5V	JP1,JP3
+12V	JP11
- 5V	JP7
-12V	JP9

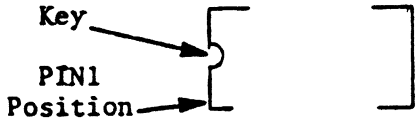
2. When the above DC voltages have been checked out to be correct, add the jumpers for the appropriate supply. Caution: Soldering should never be done with the power on!

Voltage	From	To
+ 5V	JP1	JP2
+ 5V	JP3	JP4
+12V	JP11	JP12
- 5V	JP7	JP8
-12V	JP9	JP10

3. Apply power to the System Expansion Interface and verify the voltages being used are correct.

Location	Voltage
C61 near U14PIN2	- 5V
C65 near U60PIN7	- 5V
C62 near U30PIN9	+12V
C59 near U60PIN1	+12V
C41 near U48PIN8	+12V
C25 near U25PIN9	+ 5V
C33 near U33PIN9	+ 5V
C17 near U2PIN16	+ 5V
C35 near U34PIN20	+ 5V
C43 near U40PIN1	+ 5V
C63 near U51PIN7	-12V

4. Turn the power off the System Expansion Board and install the IC's called out for in the Parts List. Make sure the pins are not bent under when inserting the IC's into the sockets. The silk screened key indicates the PIN1 position as shown below.



SECTION 4: SYSTEM CONFIGURATION

This section describes in detail how to connect the TRS-80, Parallel Printers, and Minifloppy Drives to the System Expansion Board.

It also shows how to install RAM and configure Printers and Modems to the Serial Interface. Connecting accessories to the Screen Printer Bus and the Cassette Relay Driver are also discussed.

Section 4.1: Installing Memory

Memory expansion may be upgraded in three increments. The first 16k byte should be installed in the TRS-80* keyboard and the remaining two 16k bytes may be installed in the System Expansion Board.

The first 16k bytes installed in the System Expansion Board should be located at U42 through U49, the lower bank.

The second 16k bytes should be installed in locations U53 through U60, the upper bank.

Section 4.2: Connecting to the TRS-80*

Both J4 and J3 may be utilized for the computer keyboard connection. Figure 1, Cable 1, shows the interfacing cable. Figure 2, TRS-80* Connection, show the actual connection of the TRS-80* to the System Expansion Board. When connecting to J3 with the cables down, the System Expansion Board should have the solder side up. when connecting to J4 with the cable down, the System Expansion board should have the component side up. When properly connected, there should be no twist in Cable 1.

If you choose to use the solder type card connectors in constructing of Cable 1, make sure that the pin numbers on the computer connector match the silkscreened numbers at J3 or J4.

Section 4.3: Connecting to Centronic/Radio Shack Parallel Printer

Radio Shack Printer Cable should be used when connecting to the Centronic/Radio Shack Parallel Printers. Care should be taken to match the silkscreened pin numbers on the System Expansion Board to the edge card connector.

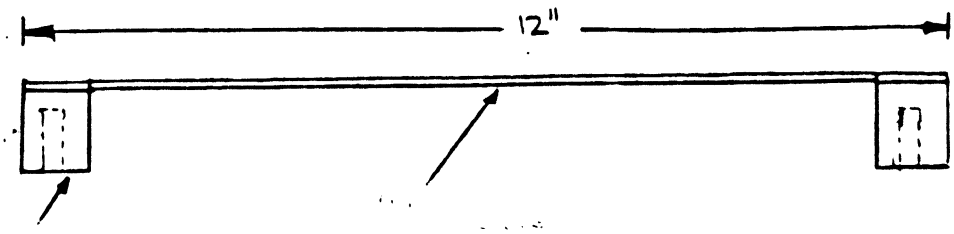


FIGURE 1. CABLE 1

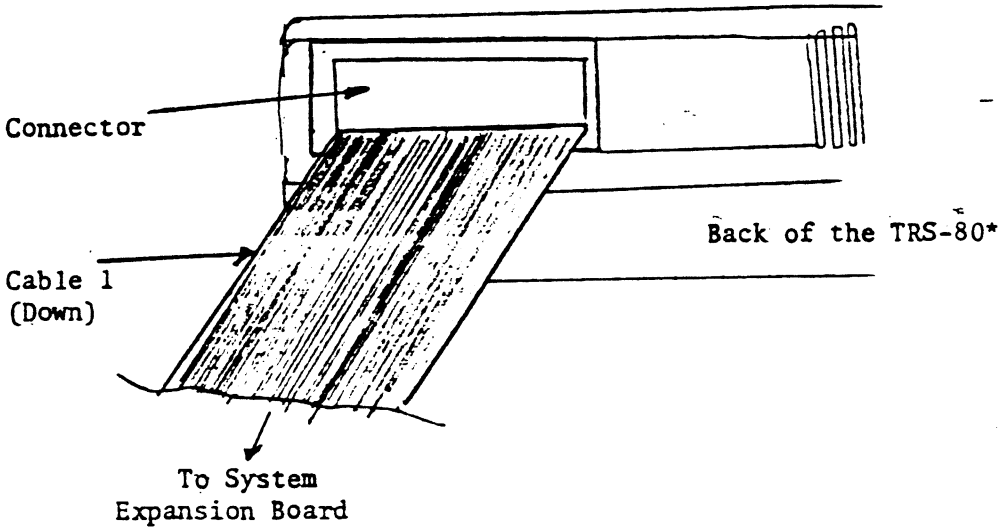


FIGURE 2. TRS-80* CONNECTION

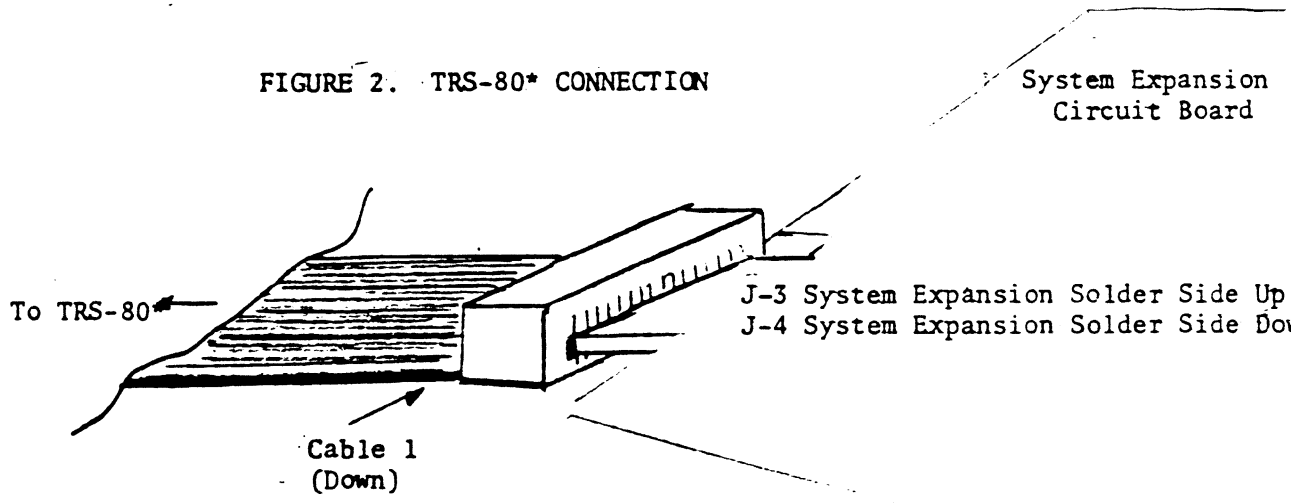


FIGURE 3. SYSTEM EXPANSION CONNECTION

Section 4.4: Connecting to Mini-floppy Drives

Only the mini-floppy disk that has been configured for use on the TRS-80* system will be compatible with the System Expansion Board. Care should be taken to match the sikscreened pin numbers on the System Expansion Board with the numbers on the edge card connector.

Section 4.5: Connecting to the 40 Pin Screen Printer Bus

Either J3 or J4 is used to connect between the TRS-80*, and the System Expansion Board.

The connector that is not used can be connected to devices designed to interface directly to the 40 pin bus. Screen printers, printers, S-100 interfaces, color graphic boards and back-plane systems are examples of the devices which may connect to the System Expansion Board Screen Printer Bus (J3 or J4). Since these devices vary in function and electrical characteristics we cannot describe in detail their compatibility. We will point out a few things which can cause problems:

1. Termination Resistors-If the device has termination on the cable input, the termination resistors R34-57,68 and 69 may or may not be needed on the System Expansion Board. The usual procedure is to terminate the last stage connected (i.e. device farthest from the TRS-80*) but experimental results will be definitive.

2. Conflicting Addresses-If the device was designed to not operate properly with the expansion interface, it will not function with the System Expansion Board. Beware of conflicting memory and port addresses. Consult the specific manufacturer's literature and the circuit description section of this manual for further information.

Section 4.6: Dual Cassette Configuration

The relay connectors should be wired as shown on Page 1 of the System Expansion schematic.

Section 4.7: Serial Interface Configuration

In order to operate serial devices from the serial interface, several jumpers must be configured on the System Expansion Board:

1. Configuring RS-232-C interface as Data Terminal (DTE) or Data Communications Equipment (DCE):

   --Jumpers at E1,E2,E3,E4

2. Configure Baud Rate:

   --Jumpers at RX,TX,a-h

3. Program Parity, Word Length, and Numbers of Stop Bits:

   --Jumpers at E5,E6,J,K,L,M,N,P

The details of each of these jumper configurations are as follows:

Section 4.7A:Configuring Jumpers E1,E2,E3,E4

There are two main classifications of Serial Interface devices- Data Terminal and Data Communication Equipment. Both types can send and receive serial data but the distinction between the two allows one type to send on the same line as the other type receives, and vice versa. Teletypes and Serial Printers are generally classified as Data Terminal Equipment (DTE) while modems are defined as Data Communications Equipment (DCE). Therefore, when connecting the serial interface to serial printers (DTE), the serial interface must be configured as Data Communications Equipment (DCE). When connecting to modems (DCE), the serial interface must be configured as a Data Terminal Device (DTE). Jumpers at E1,E2,E3, and E4 are provided for this purpose:

Device to be Interfaced (Type)		Jumper Serial Interface (Type)	
1. Serial Printers	(DTE)	E3 to E4, E1 to E2	(DCE)
2. Teletypes, Decwriter etc.	(DTE)	E3 to E4, E1 to E2	(DCE)
3. Modems	(DCE)	E1 to E4, E2 to E3	(DTE)

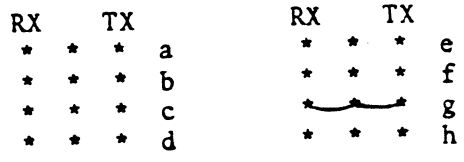
Section 4.7B:Baud Rate Configuration

The baud rate jumpers (RX,TX,a-h) near U10 consist of two groups of twelve (12) pads with the markings RX and TX above. The center pads of the unmarked columns supply the eight different baud frequencies. To select

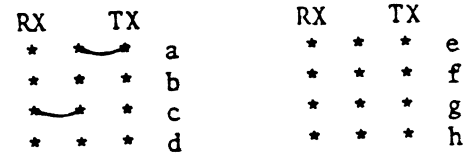
the baud rate for transmit (usually the same as baud rate for receive), jumper from the center column pad of the row (a-h) to TX (transmit pad). For receive, jumper from center column pad (a-h) to the RX (recieve) pad. The following table list the baud frequencies with the corresponding letters:

A - 9600 baud
B - 4800 baud
C - 2400 baud
D - 1200 baud
E - 110 baud
F - 150 baud
G - 300 baud
H - 600 baud

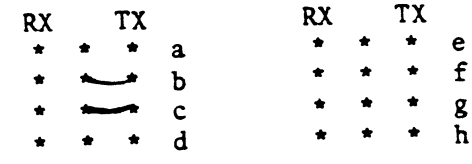
Do not jumper two center pads to any RX pad or jumper two center pads to any TX pad. The following figure shows two correct configurations and one incorrect configuration:



Correct Configuration
Set for 300 baud Transmit
300 baud Receive



Correct Configuration
Set for 9600 baud Transmit
2400 baud Receive



Incorrect Configuration
Both 4800 baud and 2400 baud are shorted together.

Section 4.7C:Programming Parity, Word Length, and Number of Stop Bits

Some serial devices transmit and receive without parity; others with even or odd parity. Word length might be 5,6,7, or 8 bits and the number of stop bits may be 1, 1½, or 2 for the specific device being interfaced.

The UART in the serial interface must be programmed for the above functions. The software driver programs do configure the above functions. To allow the user the ability to change the above configuration with jumpers whenever these parameters are changed, the software drivers program reads the status of the configuration jumpers and utilizes this information in initializing the UART. The configuration jumpers (near U28) consists of wires connecting the points J,K,L,M,N, and P to either E5 (+5V, Logic "1") or E6 (OV, Logic "0"). The following chart describes these various configurations.

Function	Condition	Jumper K to Jumper E5
Parity	Inhibited	K — E5 J — Don't Care
Parity	Even	K — E6 J — E5
Parity	Odd	K — E6 J — E6
Word Length	5 Bits	M — E6 P — E6
Word Length	6 Bits	M — E5 P — E6
Word Length	7 Bits	M — E6 P — E5
Word Length	8 Bits	M — E5 P — E5
Stop Bits	1	N — E6
	2	N — E5

NOTE: For a five (5) bit word length, when selecting two (2) stop bits, the actual number of stop bits is 1½ stop bits.

Section 4.7D:Connecting to the DB25 Connector J2

Except for RS232 Send (Pin 3) and RS232 Receive (Pin 2) which are jumper selectable, the rest of the RS232 interface lines on J2 are configured as "Data Terminal Equipment." This allows all the handshaking required when interfacing to a modem. Since RTS (Pin 4) and DTR (Pin 20) are also driven by RS232-C Teletypes, Decwriters, and other Data Terminal Equipment, conflicts may result when the Serial Interface is configured as a DCE.

Make sure when connecting to the above mentioned equipment, the RTS and DTR lines are not connected to the Decwriter or Teletype (in the DB25 cable). When using a Decwriter or Teletype as a serial printer, the RTS, DTR line are not used. They are used only when the Teletype or Decwriter is connected to a modem. The illustration on the following page shows the required interconnection for modems, printers and teletypes.

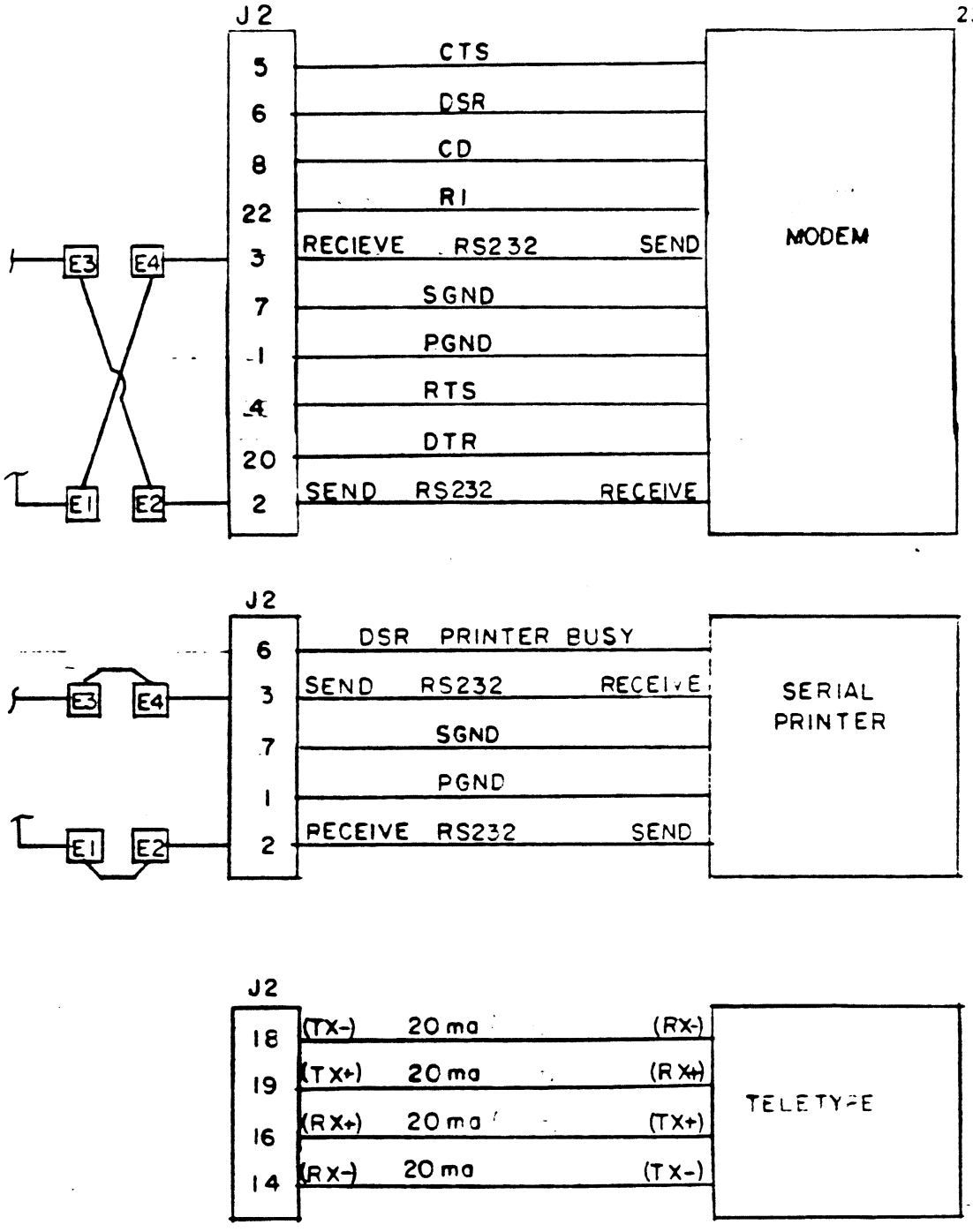


FIGURE 4.
SERIAL INTERFACE CONFIGURATION

Section 4.7E:Software Driver Programs

After the configuration jumpers have been set according to the specific needs of your system and your serial device connected to your interface, software driver programs must be used to:

1. Reset the UART.
2. Read in jumpers at J,K,L,M,N,P.
3. Program the UART based on the jumpers (2 above) for parity, word length and number of stop bits.
4. Drive the serial interface inputting and outputting data through the UART's Registers, the Handshaking Latch and the Modem Status Buffer.

The software listings supplied in the appendix (Section 9.3) do all the above. The Basic Serial Printer Program allows the use of a serial printer with handshaking. This Level II Basic (or Disk Basic) program pokes a machine language program into RAM starting at 7FØØH. Since large disk basic programs will conflict with this address, it may be necessary to change the program so that it will load at a higher location.

If your printer does not support handshaking, change Line #110 to 110 DATA 219,232,203,119,0,0,219,234.

The Serial CRT Terminal Program allows the TRS-80 to be used as a CRT Terminal with communication to a modem or other serial device through the serial interface. The source program can be assembled or the binary can be entered into memory by using Debug.

SECTION 5: SYSTEM TEST

This section describes some simple test to check the operation of the System Expansion Board. These tests are not definitive, but give a general indication that the system is working properly.

Section 5.1: Memory Test

For systems with 16kb of memory in the keyboard and 16kb of memory in the System Expansion:

1. Depress the 'break key' while powering up the TRS-80*.
2. ? MEM
   The computer will respond with a number greater than 30,000.

This number will indicate the available memory space. For systems with 16kb of memory in the keyboard and 32kb of memory in the System Expansion the reply to ? MEM should be a number > 48,000.

Section 5.1: Minifloppy Test

A good test is to try it with a minifloppy drive. The following steps should be followed for a proper power up sequence:

Connect a minifloppy drive cable to J6. Apply power to the drive and the System Expansion. Insert a write protected DOS diskette (write protect tab on). Next power up the TRS-80*, at this time the drive should be selected and motor on the drive should be activated. The computer should reply with DOS ready. A good test of the write capability is to make a back-up copy of a DOS Diskette. There are several types of TRS-80* compatible DOS available, so follow the DOS manual for the actual commands.

Section 5.3: Parallel Printer Test

Connect the cable to the printer according to Section 4.3. While in Basic, try a LPRINT command or enter a simple basic program and try a LLIST command. These basic commands will output to the parallel printer port.

Section 5.4: Serial Interface Test

Either key in the Serial CRT Terminal Program in Section 9.3 Serial Interface Driver Listings under debug or key in the Source Listing and assemble the program to generate the binary program.

When running the Serial CRT Terminal Program, the Jumpers E1 and E3 should be shorted together. This will allow the send data to be read back into the TR1602B UART. What is typed on the keyboard will be displayed on the CRT.

Section 5.5: Real Time Clock Test

While under DOS, use the clock command to display the real time clock.

The 'TIME' command is used to set the real time clock. The CMD"T" will stop the clock (disable interrupts); a CMD"R" will enable interrupts which will start the real time clock.

Section 5.6: Dual Cassette Control Test

Apply the ohm meter at the minus (-) pad of CR9 and GND, a reading of above 500 ohms should be indicated on the ohm meter. Under the Basic Program type:

```
CLOAD #-2, "A"
```

The ohm meter should now indicate a reading of below 500 ohms.

SECTION 6: PARALLEL TO SERIAL MODIFICATION

This special modification allows the use of a serial printer in place of the parallel printer for all applications without requiring serial driver programs in RAM and without the device control block driver address being changed. This modification is useful in applications where software supports only the Radio Shack/Centronics parallel printer. In order to use this modification, the serial printer (or teletype) must have "Auto-Linefeed" (must be able to recognize a carriage return and automatically generate a line feed). Most serial printers have this capability and many teletypes and decwriters have this capability as an option. This modification can be configured for printers with or without handshaking.

A switch is used to select the Serial Interface Port Addressing so just the flip of a switch and the Serial Interface is back to its standard configuration. All that is required to bring the Parallel Printer Port back to it's original configuration is to disconnect the RS-232-C device from J-2 (handshaking) or change one jumper (without handshaking).

A Serial Printer Initialization Program (listing supplied in Appendix 9.3) must be run each time the System Expansion is powered up to initialize the UART in the Serial Interface. After the UART has been initialized, the TRS-80* can be turned off, any software run, and as long as the device control block driver address (see Appendix 9.3, Serial Printer Driver Program) has not been changed from the standard Parallel Printer value, the LPRINT and LLIST commands will output to the Serial Printer.

Section 6.1: Modification Instructions

Parts Required

1-DPDT miniature toggle switch (S1)
3½ ft-30ga solid insulated wire
1 ft -7 conductor ribbon cable (actual length will depend on location of S1)

Etch Cuts

When cutting the etch on the circuit board, be careful not to damage any other traces of etch. Use a sharp blade and refer to the following drawing when making these two etch cuts.

1. Solder side between U40-16 and feedthrough.

2. At feedthroughs near U26 and U18.

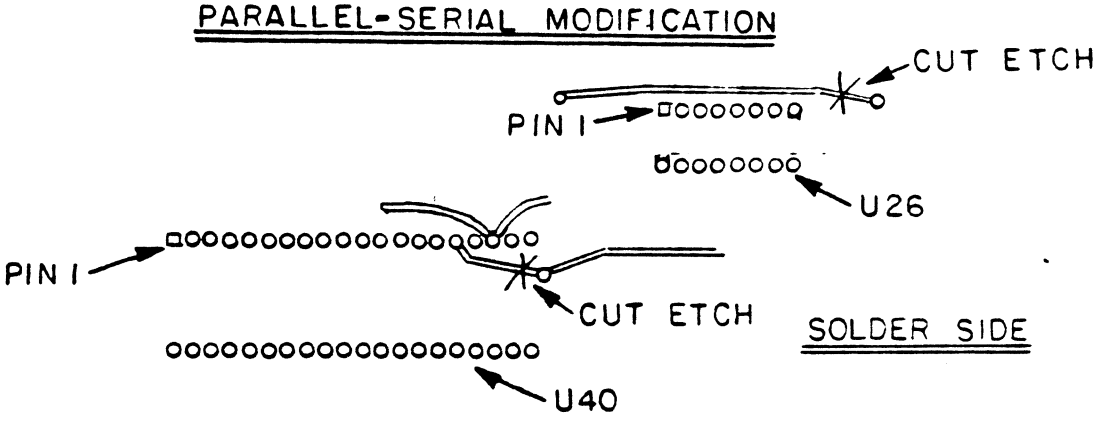


FIGURE 5.

Depending whether your printer has handshaking, printer busy connected-pin6 of J2 (DB25 connector) DSR, or not will determine which of the following jumpers are to be installed:

With Handshaking-(Printer busy connected to pin6, DSR, of the DB25 connector at J2)

Jumper	Location
3"	U32-11 to U33-4

Without Handshaking-If your printer (teletype) does not have handshaking (i.e. nothing connects to DSR pin6 of J2) install the following jumper:

Jumper	Location
1"	U32-11 to U32-7 (GND)

Jumpers

Using 30 ga wire, jumper the following locations:

Wire Length	Jumper Location
7"	U40-18 to u18-11
10"	U40-22 to U1-10
½"	U1-10 to U1-13
1"	U1-9 to U1-12
9"	U1-12 to U32-10
3"	U1-8 to U3-2
3"	U1-11 to U3-6

Now using the figure on the next page as a reference, wire the DPDT switch S1 using the 6 conductor ribbon cable. The length of the ribbon cable should be selected on the basis of the location of the switch S1.

S1 pin 1 to U16-12
S1 pin 2 to U40-23
S1 pin 3 to U40-16
S1 pin 4 to U16-5
S1 pin 5 to U18-10
S1 pin 6 to U 5-9
S1 case to U33-8 (GND)

Section 6.2: Test and Operation

Refer to Section 4.7 on how to connect your serial printer to the RS232/20mA serial interface. Set S1 (Printer/Modem) to PRINTER.

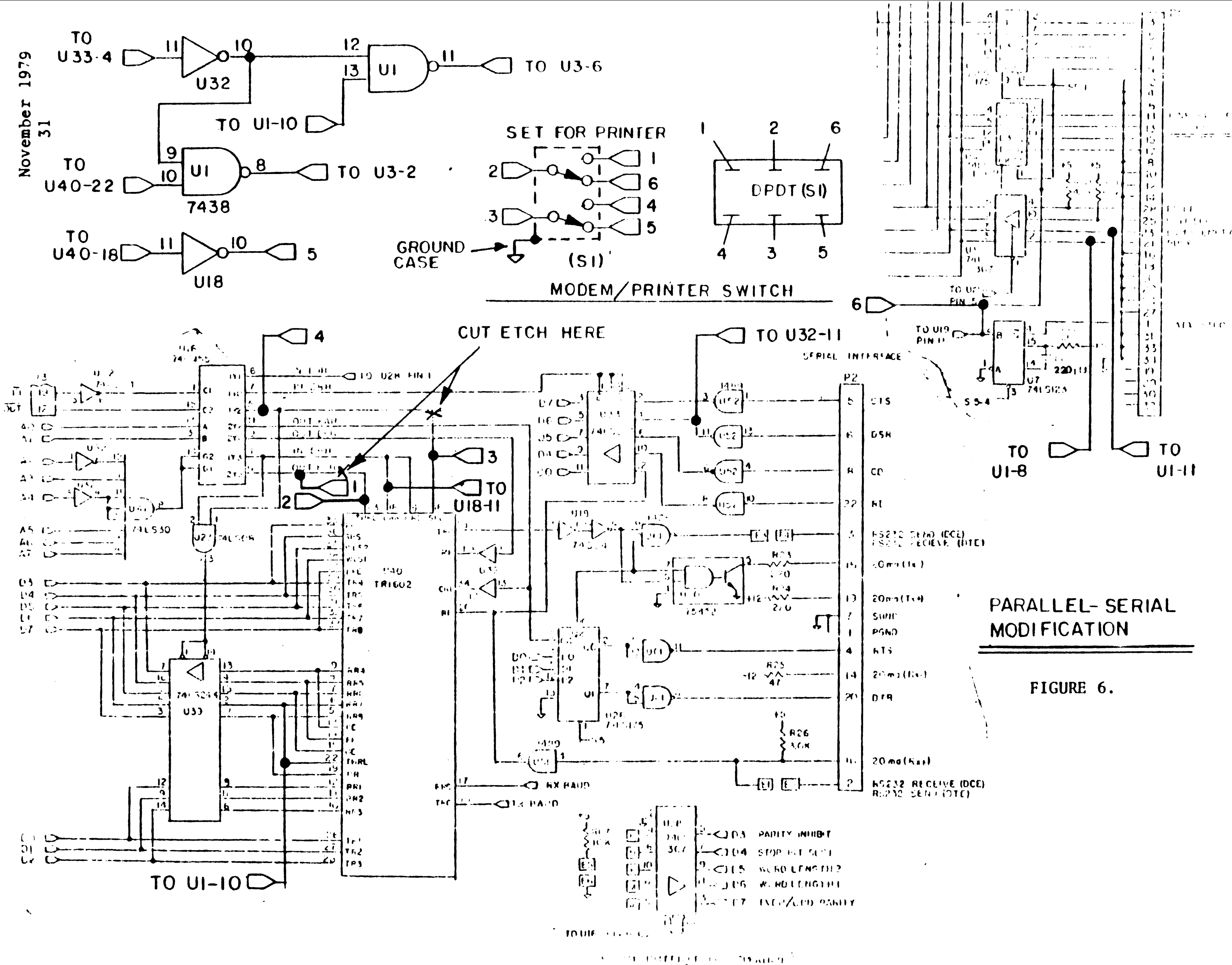
In order to initialize the UART with Parity, Number of Stop Bits, and Word Length, configure the serial interface as described in Section 4.7 on Serial Configuration. Then use the Printer Initialization Program to initialize the UART. To run this program, either reassemble the source or enter, using debug, the binary. After the program runs, it jumps back to the entry point of DOS (402D-H). If you would like to change that location, simply substitute your entry location for the one currently used (remember--last byte of the address comes first in the binary).

Test

Now with the printer set for Auto Linefeed, load basic and test your interface with the LPRINT command.

Type in LPRINT "TEST" <Enter>

The printer should have printed the letters TEST, returned to the start of the line and advances the paper one line. If the printer did not print and the keyboard locks out, recheck your wiring of the MOD. If the keyboard is not locked out, check the wiring to your printer and check to make sure your serial interface and printer are both configured properly. If the printer prints strangely, chances are the baud rate, number of stop bits, word length and/or parity are improperly set. Refer to the Serial Configuration Section of this manual for more information.



PARALLEL- SERIAL MODIFICATION

FIGURE 6.

SECTION 7: IN CASE OF PROBLEMS

The following is a list of common problems that might be encountered. As always, all problems cannot be anticipated; but, by isolating the fault most problems can be found easily.

LIST OF COMMON PROBLEMS	POSSIBLE CAUSES
Floppy motor stays on intermittently	U7 must be a 74LS123
Floppy disk operation intermittent	C61 not installed
Intermittent memory operation	Termination resistors not installed; Jumper from GND at J3 to JP13 not installed; C14 missing or wrong value; Capacitors on memory not installed.
Floppy inoperative, Baud rate clock missing	U18 must be a 74S04
Intermittent program "crash"	Inductive load switching on A.C. power line. If changing the A.C. outlet is not possible, try an A.C. surge/noise filter.
Serial Interface runs Serial CRT Terminal Program, but, communication to other Serial devices is incorrect.	Configuration jumpers or baud rate improperly set.

3. Checks for desired section, check ID field and locate it's data address mark.

4. Track number of the current read-write head position is kept accounted.

The interface to the processor is accomplished through the eight Data Access Line (DAL) and the associated control signals.

When reading for the DAL, the address decoder U19pin4 (37EC $\overline{\text{READ}}$) will be low enabling U8 and U15 to buffer data from U14 DALØ-DAL7 to the data bus DØ-D7. When writing from the data bus to DAL, the address decoder U19pin12 (37EC $\overline{\text{WRITE}}$) will be low enabling U8 and U15 to buffer data from the data bus DØ-D7 to the Floppy Controller DALØ-DAL7.

The least significant address AØ, A1 is decoded by the Floppy Disk Controller U14 to interpret the selected registers of the read and write operations. These registers are decoded as follows:

A1	AØ	Read (RE)	Write (WE)
Ø	Ø	Status Reg.	Command Reg.
Ø	1	Track Reg.	Track Reg.
1	Ø	Sector Reg.	Sector Reg.
1	1	Data Reg.	Data Reg.

The interrupt request of the Floppy Disk Controller (FDC) U14pin39 indicates the completion or termination of any operation. This interrupt signal (INTRQ) presets the flip-flop U22A presenting a high to U1pin4 and 5, which is reset by reading the FDC Status Register. Reading from 37EØH will reset the interrupt signal Int by clocking a low at the output of flip-flop U22A.

The FDC U14 requires a 1 MHz clock generated from the 4MHz main clock circuit. U9 and U22B are "divide-by-two" circuits which divided the 4 MHz down to 1 MHz.

Drive Selection through Data Line DØ-D3 is clocked into U13 by the signal 37EØ write. This also triggers the one-shot (74LS123) U7A generating the motor on signal. The drive selection is only activated when the motor on signal from U7Apin5 is high.

When U7pin5 (motor on signal) is low, clearing U13, a high is generated at U11pin8. This high at U11pin8 is inverted by U22pin10 providing a low command and the floppy status is ready.

Most users need not worry about programming the FDC when utilizing TRS or other compatible TRS-80* type DOS. There will be knowledgeable users who will program the FDC, an understanding of the Western Digital's FD1771A/B-01 Data Sheet (Appendix, Section 9.3) is manditory.

The drive configuration and eable positioning are described in Section 4, system Configuration.

SECTION 8: CIRCUIT DESCRIPTION

The circuit description is supplied as an aid in trouble-shooting or understanding the System Expansion board.

Section 8.1: Memory Expansion

Address lines A0-A13 are received by U37 and U38, octal buffers/line drivers. These receivers have Hysteresis at inputs to improve noise margins. The $\overline{MUX}$ line selects the row and column addressing. The row address strobe ($\overline{RAS}$) is buffered to all of the RAMS while the column address signal is gated by U29 with the 48k $\overline{RAMEN}$ and 32k $\overline{RAMEN}$. The 48k $\overline{RAMEN}$ and 32k $\overline{RAMEN}$ signals are decoded by U30 the address decoder. The 48k $\overline{RAMEN}$ signal will be low between the hex address range of C000-FFFF. The 32k $\overline{RAMEN}$ signal will be low between the hex address of 8000-BFFF.

The data bus is buffered by U34 and U35 octal buffer/line drivers. These buffers will pass data from the memory onto the data bus when Pin 1 of U34 and U35 is low. The memory data are enabled by Pin 19 of U34 and U35, this pin is always low enabling data from the data bus to the data input of the memory array.

The series terminations R64 through R65 greatly reduces the signal reflections generated by interfacing TTL with MOS inputs. These series terminations greatly reduce the characteristic "signal ringing" resulting in a quieter memory array.

Section 8.2: Mini Floppy Disk Interface

The function of interfacing the TRS-80* computer to a minifloppy drive is performed primarily by the Western Digital's FD1771B-01 Floppy Disk Formmatter/Controller chip.

This MOS/LSI device performs much of the housekeeping involved in reading and writing data to and from the disk. Some of the internal features include:

1. Cyclic redundancy check and generation for error checking.

2. Internally separates disk head output into data.

Section 8.3: Parallel Line Printer Port

The System Expansion contains an interface to the Radio Shack/ Centronic Printer. This Parallel Printer Interface consists of an eight bit output port and a four bit input port.

This I/O port is accessed by either writing or reading from memory address 37E8H.

When a read to memory address 37E8H, the following data bit indicates these printer status:

Data Bit	Printer Status
D 7	Printer Busy
D 6	Paper Empty
D 5	Unit Select
D 4	Fault

The Radio Shack's parallel printer has wire ORed internally, the printer busy status, and the paper empty signal.

When using the Radio Shack/Centronic Printer, only one of these two status bits, D6 or D7, needs to be checked. The printer busy indication is issued by asserting a logic one. When this occurs, the paper empty status will also be a logic one. The printer program only needs to check one of the two status bits for a logic zero at the data bits, D6 or D7, prior to outputting to the printer data latch. The unit select and fault status bits are not used by the Radio Shack's printer.

A write to memory location 37E8H will load the output latch U42 and U43 to generate a signal called "Data Strobe." This signal "Data Strobe" will transfer the data from the output latch U42 and U43 to the line printer's internal data buffer.

The "Data Strobe" signal will be a low-going pulse of approximately 1.5 microseconds.

The Radio Shack's printer is set up to recognize the following control characters for the line feed and carriage return:

Character	Function
ØAH	Line Feed
ØDH	Carriage Return

When either one of these control characters are received by the printer, the printer will assert a logic one bit at the printer busy status (J5pin21).

Section 8.4: Serial Interface

The Block Diagram (Figure 7) outlines the major sections of the Serial Interface. For the following circuit description, use the schematics along with the Block Diagram to aid in visualizing the circuit theory.

Section 8.4A:Crystal Drivers and Dividers for Baud Rate Generation

Crystal Y-1 has U18 as a driver and is divided by counters U24,25,10,17,9 and 12. Part of U9 is used to drive a divider for the Floppy Controller and U12 is used to drive the Real-Time Clock. In order to provide the receive and transmit baud clocks for the UART, the 4 MHz ouput of U18 must be divided down. U24 and U18 divide the crystal frequency by 13 (U24pin11) which is further divided by 16 (U25) to provide the upper 4 baud frequencies (9600,4800,2400,1200). The 1200 baud tap feeds U10 where the next three baud frequencies (600, 300, 150) are generated. U25pin12 (2400 baud) is divided by 11 at U17 and U10pin14 (÷ 2) to provide the 110 baud. Baud rate is programmed by jumpering A,B,C,D,E,F,G, or H to the RX and TX line. These RX and TX lines are used by the UART for the Receive and Transmit Baud Clocks (see UART, next section).

Section 8.4B:TR1602B UART

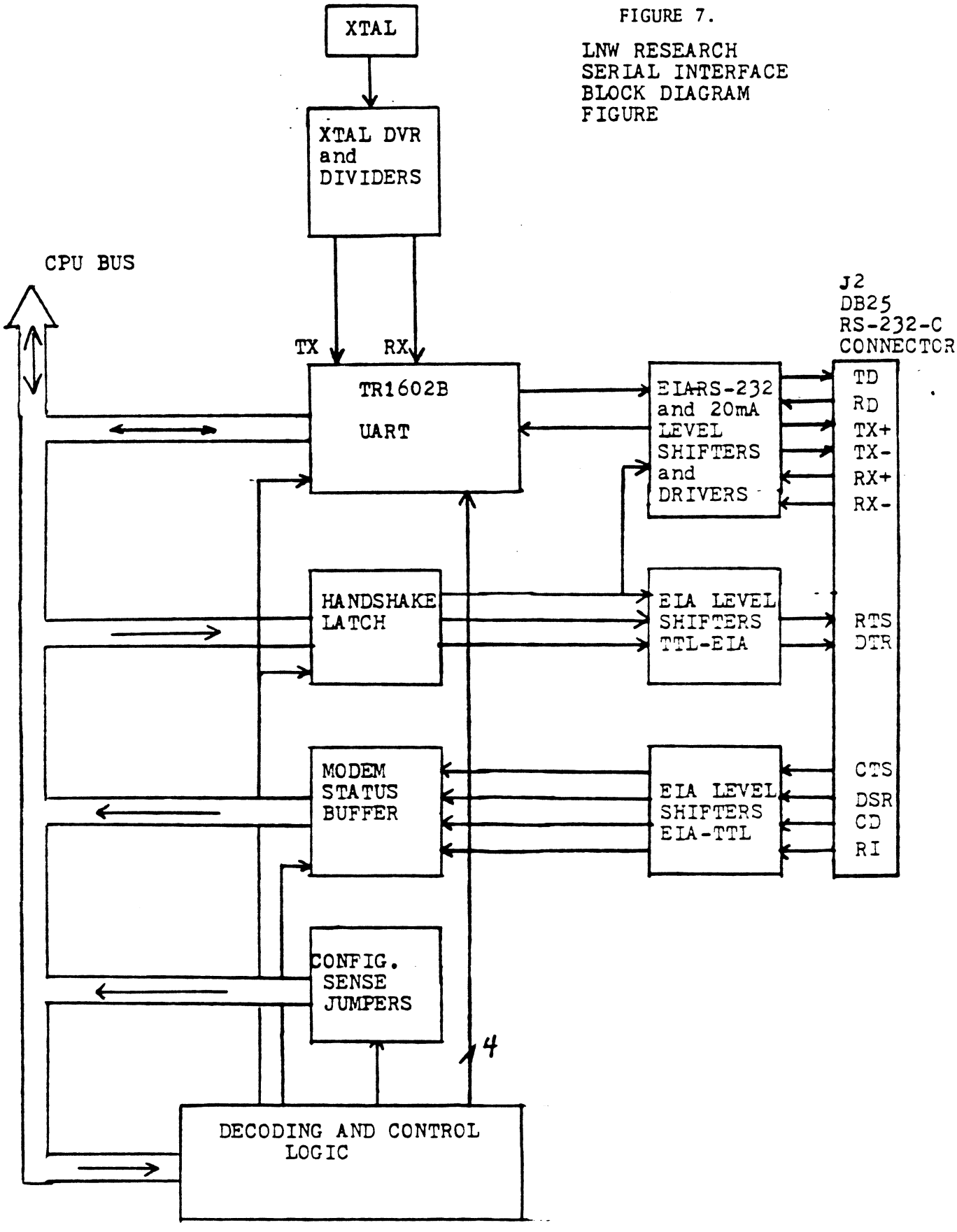
The TR1602B Universal Asynchronous Receiver/Transmitter (UART) is the heart of the serial interface. It takes parallel data from the CPU BUS and converts it to serial data and at the same time can receive serial data and convert it to parallel. It has two registers which can be read--one for the status and the other with received data. It has two registers which can be loaded--one with transmit data and the other with control information (word length,parity,stop bits). A reprint of the Western Digital TR1602B Data Sheet is included in the next section for those interested in the details of it's operation.

Section 8.4C:EIA RS232C and 20mA Level Shifters and Drivers

The serial output of U40 is pin25 (TRO). It drives U18 for buffering to EIA Driver U61pin9 and the 20 mA driver U50pin6. Serial output can be by U26pin10 which drives both U60pin10 and U50pin7. U50, R23 and 24 provide the 20mA interface. When U50 conducts it allows about 20mA of current to flow (20mA=mark,ØmA=space). Received serial data is brought in to U50pin4. U51 is an EIA to TTL receiver. The 20mA serial input is accomplished by the current to voltage conversion of R25 and 26. The TTL received data is fed to the Receive Data (RI,U40pin20) of the UART and is fed to U33pin12 to be read as part of the Modem Status Buffer.

FIGURE 7.

LNW RESEARCH
SERIAL INTERFACE
BLOCK DIAGRAM
FIGURE



Section 8.4D:Handshake Latch

U26 is the handshake latch. D0-D2 inputs to U26pin4,5, and 12 respectively. The latch is loaded when U26pin9 goes "low" from OUT EAH (U16pin5). The outputs of U26 are fed to U61pin12,13, and U61pin4,5 for level conversion to EIA standards.

Section 8.4E:Modem Status Buffer

U33 is the modem status buffer. EIA receiver at U52 converts EIA levels to TTL. This is input to U33 at pins 2,4,6, and 10. In addition, the Serial Input (TTL) is fed to U33pin12 to allow the CPU to directly input the serial data.

8.4F:Configuration Sense Jumpers

Jumper wires from K,N,P,M, and J connected to E5 or E6 select whether the associated data bit is a "one" or a "zero" when U28 is enabled on the data bus. U16pin6 goes "low" when port E9H is addressed which drives the enable pin5 (1 and 15) of U28. These jumpers are used by the serial driver software so stop bits, parity and word length can be selected by hardware configuration.

8.4G:Decoding and Control Logic

The port address decoding (IN,OUT-E8,E9,EA,EB) is accomplished by U41 and U16. U41 decodes the upper 6 bits (E8) and outputs to the strobe inputs (1G,2G) of U16. The lower two address bits (A0,A1) feed to the A and B inputs of U16. U16 is a 2/4 line decoder and its outputs (pins4,5,6,7,9,11,12) (active low) select which port is addressed and whether it is an in or out instructions. U23 (pins1 and 2) is driven by INEAH and INEBH such that, whenever, the Receive Register and the Status Register of the UART are read, U39 drives the data onto the data bus. Below is a summary of the address decoding:

IN E8H - Modem Status Register
IN E9H - Configuration Jumpers
IN EAH - UART Status Register
IN EBH - UART Receive Register, Data Received Reset

OUT E8H - Master Reset
OUT E9H - Not Used
OUT EAH - Control Register Load, Handshake Latch Load
OUT EBH - Transmit Holding Register Load

Data Bit	Jumper Letter	Configuration Jumpers	UART Control Register Handshake Latch	UART Status Register	Modem Status Register
D7	j	Even/Odd Parity 1=Even 0=Odd	Even/Odd Parity	Data Received 1=True	Clear to send Pin 5 DB-25
D6	m	Word Length 1	Word Length 1	THRE 1=True	DSR Pin 6 DB-25
D5	p	Word Length 2	Word Length 2	OverrunError 1=True	CD Pin 8 DB-25
D4	n	Stop Bit Slct. 1=2bits,0=1bit	Stop Bit Slct. 1=2bits,0=1bit	Framing Err. 1=True	Ring Indctor. Pin 22 DB-25
D3	k	Parity Inhibit 1 disabled par.	Parity Inhibit 1 disabled par.	Parity Error 1=True	
D2			Break,0 Disable Transmit Data		
D1			Request to Send Pin 4 DB-25		Receiver In. UART Pin 20
D0			Data Terminal Ready Pin 20 DB-25		
		IN ØE9H	OUT ØEAH	IN ØEAH	IN ØE8H

FIGURE 8.
SERIAL INTERFACE PORT ADDRESSING

Section 8.5: Real Time Clock

The Real Time Clock is asserted every twenty-five (25) milliseconds, the time period corresponds to a 40HZ interrupt. The programming can be by DOS or in a User's Machine Program. The interrupt service must read from address 37EØH. If Bit D7 is equal to a logical 1, this indicates the RTC generated the interrupt request. Note the TRSDOS Manual for commands.

Section 8.6: Dual Cassette Port

The System Expansion features a Dual Cassette Port Control. An externally wired relay will be required (shown on the schematic) to control two cassette recorders.

The cassette control utilizes data bit Ø (DØ) to control the selection of cassette output jacks. Memory address 37E4H will generate signal CSW allowing bit DØ to either set or reset the flip-flop U41. U41 is a set of nand gates wired as a flip-flop which will control U50, a high current driver to force the relay to switch states. The following assembly program illustrates the selection of cassette zero or cassette one:

```
; cassette zero selection

        LDA, ØØH            ; load Ø in DØ

        LD (37E4H), A       ; output to U41 flip-flop

; cassette one selction

        LDA, ØlH            ; load 1 in DØ

        LD (37E4H), A       ; output to U41 flip-flop
```

Under the Basic Program, the cassette related commands are: CSAVE and CLOAD. Examples are as follows:

```
CLOAD # - 1, "A"

CSAVE # - 2, "A"
```

The above basic commands will load from cassette tape #1 and transfer the resident program to cassette tape #2.

Section 8.7: Power Supply

The Radio Shack UL Approved Power Pack at T-1 provides 17.0VAC at 1A and 19.8VDC (internally rectified) at .35A. Both windings are center tapped. The AC secondary is full wave rectified by CR1 to provide unregulated DC for the +5 and -5 supplies.

Section 8.7A:+5 Supply

The unregulated positive output of CR-1 is filtered by C1 and fed through F-1 to limiting resistors R32 and R1,C66 and C67 at the input of regulators U62 and U66 eliminate oscillation along with the output bypass capacitors C-8 and C60. Regulators U62 and U66 provide accurate +5 supplies to JP3 and JP1 with short circuit current limiting and thermal shutdown.

Section 8.7B:-5 Supply

The minus lead of CR-1 is filtered by C-3 and regulated by R10 and CR-2 (5.1 V 5%) C-4 filters the regulated output.

Section 8.7C:+12 Supply

The 19.8 volts unfiltered DC from T-1 is filtered by C-2 and through F-2 provides the unregulated input to U63. U63 serves as a pre-regulator to U64. This arrangement with U63, R-6 and U64 provides Foldback Current Limiting under overload or short circuit conditions. Imagine that the output of U64 is shorted to ground. The GND reference for U63 is now at ground and being a +5 regulator it has exactly 5VDC at its output. With the voltage drop across R6, the input voltage to U64 is around 3V. This voltage approaches the minimum differential input-output voltage of the 7812 regulator. For this reason, the regulator cannot supply more than a few hundred milliamps of current to the short. With this scheme, the power pack is protected against long term overloads and circuits on the +5 supplies are protected in the event of a +5 to +12 short.

Section 8.7D:-12 Supply

Minus 12VDC is required for the UART and RS-232-C/20mA interface. In order to provide this, voltage doubling is required to obtain a negative voltage greater than -15V for regulation. R11 limits current, C5 provides DC blocking and CR3 and CR4 provide doubling with C6 filtering the final doubled unregulated supply (-20V).

C7 filters the regulated output of regulator U65 providing -12VDC.

Section 8.7E:Overvoltage Crowbar

In the event the +5 supplies at JP1 overvoltages over 6.2 volts, CR5 will begin to conduct current. While the gate voltage of Q-1 remains the same, the anode voltage will continue to rise. When the anode is more positive than the gate, the anode will conduct forward current to the cathode which feeds through CR8 to fire SCR1 and SCR2. This causes both F-1 and F-2 to open. CR10 is used to isolate the two five volt regulators but cause the crowbar to fire in the event of a +5 overvoltage at JP3 (6.9V). Q2 operates in the same fashion but since CR7 is a 14V zener, as Q1, the trigger voltage is around 14V.

Troubleshooting begins with cutting of the power supply jumpers at JP1,JP12,and JP3. Then jumper across the gate and anode of Q1 and jumper the gate and anode of Q2. Replace F1 and F2, power up the board and with a voltmeter, quickly identify the overvoltage source. When the supply is repaired, remove the jumpers across Q1 and Q2 and reinstate jumpers at JP1,JP12, and JP3.

WESTERN DIGITAL CORPORATION

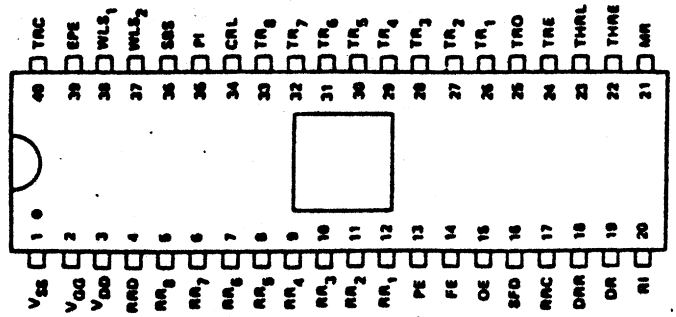
MOS/LSI
TR1602A & TR1602B
ASYNCHRONOUS RECEIVER/TRANSMITTER

WESTERN DIGITAL CORPORATION • 3242 RED HILL AVENUE • NEWPORT BEACH, CALIFORNIA 92663 • (714) 557-3550

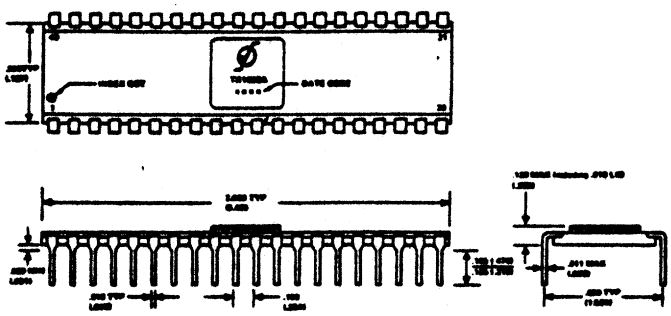
FEATURES

- SILICON GATE TECHNOLOGY – LOW THRESHOLD CIRCUITRY
  Directly TTL and DTL Compatible – External Resistors Eliminated
- D. C. STABLE (STATIC) CIRCUITRY
- FULL DUPLEX OR HALF DUPLEX OPERATION
  Transmits And Receives Serial Data Simultaneously Or Alternately
- AUTOMATIC INTERNAL SYNCHRONIZATION OF DATA AND CLOCK
- AUTOMATIC START BIT GENERATION
- BUFFERED RECEIVER AND TRANSIMITTER REGISTERS
- FULLY PROGRAMMABLE – EXTERNALLY SELECTABLE
  Word Length
  Baud Rate
  Even/Odd Parity (Receiver/Verification – Transmitter/Generation)
  Parity Inhibit – Verification/Generation
  One, One and One-Half, or Two Stop Bit Generation
- AUTOMATIC DATA RECEIVED/TRANSMITTED STATUS GENERATION
  Transmission Complete
  Buffer Register Transfer Complete
  Received Data Available
  Parity Error
  Framing Error
  Overrun Error
- THREE-STATE OUTPUTS
  Receiver Register Outputs
  Status Flags
- AVAILABLE IN CERAMIC OR HERMETIC PLASTIC CAVITY PACKAGES

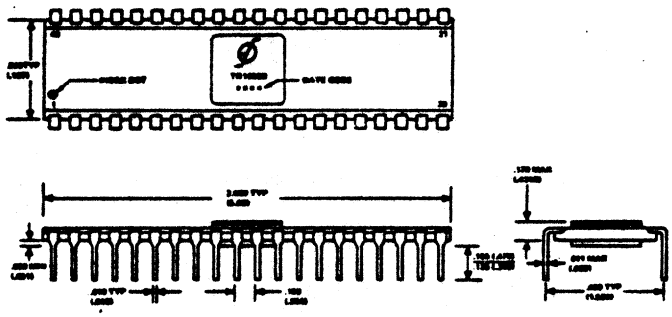
PIN CONNECTIONS



TR1602A CERAMIC PACKAGE OUTLINE



TR1602B HERMETIC PLASTIC CAVITY PACKAGE OUTLINE



APPLICATIONS

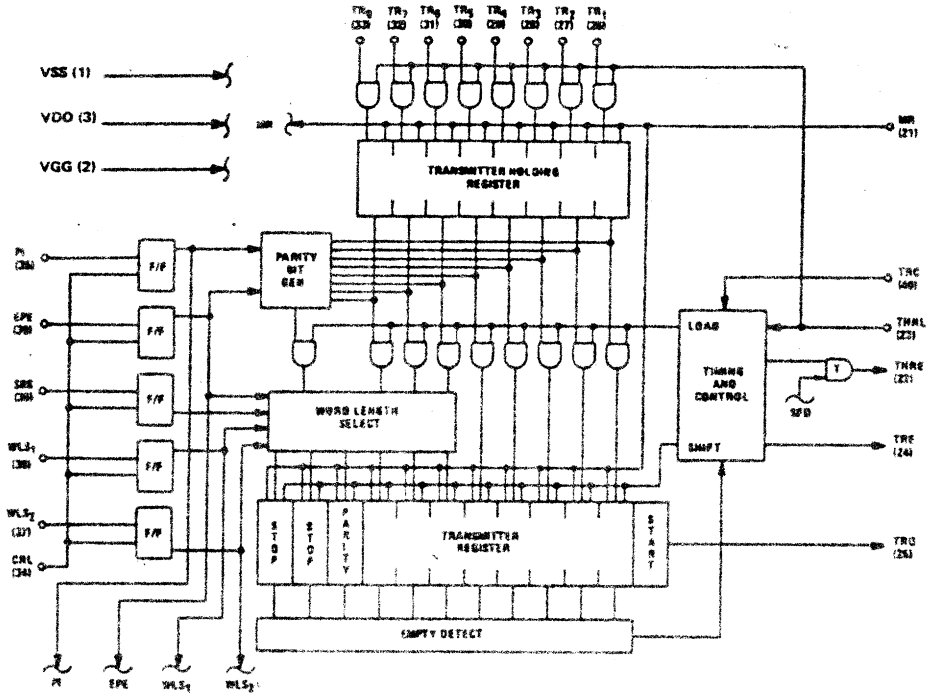
- PERIPHERALS
- TERMINALS
- MINI COMPUTERS
- FACSIMILE TRANSMISSION
- MODEMS
- CONCENTRATORS
- ASYNCHRONOUS DATA MULTIPLEXERS
- CARD AND TAPE READERS
- PRINTERS
- DATA SETS
- CONTROLLERS
- KEYBOARD ENCODERS
- REMOTE DATA ACQUISITION SYSTEMS
- ASYNCHRONOUS DATA CASSETTES

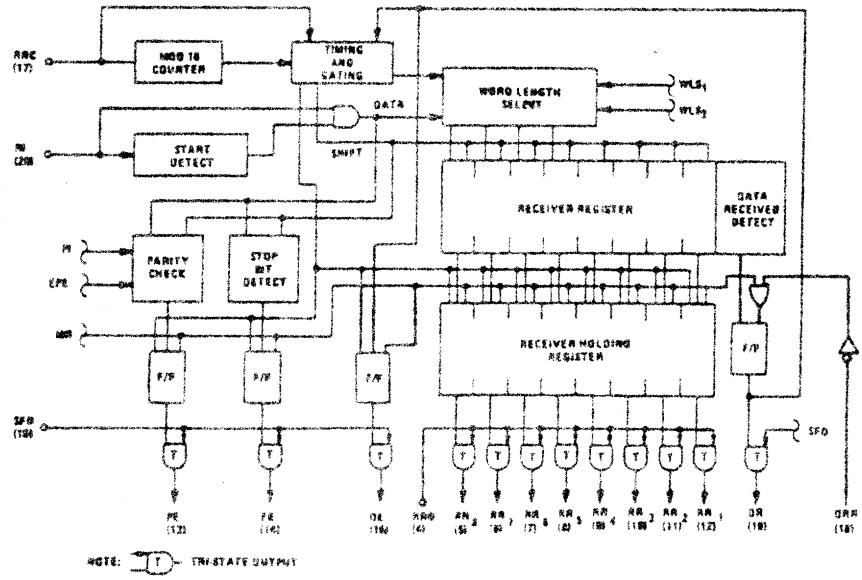
GENERAL DESCRIPTION

The TR1602A & the TR1602B are ASYNCHRONOUS RECEIVER/TRANSMITTER sub-systems using silicon gate process technology. The use of this low threshold process provides direct compatibility with all forms of current sinking logic. Interfacing restraints, such as external resistors, drivers and level shifting circuitry, are eliminated. All output lines have been designed to drive TTL directly.

The ASYNCHRONOUS RECEIVER/TRANSMITTER is a general purpose, programmable MOS/LSI device for interfacing an asynchronous serial data channel of a peripheral or terminal with parallel data of a computer or terminal. The transmitter section converts parallel data into a serial word which contains the data along with start, parity, and stop bits. The receiver section converts a serial word with start, data, parity, and stop bits, into parallel data, and it verifies proper code transmission by checking parity and receipt of a valid stop bit. Both the receiver and the transmitter are double buffered. The array is compatible with bipolar logic. The array may be programmed as follows: The word length can be either 5, 6, 7, or 8 bits; parity generation and checking may be inhibited, the parity may be even or odd; and the number of stop bits may be either one or two, with one and one half when transmitting a 5 bit code. Note: See TR1402A Data Sheet for operation with 5 level code-2 stop bits.

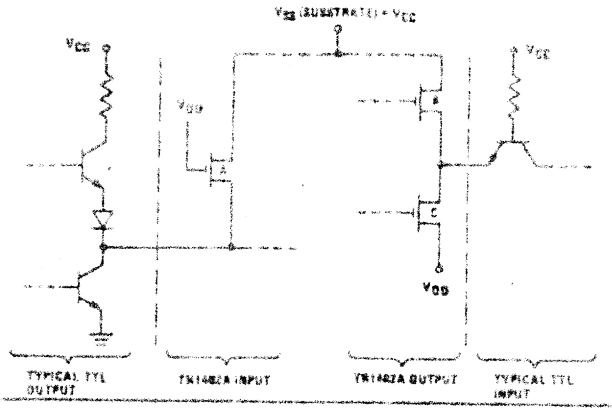
ADVANCE ENGINEERING INFORMATION





INPUT STRUCTURE

MOS DEVICE "A" ACTS AS AN INTERNAL PULL-UP RESISTOR TO $V_{SS} = V_{CC}$ WHICH BIASES OFF THE CASCODE DEVICE OF THE TTL OUTPUT IN THE HIGH-LEVEL OUTPUT STATE. IN THE LOW-LEVEL OUTPUT STATE THE TTL OUTPUT DEVICE SINKS THE CURRENT SUPPLIED BY DEVICE "A".



OUTPUT STRUCTURE

DEVICES "B" & "C" COMPRISE A PUSH-PULL OUTPUT BUFFER. IN THE LOW-LEVEL STATE, OUTPUT TRANSISTOR "C" IS "ON" AND CASCODE DEVICE "B" IS OFF. IN THE HIGH-LEVEL STATE, THE OPPOSITE IS TRUE. IN THE DISCONNECTED STATE, BOTH "B" AND "C" ARE TURNED OFF CAUSING THE OUTPUT NODE TO FLOAT.

PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	V_{SS} Power Supply	V_{SS}	+5 volts supply
2	V_{GG} Power Supply	V_{GG}	-12 volts supply
3	V_{DD} Power Supply	V_{DD}	Ground
4	Receiver Register Disconnect	RRD	A high level input voltage, V_{IH}, applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR_8-RR_1 data outputs (pins 5-12).
5—12	Receiver Holding Register Data	RR_8–RR_1	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low-level input voltage, V_{IL}, is applied to RRD. For character formats of fewer than eight bits received characters are right-justified with RR_1 (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V_{OL}.
13	Parity Error	PE	A high level output voltage, V_{OH}, on this line indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE control line (pin 39). This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by Status Flag Disconnect line (pin 16).
14	Framing Error	FE	A high-level output voltage, V_{OH}, on this line indicates that the received character has no valid stop bit, ie., the bit following the parity bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Register, FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
15	Overrun Error	OE	A high-level output voltage, V_{OH}, on this line indicates that the Data REceived Flag (pin 19) was not reset before the next character was transferred to the REceiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
16	Status Flags Disconnect	SFD	A high-level input voltage, V_{IH}, applied to this pin disconnects the PE, FE, OE, DR and THRE allowing them to be buss connected.
17	Receiver Register Clock	RRC	The receiver clock frequency is sixteen (16) times the desired receiver shift rate.
18	Data Received Reset	DRR	A low-level input voltage, V_{IL}, applied to this line resets the DR line.
19	Data Received	DR	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.
20	Receiver Input	RI	Serial input data received on this line enters the RECEIVER REGISTER at a point determined by the character length, parity, and the number of stop bits. A high-level input voltage, V_{IH}, must be present when data is not being received.
21	Master Reset	MR	This line is strobed to a high-level input voltage, V_{IH}, to clear the logic. It resets the Transmitter and Receiver Registers, the Receiver Holding Register, FE, OE, PE, DRR and sets TRO, THRE, and TRE to a high-level output voltage, V_{OH}.
22	Transmitter Holding Register Empty	THRE	A high-level output Voltage, V_{OH}, on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.

PIN DEFINITIONS (CONT)

PIN NUMBER	NAME	SYMBOL	FUNCTION
23	Transmitter Holding Register Load	THRL	A low-level input voltage, V_{IL}, applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.
24	Transmitter Register Empty	TRE	A high-level output voltage, V_{OH}, on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.
25	Transmitter Register Output	TRO	The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a high-level output voltage, V_{OH}. Start of transmission is defined as the transition of the START bit from a high-level output voltage, V_{OH}, to a low-level output voltage, V_{OL}.
26–33	Transmitter Register Data Inputs	TR_1 – TR_8	The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), the character is right justified to the least significant bit, RR1, and the excess bits are disregarded. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted.
34	Control Register Load	CRL	A high-level input voltage, V_{IH}, on this line loads the CONTROL REGISTER with the control bits (WLS_1, WLS_2, EPE, PI, SBS). This line may be strobed or hard wired to a high-level input voltage, V_{IH}.
35	Parity Inhibit	PI	A high-level input voltage, V_{IH}, on this line inhibits the parity generation and verification circuits and will clamp the PE output (pin 13) to V_{OL}. If parity is inhibited the STOP bit(s) will immediately follow the last data bit on transmission.
36	Stop Bit(s) Select	SBS	This line selects the number of STOP bits to be transmitted after the PARITY bit. A high-level input voltage, V_{IH}, on this line selects two STOP bits, and a low-level input voltage, V_{IL}, selects a single STOP bit. Selection of two STOP bits when programming a five (5) bit word generates 1.5 STOP bits.
37–38	Word Length Select	WLS_2 – WLS_1	These two lines select the character length (exclusive of parity) as follows:

WLS_2	WLS_1	Word Length
V_{IL}	V_{IL}	5 bits
V_{IL}	V_{IH}	6 bits
V_{IH}	V_{IL}	7 bits
V_{IH}	V_{IH}	8 bits

39	Even Parity Enable	EPE	This line determines whether even or odd PARITY is to be generated by the transmitter and checked by the receiver. A high-level input voltage, V_{IH}, selects even PARITY and a low-level input voltage, V_{IL}, selects odd PARITY.
40	Transmitter Register Clock	TRC	The transmitter clock frequency is sixteen (16) times the desired transmitter shift rate.

FEB. 1978

INTRODUCTION

The transfer of digital data over relatively long distances is generally accomplished by sending the data in serial form thru a single communications channel using one of two general transmission techniques; *asynchronous* or *synchronous*. Synchronous data transmission requires that a clock signal be transmitted with the data in order to mark the location of the data bits for receiver. A specified clock transition (either rising or falling) marks the start of each data bit interval as shown in Figure 1. In addition, special synchronization data patterns are added to the start of the transmission in order for the receiver to locate the first bit of the message. With synchronous transmission, each data bit must follow contiguously after the sync word, since one data bit is assumed for every clock period.

With asynchronous transmission, a clock signal is not transmitted with the data and the characters need not be contiguous. In order for the receiver to properly recover the message, the bits are grouped into data characters (generally from 5 to 8 bits in length) and synchronizing start and stop elements are added to each character as shown in Figure 2.

The start element is a single logic zero (space) data bit that is added to the front of each character. The stop element is a logic one (mark) that is added to the end of each character. The stop element is maintained until the next data character is ready to be transmitted. (Asynchronous transmission is often referred to as start-stop transmission for obvious reasons). Although there is no upper limit to the length of the stop element, there is a lower limit that depends on the system characteristics. Typical lower limits are 1.0, 1.42 or 2.0 data bit intervals, although most modern systems use 1.0 or 2.0. The negative going transition of the start element defines the location of the data bits in one character. A clock source at the receiver is reset by this transition and is used to locate the center of each data bit.

The rate at which asynchronous data is transmitted is usually measured in *baud*, where a baud is defined to be the reciprocal of the shortest signal element (usually one data bit interval). It is interesting to note

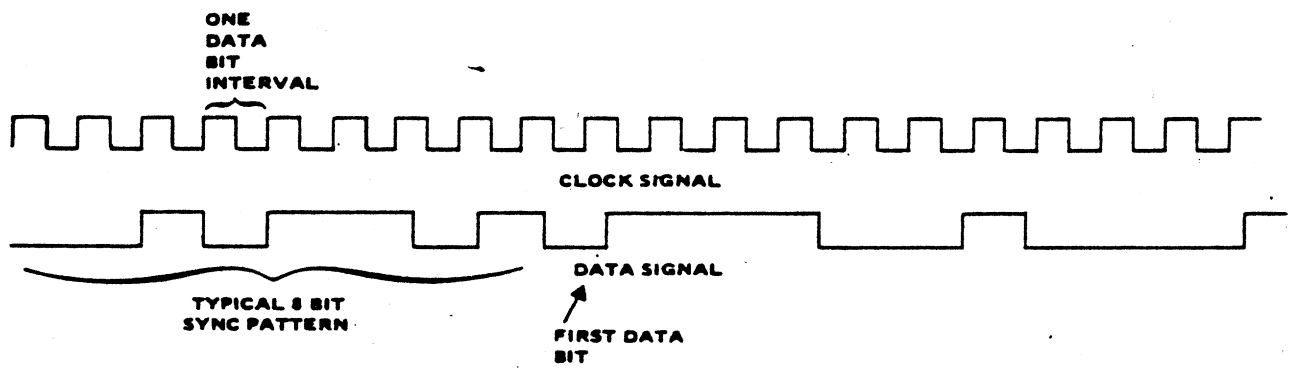


Figure 1. Synchronous Data

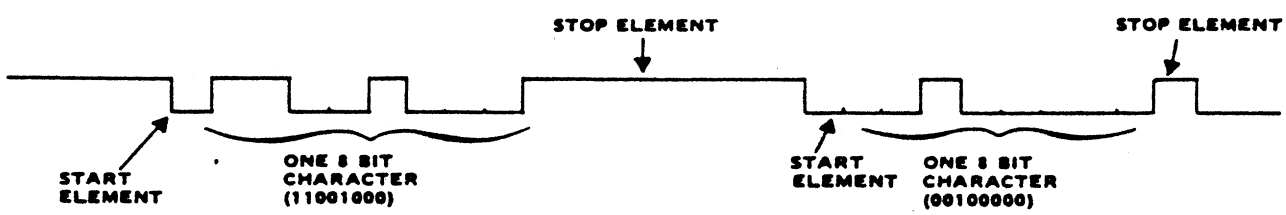


Figure 2. Asynchronous Data

PRINTED IN U.S.A. 2/78

WESTERN DIGITAL
CORPORATION
3128 RED HILL AVENUE, BOX 2180
NEWPORT BEACH, CALIFORNIA 92663
(714) 557-3550 TWX 910-595-1139

that the variable stop length is what makes the baud rate differ from the bit rate. For synchronous transmission, each element is one bit in length so that the baud rate equals the bit rate. The same is true for asychronous transmission if the stop element is always one bit in duration (this is referred to as *isochronous* transmission). However, when the stop code is longer than one bit, as shown in Figure 3, the baud rate differs from the bit rate.

Each character in Figure 3 is 11 data bit intervals in length, and if 15 characters are transmitted per second, then the shortest signal element (one data bit interval) is 66.6 ms/11 = 6.06 ms; giving a rate of 1/6.06 ms = 165 baud. However, since only 10 bits of information (8 data bits, one start bit and 1 stop bit) are transmitted every 66.6 msec, the bit rate is 150 bit/sec. (Even though the stop element lasts for two data intervals, it still is only one bit of information)

There are several reasons for using asychronous transmission. The major reason is that since a clock signal need not be transmitted with the data, transmission equipment requirements are greatly simplified. (Note, however, that an independent clock source is still required at both the transmitter and receiver). Another advantage of asynchronous transmission is that characters need not be contiguous in time, but are transmitted as they become available. This is a very valuable feature when transmitting data from manual entry devices such as a keyboard. The major disadvantage of asynchronous transmission is that it requires a very large portion of the communication channel bandwidth for the synchronizing start and stop elements (a much smaller portion of the bandwidth is required for the sync words used in synchronous transmission).

Asynchronous transmission over a simple twisted wire pair can be accomplished at moderately high baud rates (10K baud or higher depending on the length of the wire, type of line drivers, etc.) while it is generally limited to approximately 2K baud over the telephone network. When operating over the telephone network, a modem is required to convert the data pulses to tones that can be transmitted through the network.

One of the major limiting factors in the speed of asynchronous transmission is the distortion of the signal elements. Distortion is defined as the time displacement between the actual signal level transition and the nominal transition (Δt), divided by the nominal data bit interval (See Figure 4).

The nominal data bit interval is equal to the reciprocal of the nominal transmission baud rate and all data transitions should ideally occur at an integer number of intervals from the start bit negative going transition. Actual data transitions may not occur at these nominal points in time as shown in the lower waveform of Figure 4. The distortion of any bit transition is equal to $\Delta t \times$ NOMINAL BAUD RATE.

This distortion is generally caused by frequency jitter and frequency offset in the clock source used to generate the actual waveform as well as transmission channel, noise, etc. Thus, the amount of distortion that can be expected on any asynchronous signal depends on the device used to generate the signal and the characteristics of the communication channel over which it was sent. Electronic signal generators can be held to less than 1% distortion while electromechanical devices (such as a teletype) typically generate up to 20% distortion. The transmission channel may typically add an additional 5% to 15% distortion.

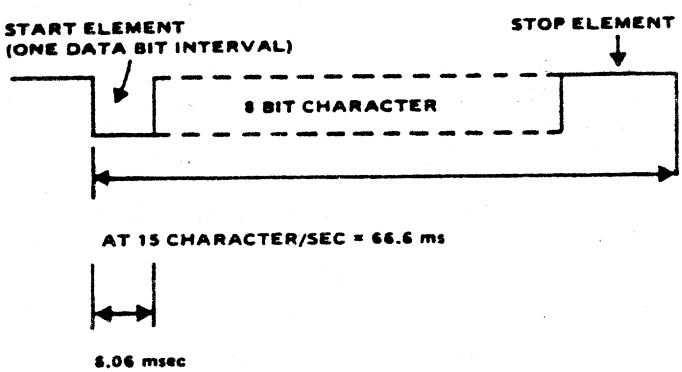


Figure 3.

3128 RED HILL AVENUE, BOX 2180
NEWPORT BEACH, CALIFORNIA 92663
(714) 557-3550 TWX 910-595-1139

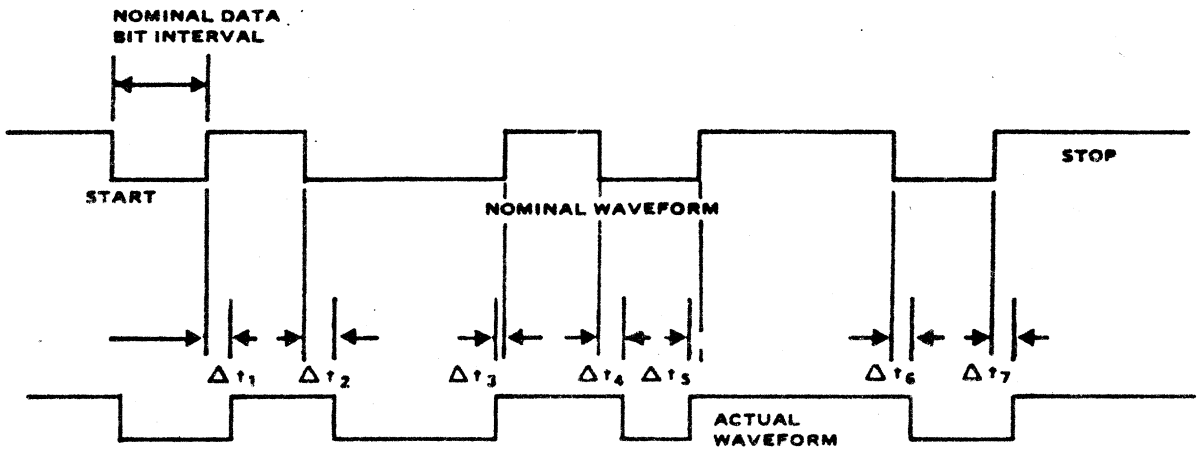


Figure 4A

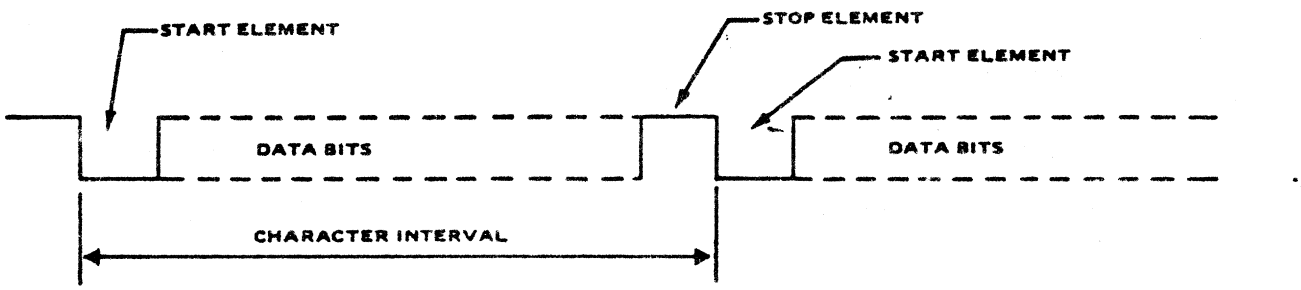


Figure 4B

The distortion previously described referred only to a single character as all measurements were referenced to the start element transition of that character. However, there may also be distortion between characters when operating at the maximum possible baud rate (i.e., stop elements are of minimum length). This type of distortion is usually measured by the minimum character interval as shown in Figure 4B.

The minimum character interval distortion is generally specified as the percentage of a nominal data bit interval that any character interval may be shortened from its nominal length. Since many of the same parameters that cause distortion of the data bits are also responsible for the character length distortion, the two distortions are often equal. However, some systems may exhibit character interval distortions of up to 50% of a data bit interval. This parameter is important when operating at the maximum baud rate since the receiver must be prepared to detect the next start bit transition after the minimum character interval.

Asynchronous receivers operate by locating the nominal center of the data bits as measured from the start bit negative going transition. However, due to receiver inaccuracies, the exact center may not be properly located. In electromechanical devices such as teletypes, the inaccuracy may be due to mechanical tolerances or variations in the power line frequency. With electronic receivers, the inaccuracies are due to frequency offset, jitter and resolution of the clock source used to find the bit centers. (The bit centers are located by counting clock pulses). For example, even if the receiver clock had no jitter or offset, and it was 16 times the baud rate, then the center of the bit could only be located within 1/16 of a bit interval (or 6.25%) due to clock resolution. However, by properly phasing the clock, this tolerance can be adjusted so that the sample will always be within ±3.125% of the bit center. Thus,

signals with up to 46.875% distortion could be received. This number (the allowable receiver input distortion) is often referred to as the receiver distortion margin. Electromechanical receivers have distortion margins of 25 to 30%. The receiver must also be prepared to accept a new character after the minimum character interval. Most receivers are specified to operate with a minimum character interval distortion of 50%.

TR1602 Operation**

The WDC TR1602 is designed to transmit and receive asynchronous data as shown in Figure 5. Both the transmitter and the receiver are in one MOS CHIP, packaged in a 40 lead ceramic DIP. The array is capable of full duplex (simultaneous transmission and reception) or half duplex operation.

The transmitter basically assembles parallel data characters into a serial asynchronous data system. Control lines are included so that the characters may be 5, 6, 7 or 8 bits in length, have an even or odd parity bit, and have either one or two* stop bits. Furthermore, the baud rate can be set anywhere between DC and 20K baud by providing a transmit clock at 16 times the desired baud rate.

*1-1/2 with 5 bit code

**All references to the TR1602 operation also apply to the TR1863 operation.

The receiver disassembles the asynchronous characters into a parallel data character by searching for the start bit of every character, finding the center of every data bit, and outputing the characters in a parallel format with the start, parity and stop bits removed. Three error flags are also provided to indicate if the parity was in error, a valid stop bit was not decoded or the last character was not unloaded by the external device before the next character was received (and therefore the last character was lost). The receiver clock is set at 16 times the transmitter baud rate.

Both the transmitter and receiver have double character buffering so that at least one complete character interval is always available for exchange of the characters with the external devices. This double buffering is especially important if the external device is a computer, since this provides a much longer permissible interrupt latency time (the time required for the computer to respond to the interrupt).

The status of the transmitter buffer and the receiver buffer (empty or full) is also provided as an output.

Another feature of the TR1602 is that the control information can be strobed into the transmitter and receiver and stored internally. This allows a common bus from a computer to easily maintain the controls for a large number of transmitter/receivers.

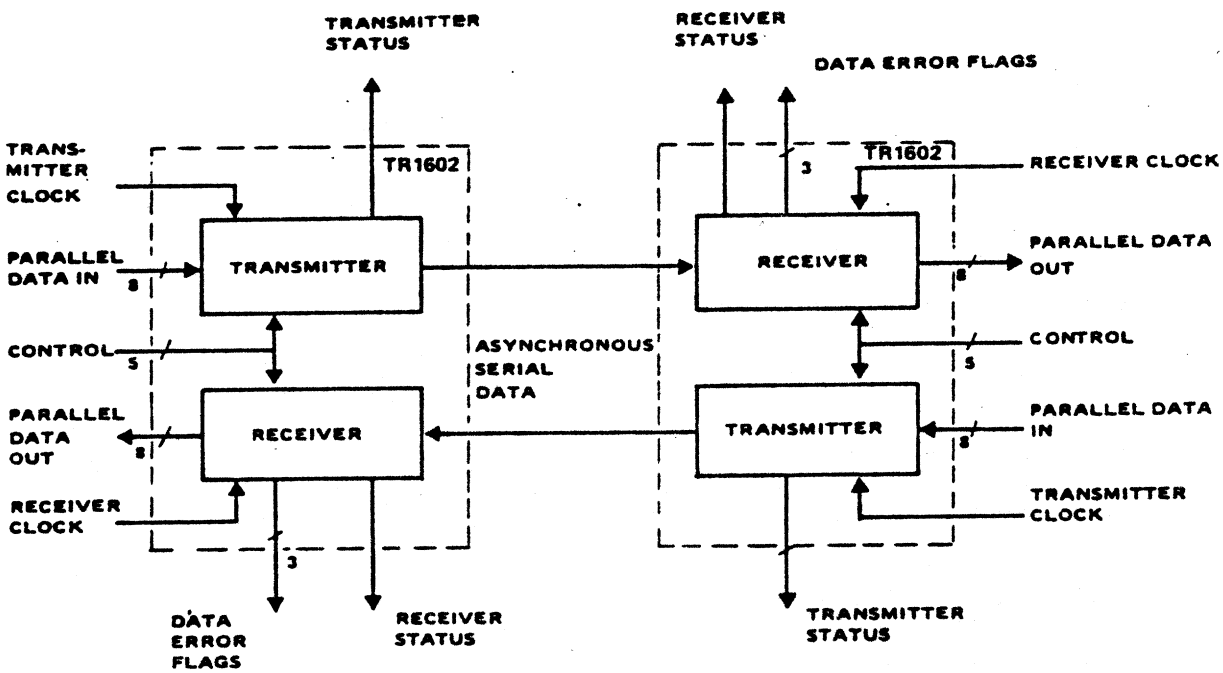


Figure 5

3128 RED HILL AVENUE, BOX 2180
NEWPORT BEACH, CALIFORNIA 92663
(714) 557-3550 TWX 910-595-1139

The TR1602 data and error flag outputs are designed for direct compatibility with bus organized systems. This feature is achieved by providing completely TTL compatible Three-state outputs (no external components are required). Three-state outputs may be set to a logic one or logic zero when enabled, or set to an open circuit (very high impedance) when disabled. A separate control line is provided to enable the data outputs and another one to enable the error flags so that the data outputs can be tied to a separate bus from the flag outputs.

The TR1602 inputs are also directly compatible with TTL logic elements without any external components.

TR1602 Description

Figure 6 is a block diagram of the transmitter portion of the TR1602. Data can be loaded into the Transmitter Holding Register whenever the Transmitter Holding Register Empty (THRE) line is at a logic one, indicating that the Transmitter Holding Register is empty. The data is loaded in by strobing the Transmitter Holding Register Load (THRL) line to a logic zero. The data is automatically transferred to the Transmitter Register as soon as the Transmitter Register becomes empty. The desired start, stop and parity bits are then added to the data and serial transmission is started. The number of stop bits and the type of parity bit is under control of the Control Register. The state of the control lines is loaded into the Control Register when the Control Register Load (CRL) line is strobed to a logic one. The 5 control lines allow 24 different character formats as shown in Table 1. These 24 formats cover almost all of the transmission schemes presently in use.

A Master Reset (MR) input is provided which sets the transmitter to the idle state whenever this line is strobed to a logic one. In addition, a Status Flag Disconnect (SFD) line is provided. When this signal is at a logic one, the THRE output is disabled and goes to a high impedance. This allows the THRE outputs of a number of arrays to be tied to the same data bus.

Figure 7 illustrates the relative timing of the transmitter signals. After power turn-on, the master reset should be strobed to set the circuits to the idle state. The external device can then set the transmitter register data inputs to the desired value and after the data inputs are stable, the load pulse is applied. The data is then automatically transferred to the Transmitter Register where the start, stop and parity (if required) bits are added and transmission is started. This process is then repeated for each subsequent character as they become available. The only timing requirement for the external device is that the data

TABLE 1
CONTROL DEFINITION

CONTROL WORD					CHARACTER FORMAT			
WLS2	WLS1	PI	EPE	SBS	START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	0	1	5	ODD	1
0	0	0	0	1	1	5	ODD	1.5
0	0	0	1	0	1	5	EVEN	1
0	0	0	1	1	1	5	EVEN	1.5
0	0	1	x	0	1	5	NONE	1
0	0	1	x	1	1	5	NONE	1.5
0	1	0	0	0	1	6	ODD	1
0	1	0	0	1	1	6	ODD	2
0	1	0	1	0	1	6	EVEN	1
0	1	0	1	1	1	6	EVEN	2
0	1	1	x	0	1	6	NONE	1
0	1	1	x	1	1	6	NONE	2
1	0	0	0	0	1	7	ODD	1
1	0	0	0	1	1	7	ODD	2
1	0	0	1	0	1	7	EVEN	1
1	0	0	1	1	1	7	EVEN	2
1	0	1	x	0	1	7	NONE	1
1	0	1	x	1	1	7	NONE	2
1	1	0	0	0	1	8	ODD	1
1	1	0	0	1	1	8	ODD	2
1	1	0	1	0	1	8	EVEN	1
1	1	0	1	1	1	8	EVEN	2
1	1	1	x	0	1	8	NONE	1
1	1	1	x	1	1	8	NONE	2

inputs be stable during the load pulse (and 20 nsec after).

The TR1602 Transmitter output will have less than 1% Distortion at baud rates of up to 20K baud (assuming the Transmitter Register Clock is perfect) and is, therefore, compatible with virtually all other asynchronous receivers.

Figure 8 is a block diagram of the Receiver portion of the TR1602. Serial asynchronous data is provided to the Receiver Input (RI). A start bit detect circuit continually searches for a logic one to logic zero transition while in the idle state. When this transition is located, a counter is reset and allowed to count until the center of the start bit is located. If the input is still a logic zero at the center, the signal is assumed to be a valid start bit and the counter continues to count to find the center of all subsequent

3128 RED HILL AVENUE, BOX 2180
NEWPORT BEACH, CALIFORNIA 92663
(714) 557-3550 TWX 910-595-1139

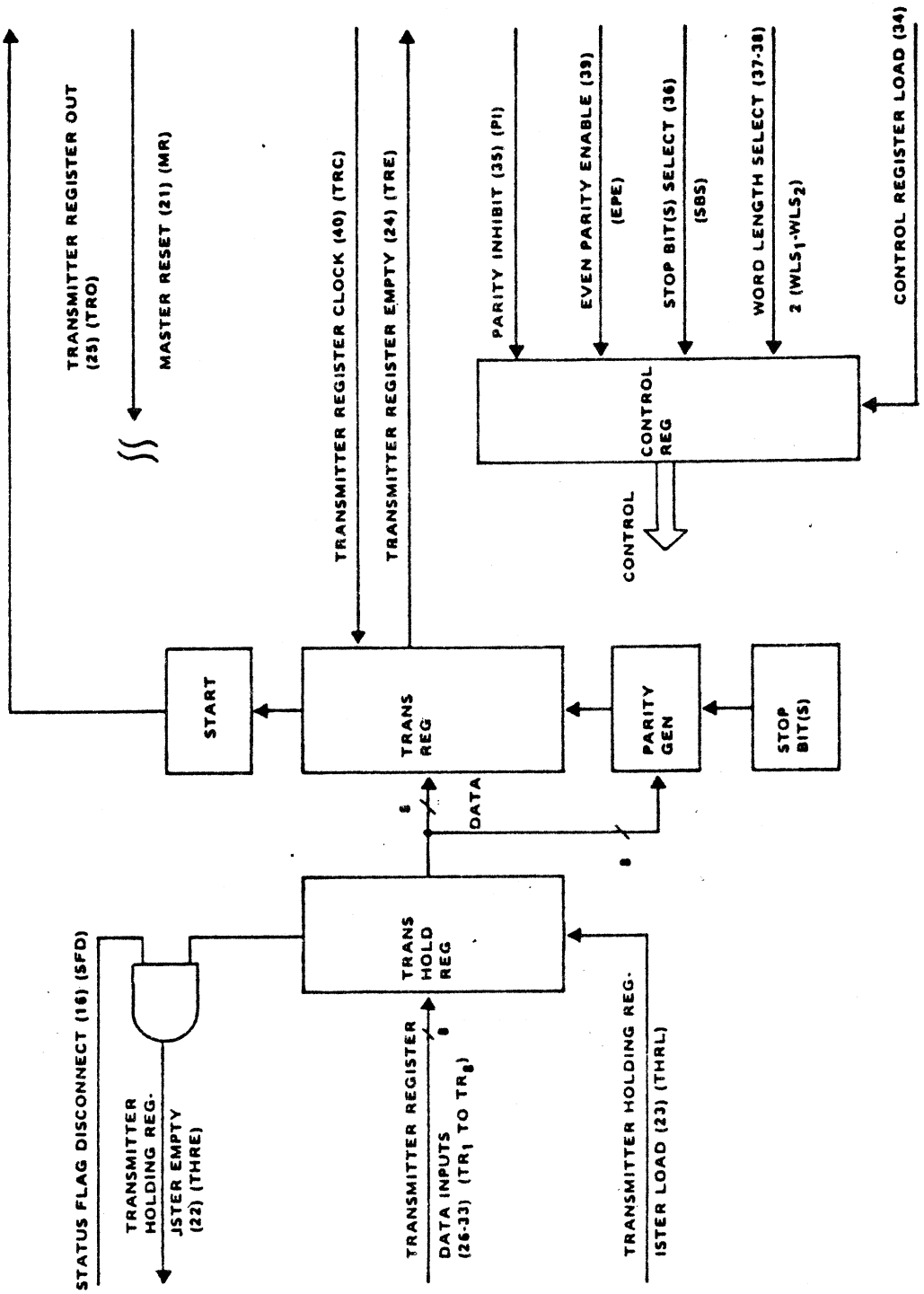


Figure 6. Transmitter Block Diagram

3128 RED HILL AVENUE, BOX 2180
NEWPORT BEACH, CALIFORNIA 92663
(714) 557-3550 TWX 910-595-1139

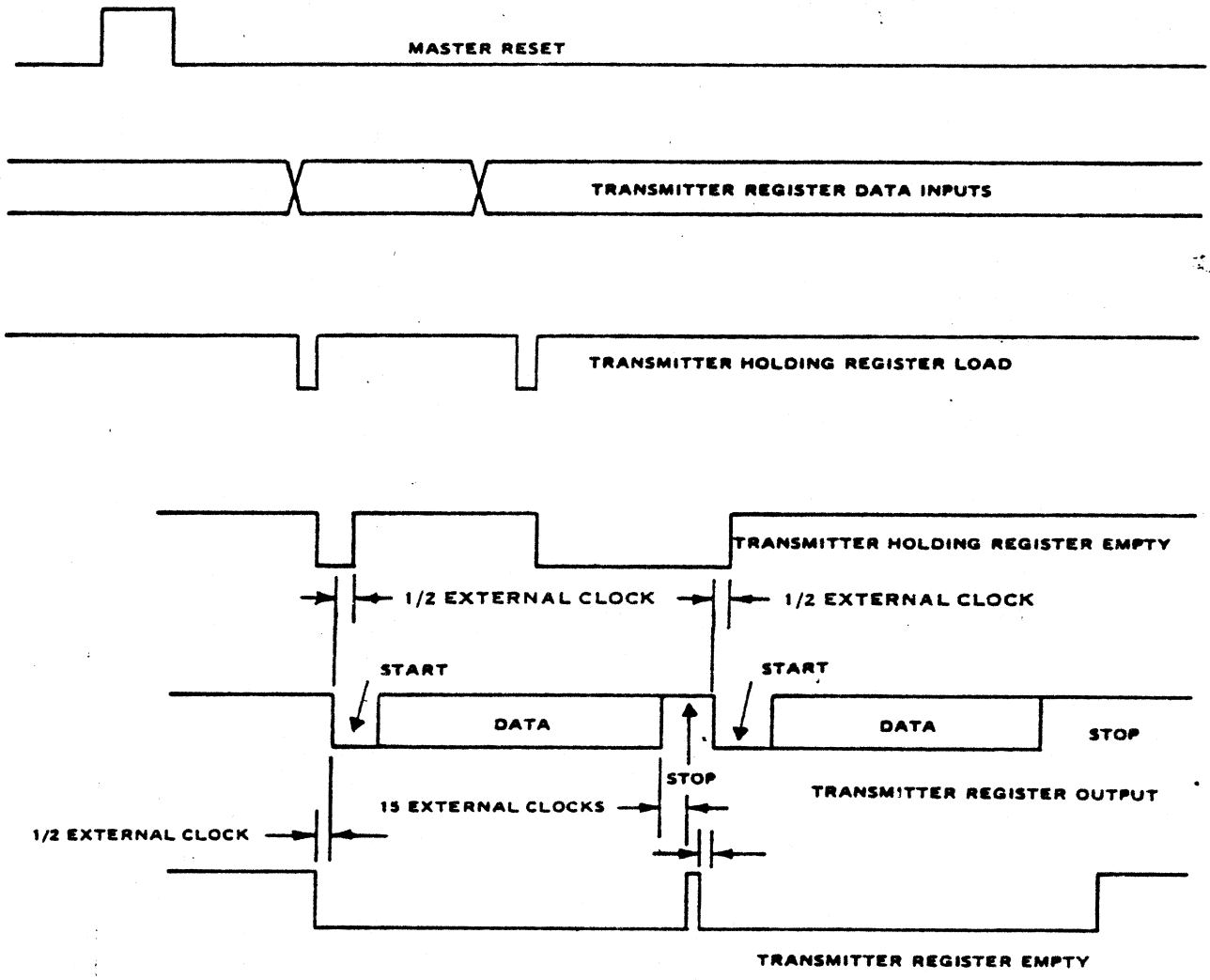


Figure 7. Transmitter Timing Diagram

data and stop bits. (Verification of the start bit prevents the receiver from assembling an erroneous data character when a logic zero noise spike is presented to the Receiver Input). The Receiver is under control of the Control Register described in the previous paragraph. This register controls the number of data bits, number of stop bits, and the type of parity as described in Table 1. The word length gating circuit adjusts the length of the Receiver Register to match the length of the data characters. A parity check circuit checks for even or odd parity if parity was added by the Transmitter. If parity does not check a Parity Error signal will be set to a logic one and this signal will be held until the next character is transferred to the Holding Register. A circuit is also provided that checks the first stop bit of each character. If the stop bit is not a logic one, the Framing Error line will be set to a logic one and held until the next character is transferred to the Holding Register. This feature permits easy detection of a break character (null character with no stop element). As each received character is transferred to the Holding Register, the Data Received (DR) line is set to a logic one indicating that the external device may sample the data output. When the external device samples the output, it should strobe the Data Received Reset (DRR) line to a logic zero to reset the DR line. If the DR line is not reset before a new character is transferred to the Holding Register (i.e., a character is lost) the Overrun Error line will be set to a logic one and held until the next character is loaded into the Holding Register. The timing for all of the Receiver functions is obtained from the external Receiver Register Clock which should be set at 16 times the baud rate of the transmitter.

3128 RED HILL AVENUE, BOX 2180
NEWPORT BEACH, CALIFORNIA 92663
(714) 557-3550 TWX 910-595-1139

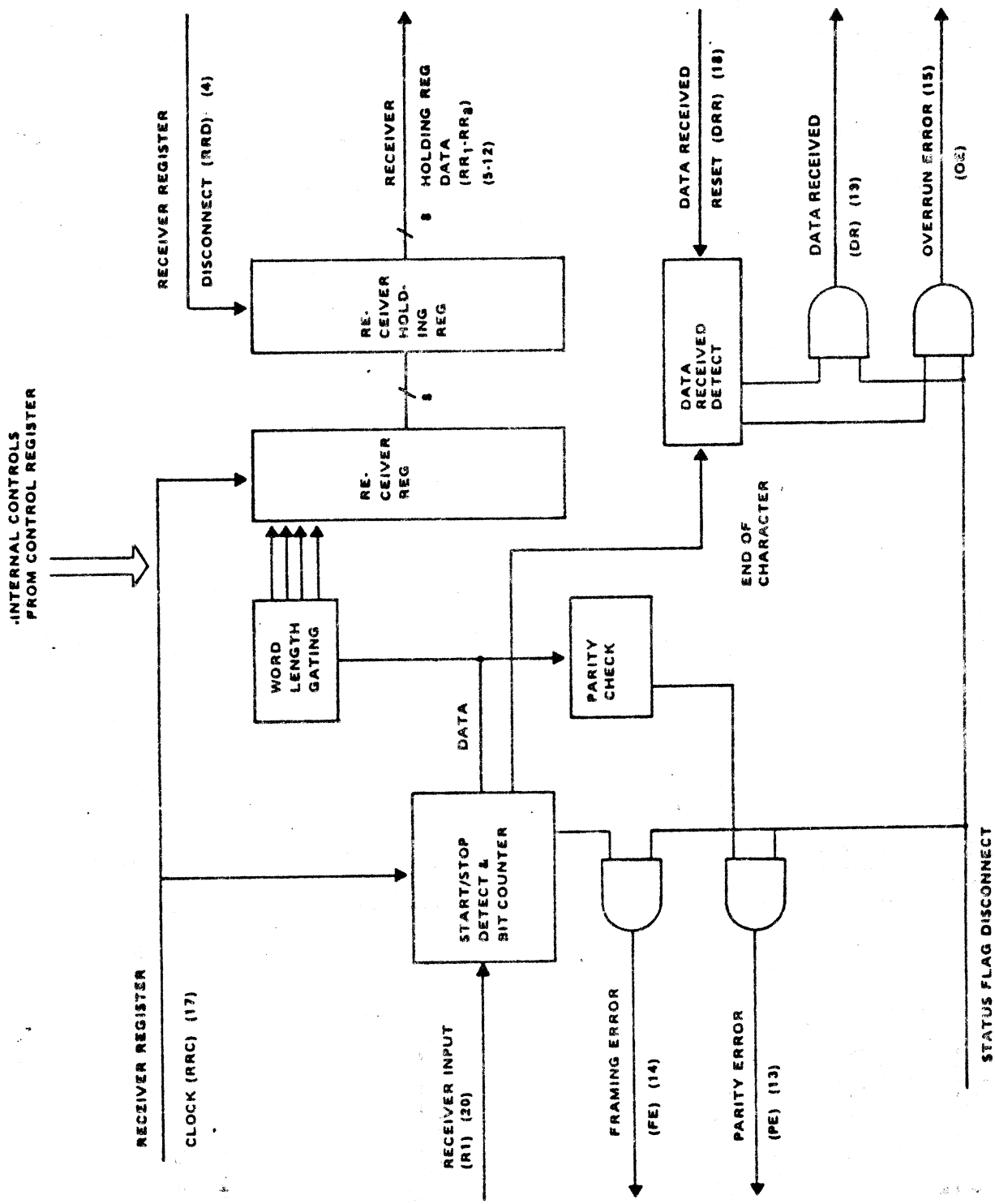


Figure 8. Receiver Block Diagram

3128 RED HILL AVENUE, BOX 2180
NEWPORT BEACH, CALIFORNIA 92663
(714) 557-3550 TWX 910-595-1139

Figure 9 illustrates the relative timing of the Receiver signals. A Master Reset strobe places the unit in the idle mode and the Receiver then begins searching for the first start bit. After a complete character has been decoded, the data output and error flags are set to the proper level and the Data Received (DR) line is set to a logic one. Although it is not apparent in Figure 9, the data outputs are set to the proper level one half clock period before the DR and error flags, which are set in the center of the first stop bit. The Data Received Reset pulse resets the DR line to a logic zero. Data can be strobed out at any time before the next character has been disassembled.

The TR1602 Receiver uses a 16X clock for timing purposes. Furthermore, the center of the start bit is defined as clock count 7-1/2. Therefore, if the receiver clock is a symmetrical square wave as shown in Figure 10, the center of the bits will always be located within ±3.125% (assuming a perfect input clock) thus giving a receiver margin of 46.875%.

In Figure 10, the start bit could have started as much as one complete clock period before it was detected, as indicated by the shaded area of the negative going transition. Therefore, the exact center is also unknown by the shaded area around the sample point. This turns out to be ±1/32 = ±3.125%.

If the receiver clock is not perfect, then the receiver distortion margin must be further reduced. For example, if the clock had 1.0% jitter, 0.1% offset and the positive clock pulse was only 40% of the clock cycle; then, for a 10 element character, the clock would add:

1.0% (Jitter) + (0.1% × 10) (Offset) + 0.1 (1/16) (Non-symmetrical Clock) = 2.3% Distortion

(The frequency offset was multiplied by the number of elements per character since the offset is cumulative on each element).

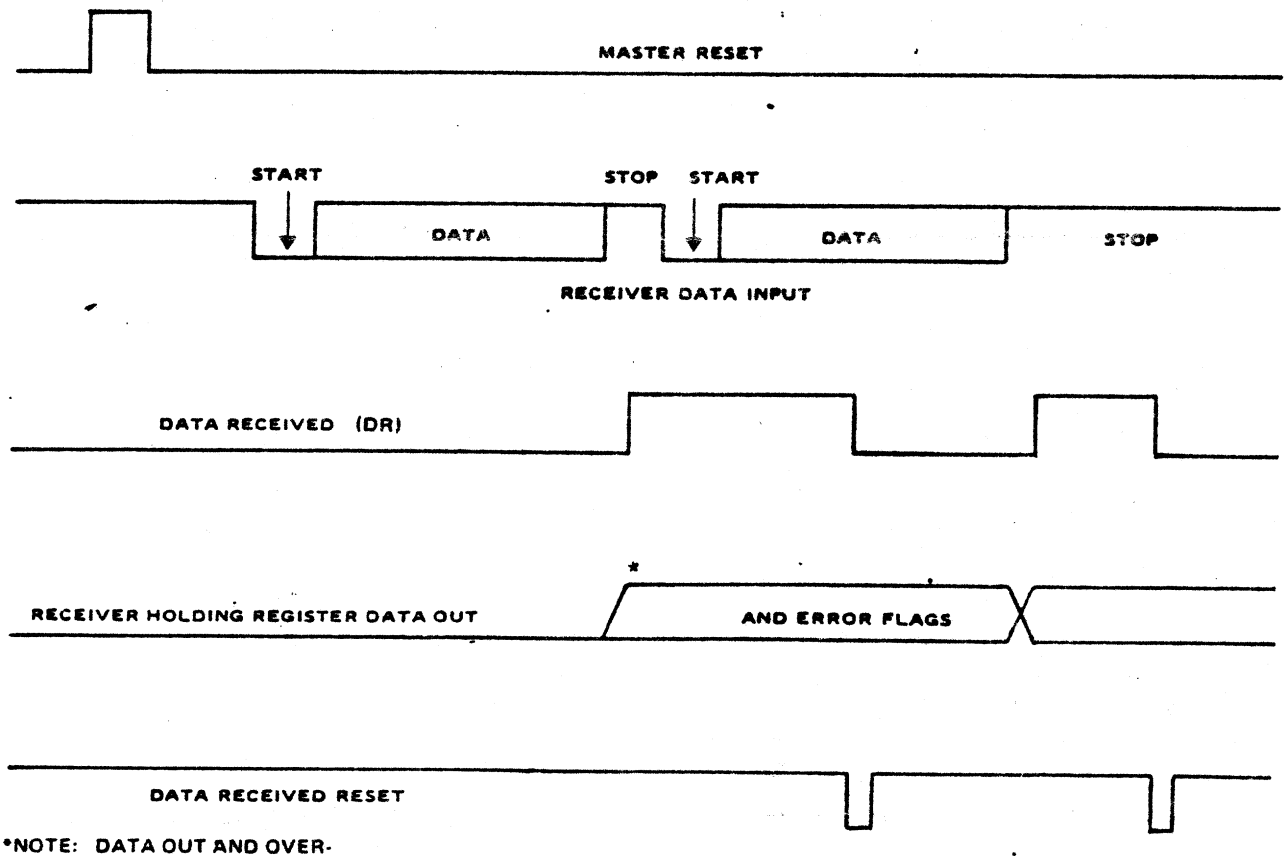


Figure 9. Receiver Timing Diagram

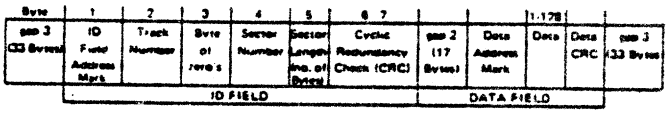
3128 RED HILL AVENUE, BOX 2180
NEWPORT BEACH, CALIFORNIA 92663
(714) 557-3550 TWX 910-595-1139

MARCH, 1978

FLOPPY DISK CONTROLLER APPLICATION NOTE

Introduction

The FD1771 is a MOS/LSI device that performs the function of interfacing a processor to a flexible (Floppy) diskette drive. This single chip replaces nearly 80% of the required disk drive interface electronics. (See figure 1-1). It provides the data accessing controls and the bidirectional transfer of information between the processor's memory and the magnetically stored data on the diskette. The diskette data is stored in a data entry format compatible with the IBM 3740 specification (other formats may be used providing more data storage). In this format all information is recorded on tracks (radial paths) in sectors (arc sections) defined by a programmed header as shown below:



The FD1771 handles single density frequency modulated (FM) data. Each data cell is defined by clock pulses. A pulse recorded between clock pulses identifies the presence of a logic 1 bit; the absence of this pulse is interpreted as a logic 0 bit. The Address Marks for Index, ID, and Data are identified by a particular pattern not repeated in the remainder of the ID field or Data field. This is accomplished by reading patterns that are recorded with missing clock bits (logic 0) as shown below:

Index Address Mark	Data	1 1 1 1 1 1 0 0	=FC
	Clock	1 1 0 1 0 1 1 1	=D7
ID Address Mark	Data	1 1 1 1 1 1 1 0	=FE
	Clock	1 1 0 0 0 1 1 1	=C7
Data Address Mark	Data	1 1 1 1 1 0 1 1	=FB
	Clock	1 1 0 0 0 1 1 1	=C7
Deleted Data Address Mark	Data	1 1 1 1 1 0 0 0	=F8
	Clock	1 1 0 0 0 1 1 1	=C7

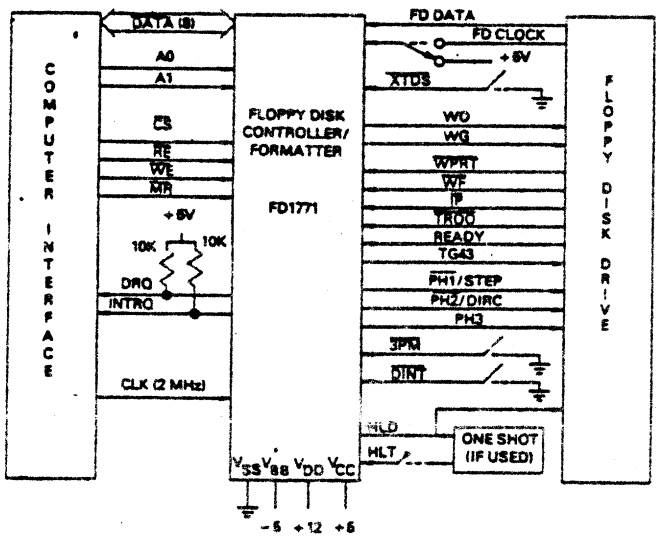
These patterns are used as synchronization codes by the FD1771 when reading data and are recorded by the formatting command, Write Track, when the FD1771 is presented with data F7 through FE.

SECTION I FD1771 DESCRIPTION

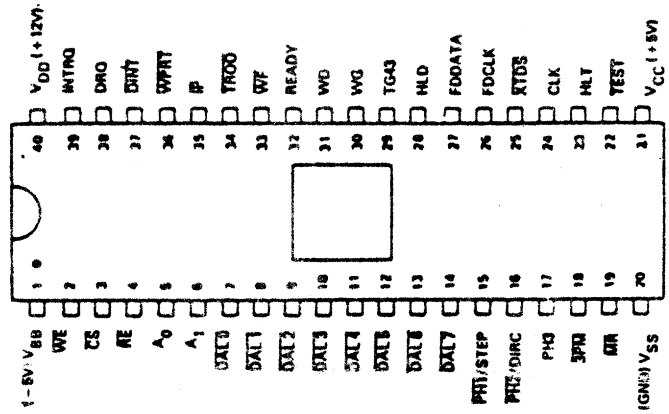
1.1 FD1771 — Flexible Drive Interface (Refer to Figure 1-1 FD1771 Block Diagram)

The FD1771 generates all controls to position the read/write head over the desired track. The FD1771 has the capability of sending successive three phase pulses over the lines PH1, PH2, and PH3 for 3 phase stepping motors or by sending a level over the PH2 line and pulses over the PH1 lines to determine direction and stepping rate for step-direction motors. The particular motor interface is chosen by hardwiring the external pin, 3PM.

ALL REFERENCE TO FD1771 DENOTES FD1771-01 VERSION



FD1771 SYSTEM BLOCK DIAGRAM
FIG 1



A Suffix = Ceramic
B Suffix = Plastic

FD1771 PIN CONNECTIONS
FIG 2

3128 RED HILL AVENUE, BOX 2180
NEWPORT BEACH, CALIFORNIA 92663
(714) 557-3550 TWX 910-595-1139

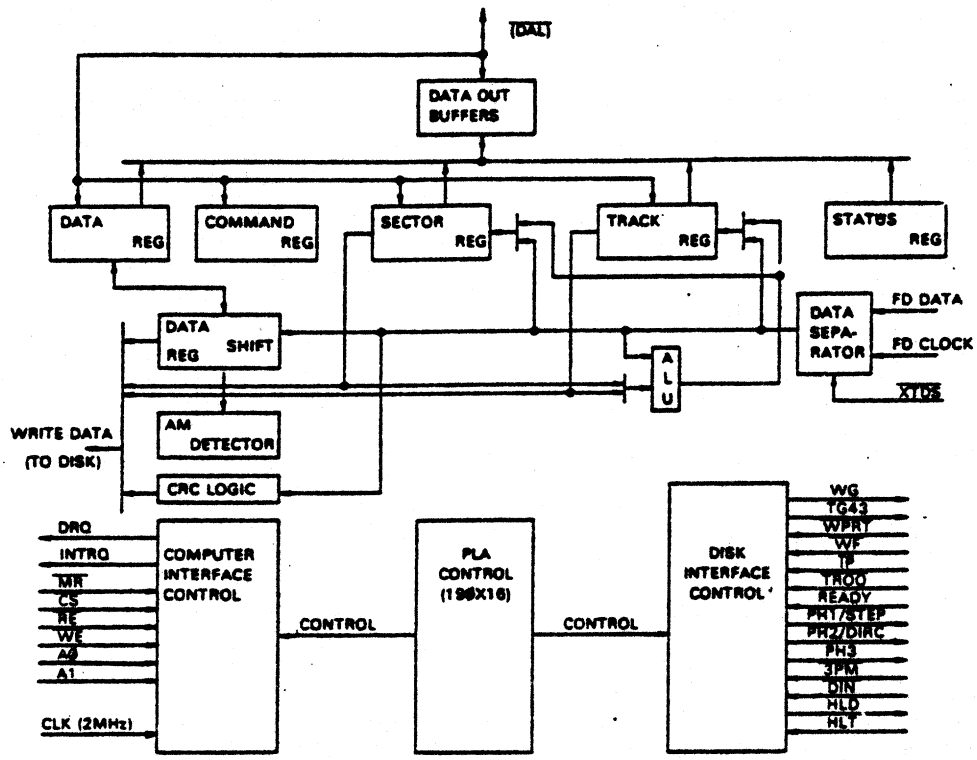


FIGURE 1-1

The head is loaded against the recording media (diskette) by the HLD (Head Load) signal from the FD1771. A read or write operation does not occur until a logic high signal is sampled at the HLT (Head Load Timing) input. This input is sampled after a 10 msec internal delay. This input may be wired high if 10 msec time is sufficient or a one shot may be used to extend this time. If the head is already engaged from a previous operation the resetting of bit 2 in the Read or Write Command (see Processor Interface) will disable the HLT functions and the 10 ms delay.

When reading the serial data from the disk the FD1771 will look for the desired sector to be read, check its ID field and locate its data address mark. All subsequent serial data is assembled in parallel form and presented to the processor interface. The serial data read from the Floppy Driver may be input as composite data, both clock and data present at the FDDATA input, or as separated data in which the data is input to the FDDATA pin and the clock is input to the FD Clock pin.

When writing, information is presented as composite of serial clock and data pulses of 500 nsec periods. With data present at the WD output the WG (Write Gate) signal is activated to allow current to flow in the Read/Write head.

The remaining interface between the FD1771 and the Floppy Drive concerns status information. The $\overline{IP}$ (Index Pulse) and $\overline{TROO}$ (Track 00) signals are outputs of the drive to indicate when the index mark is encountered (once per revolution of the disk) or when the Read/Write head is located over Track 00 respectively.

The $\overline{WPRT}$ (Write Protect), $\overline{DINT}$ (Disk Initialization), and Ready signals reflect the drive condition. The Write Protect signal, when a logic low, prevents the FD1771 from executing a Write Command. The Disk Initialization input, when a logic low, prevents a Write Track Command and essentially disables the rewriting of a format over a previously formatted diskette. The Ready signal indicates Floppy Drive readiness and a logic low on this input prevents any Read or Write command from being executed.

3128 RED HILL AVENUE, BOX 2160
NEWPORT BEACH, CALIFORNIA 92663
(714) 557-3550 TWX 910-596-1139

Other status interface signals are $\overline{WF}$ (Write Fault) from the Drive which signifies a write operation fault such as failure to detect write current when WG is turned on terminating the Current Write command; and the TG43 signal to the drive indicating the track to be written on is located between Track 44 and Track 76. This latter signal is used by the drive to lower the write current on inner tracks and compensate for the higher density recording of these tracks.

1.2 FD1771 — Processor Interface (See figure 1-1)

All commands, status and data are transferred over the 3 state bidirectional $\overline{DAL}$ (Data Access) lines. These 8 lines present an open circuit to the common processor peripheral bus until activated by the $\overline{CS}$ (Chip Select) signal. An active $\overline{CS}$ combined with $\overline{RE}$ (Read Enable) sets the $\overline{DAL}$ into the transmitter mode while the $\overline{CS}$ combined with an active WE (Write Enable) sets the $\overline{DAL}$ in the receiver mode. The information in the FD1771 resides in 5 accessible 8 bit registers. These registers are: (1) The bidirectional Data Register which acts as a parallel buffer for read or write operations, and receives the desired track number to be accessed in seek operation. (2) the Command register which receives and stores commands from the processor. (3) The sector register which receives the desired sector number to be accessed, (4) The track register which contains the present Track position, (5) The Status Register containing information about the present operation.

The accessing of the registers is accomplished by a combination of active levels on the $\overline{CS}$, $\overline{RE}$, or $\overline{WE}$, and the register address lines A1 and A0. The Command Register can only receive information and the Status Register can only transmit information.

Two signals are available to aid in program response to the FD1771. The INTRQ (Interrupt Request) is activated by the controller whenever an operation is completed successfully or terminated by a fault. The DRQ (Data Request) signal is available as an indication of the chips readiness to transfer a byte of data during read or write operations.

A 2MHZ clock is required by the chip as a reference for all timed signals such as motor controls and data transfers. The $\overline{MR}$ (Master Reset) clears the command register and initiates a Restore (seek track 00) Command when the $\overline{MR}$ line is returned to an inactive state.

1.3 FD1771 Instructions

The FD1771 can be considered a specialized microprocessor with its own instruction repertoire. These are listed in the Tables below.

The Restore, Seek, and the three Step commands position the Read/Write head over the desired track. The Restore positions it over Track 00, the Seek poisitions it over the track specified in the Data Register, and the Step Commands position the head over an adjacent track to its present position.

The Step In moves the head inward toward the center of the disk while the Step Out moves it outward from the center. The Step Command moves the head one step in the same direction as the previous command.

The Read and Write commands are the normally executed commands when transferring information. The Read command initiates a search for a track and sector code in the ID field equal to that in the track and sector registers. When found, the data is formatted from serial to parallel and presented to the Data Register along with the setting of the DRQ signal. By setting of bit 4 in the Read (or Write) command all data records from the desired sector until the last sector on the track are sequentially assembled. The setting of bit 3 allows other combinations of byte count per sector than the standard IBM format.

The Write Command operates similar to the Read Command in multiple sector and variable sector length. All received words in the Data register are transferred to the shift register at which time the DRQ line is set. Four separate Data address marks are selectable through bits 1 and 0 which are written on the diskette prior to writing the sector data.

The Read Address command provides the next encountered ID field (6 bytes) on the diskette to the processor. This can be used to identify the track over which the head resides and can be used if one were to multiplex between two or more drives and wish to return to the first drive. This could also be accomplished by storing the track register in memory and returning it when reactivating the first drive.

The Write Track command is basically used for formatting. Once the index position is located the FD1771 will request data and transfer it to the disk including all ID fields, gaps, and Data fields. Special address marks and the CRC characters are written by detecting certain data patterns. The Read track command allows the reading of the entire recorded pattern on a track including gaps. (Refer to Data Sheet for formatting details)

The final command is the Force interrupt which can be loaded into the Command register at any time. This will terminate any present operation and can also generate an interrupt under four selectable conditions.

1.4 Status Register (See Table 1, page 16)

This register contains status information associated with each of the command instructions. Bit 7 always reflects the Ready condition of the Drive while bit 0 (Busy) always defines the status of the FD1771 concerning present operations.

COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	$\bar{s}$
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

COMMAND FLAG SUMMARY

TYPE I

h = Head Load flag (Bit 3)

h=1, Load head at beginning
h=0, Do not load head at beginning

V = Verify flag (Bit 2)

V=1, Verify on last track
V=0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)

r_1r_0=00, 6ms between steps
r_1r_0=01, 6 ms between steps
r_1r_0=10, 10ms between steps
r_1r_0=11, 20ms between steps

u= Update flag (Bit 4)

u=1, Update Track register
u=0, No update

In general bit 1 reflects the state of the external DRQ signal while bit 2 indicates lost data due to overrun or underrun conditions. The Type 1 or head positioning instructions use bit 1 and 2 as a reflection of the $\overline{IP}$ and $\overline{TROO}$ inputs respectively.

Bit 3 normally indicates the encounterance of a CRC error in the ID or Data fields except for Read Track and Write Track commands in which the CRC is not checked. Bit 4 indicates that the desired track or sector was not correctly located. Bit 6 reflects the $\overline{WP}$ input on Seek and Write Commands and combines with bit 5 to identify the encountered data address mark on the Read command. Bit 5 also indicates the head engaged status on Seek commands and Write fault or Write commands.

TYPE II

m = Multiple Record flag (Bit 4)

m=0, Single Record
m=1, Multiple Records

b = Block length flag (Bit 3)

b=1, IBM format (128 to 1024 bytes)
b=0, Non-IBM format (16 to 4096 bytes)

a_1a_0 = Data Address Mark (Bits 1-0)

a_1a_0=00, FB (Data Mark)
a_1a_0=01, FA (Data Mark)
a_1a_0=10, F9 (Data Mark)
a_1a_0=11, F8 (Data Mark)

TYPE III

s = Synchronize flag (Bit 0)

$\bar{s}$=0, Synchronize to AM
$\bar{s}$=1, Do not synchronize to AM

TYPE IV

Ii = Interrupt Condition flags (Bits 3-0)

I_0=1, Not Ready to Ready Transition
I_1=1, Ready to Not Ready Transition
I_2=1, Index Pulse
I_3=1, Immediate Interrupt

E=Enable HLD and 10 msec Delay

E=1, Enable HLD, HLT and 10 msec Delay
E=0, Head is assumed Engaged and there is no 10 msec Delay

3128 RED HILL AVENUE, BOX 2180
NEWPORT BEACH, CALIFORNIA 92663
(714) 557-3550 TWX 910-595-1139

PIN NO	PIN NAME	SYMBOL	FUNCTION
Computer Interface:			
7-14	DATA ACCESS LINES	$\overline{DAL0}$-$\overline{DAL7}$	• Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by $\overline{WE}$ or a transmitter enabled by $\overline{RE}$.
3	CHIP SELECT	$\overline{CS}$	• A logic low on this input selects the chip and enables computer communication with the device.
5,6	REGISTER SELECT LINES	A0, A1	•These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: A1 A0 $\overline{RE}$ $\overline{WE}$ 0 0 Status Reg Command Reg 0 1 Track Reg Track Reg 1 0 Sector Reg Sector Reg 1 1 Data Reg Data Reg
4	READ ENABLE	$\overline{RE}$	•A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
2	WRITE ENABLE	$\overline{WE}$	•A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
38	DATA REQUEST	DRQ	•This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operation, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	•This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register. Use 10K pull-up resistor to +5.
24	CLOCK	CLK	•This input requires a free-running 2 MHz + 1% square wave clock for internal timing reference.
Floppy Disk Interface:			
25	EXTERNAL DATA SEPERATION	XTDS	•A logic low on this input selects external data separation. A logic high or open selects the internal data separator.
26	FLOPPY DISK CLOCK (External Separation)	FDCLOCK	•This input receives the externally separated clock when $\overline{XTDS}$ = 0. If $\overline{XTDS}$ = 1, this input should be tied to a logic high.
27	FLOPPY DISK DATA	FDDATA	•This input receives the raw read disk data if XTDS = 1, or the externally separated data if XTDS = 0.
31	WRITE DATA	WD	•This output contains both clock and data bits of 500 ns duration.
28	HEAD LOAD	HLD	•The HLD output controls the loading of the Read-Write head against the media the HLT input is sampled after 10 ms. When a logic high is sampled on the HLT input the head is assumed to be engaged.
23	HEAD LOAD TIMING	HLT	
15	Phase 1/Step	PH1/STEP	•If the 3PM input is a logic low the three phase motor control is selected and PH1, PH2, and $\overline{PH3}$ outputs form a one active low signal out of three. PH1 is active low after MR. If the 3PM input is a logic high the step and direction motor control is selected. The step output contains a 4usec high signal for each step and the direction output is active high when stepping, active low when stepping out.
16	Phase 2/Direction	PH2/DIRC	
17	Phase 3	$\overline{PH3}$	
18	3 Phase Motor Select	3PM	

3128 RED HILL AVENUE, BOX 2180
NEWPORT BEACH, CALIFORNIA 92663
(714) 557-3550 TWX 910-595-1139

PIN NO.;	PIN NAME;	SYMBOL;	FUNCTION
29	Track Greater Than 43	TG43	•This output informs the drive that the Read-Write head is positioned between track 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	•This output is made valid when writing is to be performed on the diskette.
32	Ready	READY	•This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. A Seek operation is performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$	$\overline{\text{WF}}$	•This input detects writing faults indications from the drive. When WG = 1 and $\overline{\text{WF}}$ goes low the current Write command is terminated and the Write Fault status bit is set. The $\overline{\text{WF}}$ input should be made inactive (high) when WG becomes inactive.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	•This input informs the FD1771 that the Read-Write head is positioned over Track 00 when a logic low.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	•Input, when low for a minimum of 10 usec, informs the FD1771 when an index mark is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	•This input is sampled whenever a Write Command is received. A logic low terminated the command and sets the Write Protect Status bit.
37	$\overline{\text{DISK INTIALIZATION}}$	$\overline{\text{DINT}}$	•The input is sampled whenever a Write Track command is received. If $\overline{\text{DINT}}$ = 0, the operation is terminated and the Write Protect Status bit is set.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	•This input is used for testing purposes only and should be tied to +5V or left open by the user.

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

WESTERN DIGITAL
CORPORATION
3128 RED HILL AVENUE P.O. BOX 2180
NEWPORT BEACH, CALIFORNIA 92663
TELEPHONE: (714) 557-3550
TWX: 910-595-1139

SECTION 9: APPENDIX

LNW RESEARCH

THANK YOU FOR YOUR RECENT PURCHASE OF OUR 'SYSTEM EXPANSION.' WE ARE CURRENTLY OFFERING TWO SETS OF PARTS AT A SPECIAL LOW PRICE. PLEASE MAIL THE BOTTOM OF THIS FORM ALONG WITH YOUR REMITTANCE TO LNW RESEARCH, P.O. Box 16216 Irvine, CA 92713

KIT 1

QUANTITY	PART TYPE	DESTINATION
1	74LS04	U18
2	74LS240	U8,15
2	74LS241	U37,38
4	74LS244	U34,35,36,39
1	4 MHZ CRYSTAL	Y1
2	MPU131	Q1,2

KIT 2

QUANTITY	PART TYPE	DESTINATION
1	FD1771A/B-01	U14
1	TR1602B	U40

WE'LL BE HAPPY TO HONOR YOUR PERSONAL CHECK, MONEY ORDER, VISA OR MASTER CHARGE. VISA OR MASTER CHARGE TELEPHONE ORDERS WILL BE ACCEPTED. CALL (714) 641-8850.

KIT 1 PRICE		
NO. OF SETS	PRICE/SET	TOTAL PRICE
	$27.50	
SHIPPING & HANDLING	$ 2.00*	
CA SALES TAX	$ 1.65	
TOTAL PAYMENT ENCLOSED		

KIT 2 PRICE		
NO. OF SETS	PRICE/SET	TOTAL PRICE
	$30.00	
SHIPPING & HANDLING	$ 2.00*	
CA SALES TAX	$ 1.80	
TOTAL PAYMENT ENCLOSED		

*IF BOTH KIT 1 AND KIT 2 ARE PURCHASED, THE SHIPPING & HANDLING IS $3.00.

CARD NO._____ EXP. DATE:_____ SIGNATURE:_____

NAME (PRINT):_____ ADDRESS:_____

CITY, STATE: _____ ZIP CODE: _____

LNW RESEARCH P.O. BOX 16216 IRVINE, CALIFORNIA 92713

LIMITED WARRANTY

LNW Research warrants the P.C. Board from manufactured defects for a period of ninety (90) days.

LNW Research does not offer or imply any other warranty.

*TRS-80 is a product of Tandy Corporation.

```
5 REM  BASIC SERIAL PRINTER PROGRAM
7 REM  THIS PROGRAM ALLOWS THE USE OF A SERIAL PRINTER WITH
9 REM  THE LNW RESEARCH SYSTEM EXPANSION CIRCUIT BOARD
15 REM POKE NEW DCB TYPE AND ADDRESS INTO RAM (4025H)
20 POKE 16421,2:POKE 16422,0:POKE 16423,127
25 REM POKE RS232 DRIVER PROGRAM INTO MEMORY (7F00)
30 FOR X=32512 TO 32560
50 READ Y
60 POKE X,Y
70 NEXT X
75 END
80 DATA 245,58,48,127,254,1,40,15
90 DATA 62,1,50,48,127,211,232,219
100 DATA 233,230,248,246,4,211,234,241
110 DATA 219,232,203,119,32,250,219,234
120 DATA 203,119,40,244,121,211,235,254
140 DATA 13,32,4,14,10,24,233,201,0
```

```
                    00100 ;        SERIAL PRINTER INITIALIZATION PROGRAM
                    00110 ;
                    00120 ;  THIS PROGRAM,WHEN EXECUTED UPON POWER UP ALLOWS THE
                    00130 ;USE OF A SERIAL PRINTER WITH THE LNW RESEARCH EXPANSION
                    00140 ;CIRCUIT BOARD SERIAL INTERFACE WITH THE PARALLEL/SERIAL
                    00150 ;MOD.THIS ALLOWS THE USE OF A SERIAL PRINTER EVEN THOUGH
                    00160 ;THE SOFTWARE SUPPORTS ONLY THE CENTRONICS/RADIO SHACK
                    00170 ;PRINTER.THIS MAKES YOUR SERIAL PRINTER COMPATIBLE WITH
                    00180 ;ALL RADIO SHACK SOFTWARE WITHOUT RESIDENT SOFTWARE
                    00190 ;DRIVERS.
                    00200 ;
00E8                00210 RESURT   EQU     0E8H     ;OUTPUT HERE RESETS UART
00E9                00220 SWITCH   EQU     0E9H     ;IN HERE READS THE SENSE JUMPERS
00EA                00230 CNTREG   EQU     0EAH     ;OUT LOADS UART CONTROL REGISTER
7F00                00240          ORG     32512    ;STARTS AT 7F00H
7F00 F5             00250 START    PUSH    AF       ;SAVE A AND F REGISTERS
7F01 3E01           00260          LD      A,01H    ;LOAD SOMETHING INTO A
7F03 D3E8           00270          OUT     (RESURT),A       ;RESET UART
7F05 DBE9           00280          IN      A,(SWITCH)       ;INPUT SENSE JUMPERS
7F07 E6F8           00290          AND     0F8H     ;MASK OFF LOWER 3 BITS (UNUSED)
7F09 F604           00300          OR      04H      ;SETS BRK IN UART
7F0B D3EA           00310          OUT     (CNTREG),A       ;LOAD UART WITH IMAGE OF
                    00320 ;SENSE JUMPERS.D0-D2(NOT USED),D3=1(PARITY INHIBIT),
                    00330 ;D4=1(2 STOP BITS),D4=0(1 STOP BIT),D5-D6 SELECT WORD
                    00340 ;LENGTH(5-8),D7=1(PARITY EVEN),D7=0(PARITY ODD)
                    00350 ;
7F0D F1             00360 RESTOR   POP     AF       ;RESTORE REGISTERS A AND F
7F0E C32D40         00370          JP      402DH    ;BACK TO ENTRY OF DOS
7F00                00380          END     START
00000 TOTAL ERRORS

RESTOR  7F0D
START   7F00
CNTREG  00EA
SWITCH  00E9
RESURT  00E8
```

```
                        00001 ;         SERIAL CRT TERMINAL PROGRAM
                        00002 ;
                        00003 ;  THIS PROGRAM ALLOWS THE USE OF THE LNW SYSTEM
                        00004 ; EXPANSION CIRCUIT BOARD AS A CRT TERMINAL.THIS
                        00005 ; PROGRAM CAN ALSO BE USED FOR TESTING THE SERIAL
                        00006 ; INTERFACE BY SHORTING E1 AND E3 TOGETHER.
                        00007 ;
0033                    00008 DSP       EQU     33H
002B                    00009 KBD       EQU     2BH
7000                    00010           ORG     7000H   ;START AT 7000H
                        00011 ;
7000 3E1C               00012 START     LD      A,1CH   ;HOME CURSOR
7002 CD3300             00013           CALL    DSP
7005 3E1F               00014           LD      A,1FH   ;CLEAR SCREEN
7007 CD3300             00015           CALL    DSP
700A 3E0E               00016           LD      A,0EH   ;TURN ON CURSOR
700C CD3300             00017           CALL    DSP
700F D3E8               00018 IUART     OUT     (MR),A  ;RESET UART WITH ANYTHING
7011 DBE9               00019           IN      A,(CONFIG)      ;GET TERM CONFIG. JUMPERS
7013 E6F8               00020           AND     0F8H    ;MASK OFF LOWER 3 UNUSED BITS
7015 F605               00021           OR      05H     ;SET BRK,RESET DTR,SET RTS
7017 D3EA               00022           OUT     (CTRL),A        ;PUT IN CONTROL REG.
7019 DBEA               00023 RSRD      IN      A,(CTRL)
701B CB7F               00024           BIT     7,A     ;IS REC. DATA AVAIL?
701D 2817               00025           JR      Z,SEROUT
701F DBEB               00026           IN      A,(DATA)        ;GET DATA
7021 B7                 00027           OR      A
7022 2812               00028           JR      Z,SEROUT        ;IF NO INPUT,LOOK TO OUT
7024 E67F               00029           AND     7FH     ;REMOVE PARITY
7026 FE60               00030           CP      60H
7028 FA2D70             00031           JP      M,$+5
702B E65F               00032           AND     5FH     ;LOWER TO UPPER CASE
702D FE0A               00033           CP      0AH
702F 28E8               00034           JR      Z,RSRD
7031 CD3300             00035           CALL    DSP     ;DISPLAY CHARACTER
7034 18E3               00036           JR      RSRD
7036 CD2B00             00037 SEROUT    CALL    KBD     ;INPUT FROM KEYBOARD?
7039 B7                 00038           OR      A
703A 28DD               00039           JR      Z,RSRD  ;IF NOTHING THEN BACK TO INPUT
703C FE05               00040           CP      05H
703E F24970             00041           JP      P,NOSPCH        ;NOT A SPECIAL CHARACTER
7041 215870             00042           LD      HL,SPCHTB-1     ;SPECIAL CHARACTER TBL
7044 4F                 00043           LD      C,A
7045 0600               00044           LD      B,0
7047 09                 00045           ADD     HL,BC   ;HL POINTS TO SPEC. CHARACTER
7048 7E                 00046           LD      A,(HL)  ;GET SPECIAL CHARACTER CODE
```

```
7049 FE1A      00047 NOSPCH   CP       01AH
704B 28CC      00048          JR       Z,RSRD   ;IS SHIFT DOWN ARROW? IGNORE
704D 4F        00049 RSWR     LD       C,A      ;SAVE DATA
704E DBEA      00050          IN       A,(CTRL)         ;GET UART STATUS
7050 CB77      00051          BIT      6,A      ;IS TRANSMIT REG EMPTY?
7052 28F9      00052          JR       Z,RSWR   ;IF NOT LOOP
7054 79        00053          LD       A,C      ;PUT CHARACTER IN A
7055 D3EB      00054          OUT      (DATA),A         ;OUTPUT DATA
7057 18C0      00055          JR       RSRD     ;BACK TO INPUT ROUTINE
7059 03        00056 SPCHTB   DEFB     03H      ;DEFAULT:EOT-CNT"A"
705A 1B        00057          DEFB     1BH      ;DEFAULT:ESC-CNT"B"
705B 7C        00058          DEFB     7CH      ;DEFAULT:VERT BAR-CNTRL"C"
705C 7F        00059          DEFB     7FH      ;DEFAULT:DEL-CNTRL"D"
00E8           00060 MR       EQU      0E8H
00E9           00061 CONFIG   EQU      0E9H
00EA           00062 CTRL     EQU      0EAH
00EB           00063 DATA     EQU      0EBH
7000           00064          END      START
00000 TOTAL ERRORS

RSWR    704D
SPCHTB  7059
NOSPCH  7049
DATA    00EB
SEROUT  7036
RSRD    7019
CTRL    00EA
CONFIG  00E9
MR      00E8
IUART   700F
START   7000
KBD     002B
DSP     0033
```

```
                    00001 ;        SERIAL PRINTER DRIVER PROGRAM
                    00002 ;
                    00003 ;    THIS PROGRAM ALLOWS THE USE OF A SERIAL PRINTER
                    00004 ;WITH THE LNW RESEARCH SYSTEM EXPANSION CIRCUIT BOARD.
                    00005 ;THIS DRIVER PROGRAM IS LEFT IN MEMORY AT A LOCATION
                    00006 ;WHICH IS UNALTERED BY BASIC AND BY USER PROGRAMS.THE
                    00007 ;PROGRAM IS EXECUTED DURING EVERY LPRINT AND LLIST FOR
                    00008 ;EACH CHARACTER TO BE PRINTED.HANDSHAKING IS SUPPORTED
                    00009 ;AS THE SOFTWARE READS THE PRINTER BUSY (DSR) BEFORE
                    00010 ;OUTPUTING A CHARACTER. N O T E : IN ORDER FOR THIS
                    00011 ;PROGRAM TO BE EXECUTED,THE LINE PRINTER CONTROL BLOCK
                    00012 ;AT HEX 4025 TO 4027 MUST BE ALTERED BEFORE PRINTING
                    00013 ;TO IDENTIFY THE PRINTER TYPE AND DRIVER ADDRESS.THE
                    00014 ;FOLLOWING LIST GIVES YOU THESE VALUES.
                    00015 ;        16421D   4025H   DCB TYPE                02H 002D
                    00016 ;        16422D   4026H   LSB DRIVER ADDR.        00H 000D
                    00017 ;        16423D   4027H   MSB DRIVER ADDR.        7FH 127D
                    00018 ;
                    00019 ;
00E8                00020 RESURT   EQU      0E8H     ;OUT HERE RESETS UART,IN READS RS232
 CONTROL BITS
00E9                00021 SWITCH   EQU      0E9H     ;IN READS SENSE JUMPERS
00EA                00022 CNTREG   EQU      0EAH     ;OUT HERE LOADS UART CONTROL REG. IN
 READS UART STATUS
00EB                00023 DTAREG   EQU      0EBH     ;OUT LOADS UART XMIT HOLDING REG.,IN
 READS RECIEVED DATA
7F00                00024          ORG      32512    ;STARTS AT 7F00H
7F00 F5             00025 START    PUSH     AF       ;SAVE A AND F REGISTERS
7F01 3A307F         00026          LD       A,(FLAG)         ;INPUT INITIALIZE FLAG
7F04 FE01           00027          CP       01H      ;IF =1,THEN ALREADY INITIALIZED
7F06 280F           00028          JR       Z,RESTOR         ;GO AND OUTPUT IF A=0
7F08 3E01           00029          LD       A,01H    ;PUT 1 IN A
7F0A 32307F         00030          LD       (FLAG),A         ;OUTPUT 1 TO FLAG
7F0D D3E8           00031          OUT      (RESURT),A       ;RESET UART
7F0F DBE9           00032          IN       A,(SWITCH)       ;READ SENSE JUMPERS
7F11 E6F8           00033          AND      0F8H     ;MASK OFF LOWER 3 BITS (NOT USED)
7F13 F604           00034          OR       04H      ;RESET RTS,DTR,SET BRK
7F15 D3EA           00035          OUT      (CNTREG),A       ;LOAD UART WITH IMAGE OF
                    00036 ;SENSE JUMPERS.D0-D2(NOT USED),D3=1(PARITY INHIBIT),
                    00037 ;D4=1(2 STOP BITS),D4=0(1 STOP BIT),D5-D6 SELECT WORD
                    00038 ;LENGTH(5-8),D7=1(PARITY EVEN),D7=0(PARITY ODD)
                    00039 ;
```

```
7F17 F1        00040 RESTOR  POP     AF        ;RESTORE A AND F REGISTERS
7F18 DBE8      00041 STATIN  IN      A,(RESURT)        ;READ R232 STATUS
7F1A CB77      00042         BIT     6,A       ;CHECK DSR
7F1C 20FA      00043         JR      NZ,STATIN         ;IF NOT ZERO,LOOP TILL ZERO
7F1E DBEA      00044         IN      A,(CNTREG)        ;INPUT UART STATUS
7F20 CB77      00045         BIT     6,A       ;CHECK TRANSMIT REGISTER EMPTY
7F22 28F4      00046         JR      Z,STATIN          ;IF 0 (NOT EMPTY),LOOP
7F24 79        00047         LD      A,C       ;LOAD A WITH CHARACTER FOR OUTPUT
7F25 D3EB      00048         OUT     (DTAREG),A        ;OUTPUT CHARACTER TO UART
7F27 FE0D      00049         CP      0DH       ;WAS IT A CARRIAGE RETURN?
7F29 2004      00050         JR      NZ,RETRN          ;RETURN IF NOT
7F2B 0E0A      00051         LD      C,0AH     ;IT WAS SO OUTPUT LINE FEED ALSO
7F2D 18E9      00052         JR      STATIN    ;GO BACK AND OUTPUT LF
7F2F C9        00053 RETRN   RET     ;RETURN TO CALLING CODE
7F30 00        00054 FLAG    DEFB    00H       ;INITIALIZATION FLAG
0000           00055         END
00000 TOTAL ERRORS

RETRN   7F2F
STATIN  7F18
RESTOR  7F17
FLAG    7F30
START   7F00
DTAREG  00EB
CNTREG  00EA
SWITCH  00E9
RESURT  00E8
```

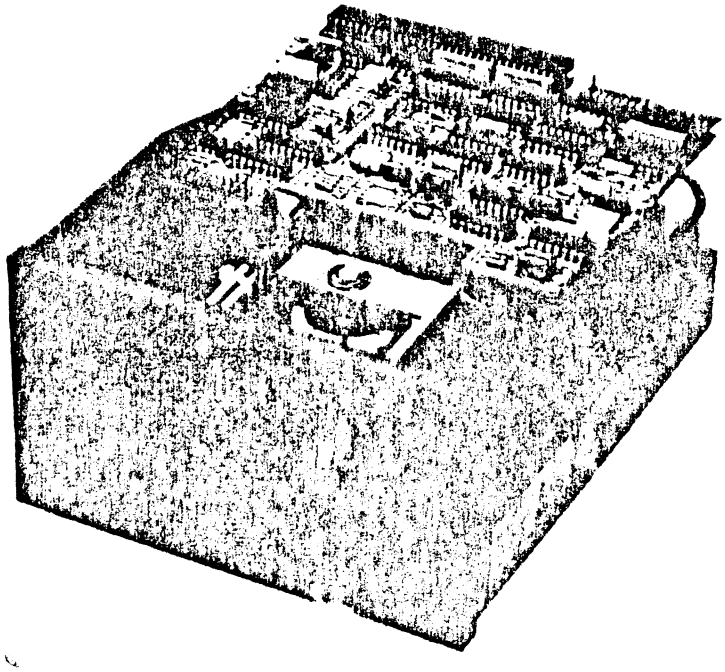
MPI

MICRO PERIPHERALS INC.

FLEXIBLE DISK DRIVE

MODEL 51/52

PRODUCT MANUAL



electronics international bv

adm. banckertweg 22, postbus 443, 2300 AK leiden,
nederland, telefoon 071-146045*, telex 39420

TABLE OF CONTENTS

SECTION I – INTRODUCTION

1.1 General
1.2 Purpose of Equipment
1.3 Physical Description
1.4 Functional Description

SECTION II – INSTALLATION AND CHECKOUT

2.1 Scope . . . 3
2.2 Unpacking . . . 3
2.3 Installation . . . 3
2.4 Hardware . . . 3
2.5 Dust Cover . . . 3
2.6 Cooling . . . 3
2.7 Drive Separation . . . 3
2.8 Input/Output Cable . . . 3
2.9 DC Power . . . 4
2.10 Initial Checkout . . . 4

SECTION III – INTERFACING REQUIREMENTS

3.1 General . . . 4
3.2 Input Lines . . . 4
3.2.1 Line Termination . . . 4
3.2.2 Programmable Shunt . . . 4
3.2.3 Drive Select 1 to 4 . . . 4
3.2.4 Motor On . . . 4
3.2.5 Direction Select . . . 5
3.2.6 Step . . . 5
3.2.7 Write Gate . . . 6
3.2.8 Write Data . . . 6
3.2.9 Side Select . . . 6
3.2.10 In Use (Optional) . . . 6
3.3 Output Lines . . . 6
3.3.1 Track 00 . . . 6
3.3.2 Index/Sector . . . 6
3.3.3 Write Protect . . . 6
3.3.4 Read Data . . . 6
3.4 Connector J2 . . . 6
3.5 Connector J1 . . . 6

SECTION IV – OPERATION

4.1 General . . . 8
4.2 Operating Instructions . . . 8
4.2.1 Flexible Diskette Loading . . . 8
4.2.2 Flexible Diskette Removal . . . 8
4.3 Diskette Handling Recommendations . . . 9

SECTION V – THEORY OF OPERATION

5.1 General . . . 9
5.2 Mechanical and Electrical . . . 10
5.3 Diskette Spindle Drive . . . 10
5.4 Head Load Mechanism . . . 10
5.5 Track 00 . . . 10
5.6 Head Positioning Control . . . 10
5.7 Write Protect Sensor . . . 10
5.8 Index Sensor . . . 10
5.9 Data Recording and Retrieving . . . 10
5.9.1 Data Recording . . . 10
5.9.2 Data Retrieving . . . 12

TABLE OF CONTENTS, Continued

		Page
	›VERY	
	s	.13
	..rors	.13
6.3	Read Errors	.13
SECTION VII – MAINTENANCE		
7.1	General	.13
7.2	Cleaning Read/Write Head	.13
7.3	Adjustment Procedures	.13
	7.3.1 Radial-Track Alignment	.13
	7.3.2 Index-to-Data Alignment	.13
	7.3.3 Track 00 Sensor Alignment	.13
	7.3.4 Speed Control	.14
	7.3.5 Track 00 End Stop	.14

LIST OF ILLUSTRATIONS

Figure		Page
1-1	Outline and Mounting Dimensions	1
3-1	Track Access Timing	5
3-2	Read Initiate Timing	5
3-3	Read Signal Timing	5
3-4	Write Initiate Timing	5
3-5	Write Data Timing	5
3-6	General Control and Data Timing	5
3-7	Index Sector Timing (soft sector)	5
3-8	Index Sector Timing (hard sector)	5
3-9	DC Power Connector, J2	6
3-10	J1 Connector Dimensions	6
3-11	Interface Signals	7
3-12	Shunt Configuration	7
3-13	Write Protect Option	8
4-1	Diskette Orientation	8
5-1	Functional Block Diagram	9
5-2	Stepper Motor Logic	.11
5-3	Read/Write Logic	.11
5-4	Drive Motor Control Logic	.11
5-5	Basic Recording Technique	.12
5-6	Wave Forms in Read Sequence	.12
7-1	Component Location	.14

LIST OF TABLES

Table		Page
1-1	Specifications	2
1-2	Power Requirements	2
1-3	Environmental	2
1-4	Data Capacity Unformatted (K Bytes)	3
2-1	Recommended Connectors, P1	3

SECTION I

1. INTRODUCTION

1.1 General. This section provides a physical and functional description, and specifications for the Model 51/52 Flexible Disk Drives, manufactured by Micro Peripherals, Inc. In addition to the standard features described, the following additional features are included in all models:

a. "Write Protect" can be used instead as "Disk Installed" indication.

b. When using FM-encoding, an additional board can be plugged on for Data separation.

c. Termination of I/O lines can be either 150 ohms or split 220/330 ohms.

1.2 Purpose of equipment. The Model 51/52 Disk Drive is a compact disk memory device designed for random-access data storage, data entry, and data output applications. Typical applications are intelligent terminal controllers, micro-computers, word processing systems, data communications systems, error logging, micro-program logging, and point-of-sale terminals. Model 51/52 is designed to meet and perform to ANSI specification.

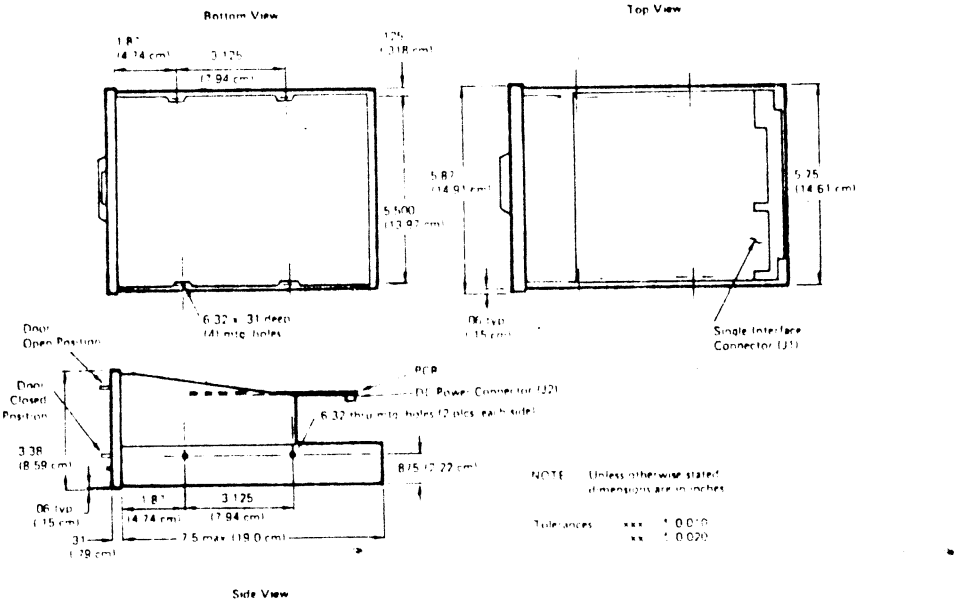


Figure 1-1 Outline and Mounting Dimensions

1.3 Physical description. Model 51/52 can be mounted vertically or horizontally. However, when mounted horizontally, it is recommended that the 51/52 be positioned so that the PCB is on the top side. The mechanical components consist of an aluminum chassis, on which is mounted a spindle (belt-driven by a dc motor); a stepper motor/band combination for positioning the magnetic head assembly; and a cone/clutch assembly for centering and holding the recording media under operation. Access for diskette loading is at the front of the drive. The recording-head assembly is of a glass bonded ferrite/ceramic structure, with lifetime expectancy in excess of 20,000 hours. The electronic circuitry is mounted on a PCB located on top of the drive. Power and interface signals plug directly into this board. The following basic circuits are included:

a. Stepper motor control logic.

b. Read circuit.

c. Write/Erase circuit.

d. Spindle motor speed control.

e. Index; Track 00 and Write Protect sensing.

f. Head load driver.

1.4 Functional description. Model 51/52 is self-contained and requires no operator intervention during operation. The drive consists of a media-rotating system, a head-load and positioning system, and a write/erase and read system. When the

front door is opened, access for inserting the diskette is provided. When inserting the diskette, all positions except in/out are controlled by physical guides internally. Correct in/out is assured by inserting the diskette until a "click" is heard. Closing the front door activates the cone/clutch system which serves two purposes in the following order:

a. Correct centering of the media.

b. Clamping the media to the spindle hub.

The spindle hub rotates at a constant speed of 300 rpm by means of a dc motor/tachometer and a reference in a closed-loop system. When in operation, it is important that the head-to-media relationship be controlled. This is accomplished by the head-load system in the following way: The media is pressed against a reference platen which is referenced to the head and the spindle hub; and a pressure pad is loaded against the media on the opposite side of the head with a force of approximately 17gr. The recording head is positioned over the correct track by means of a four-phase stepper motor band direct-drive mechanism, and its associated electronics. A one-step movement causes a one-track movement. With band positioning, very high step rates can be accomplished with the 51/52 system. When a Write Protected diskette is inserted, the write protect sensor normally disables the write/erase circuits in the drive. When writing, a .013 inches (nominal) data track is recorded, followed by a tunnel erase which trims the track down to .012 inches (nominal). Data recovery electronics include a low-frequency amplifier, a differentiator, a cross-over detector, a digital filter, and a final pulse generator. For FM recording, a data decoder may be added to achieve separated clock and data pulses on the I/O connector.

SPECIFICATIONS

TABLE 1-1

GENERAL

Parameter	Characteristics
Media	ANSI standard 5¼-inch diskette
Number of Tracks	40/51 70/52
Track Density	48 TPI
Start/Stop Time	.5 sec
Rotational Speed	300 rpm ± 1½%
Average latency	100 msec
Head loading time	35 msec
Access time	5 msec, track-to-track
Head settling time	15 msec
Head life	20,000 hours
Media life	3×10^6 passes on single track
Recording method	FM, MFM, M^2FM, GCR
Recording density (FM)	2810/5620 bpi
Flux density	5620 fci max.
Data-transfer rate	125K/250K bits/sec
Power up Delay	1 sec
PHYSICAL	
Height	3.25 inches (8.255 cm)
Width	5.75 inches (14.605 cm)
Length	7.5 inches (19.05 cm)
Weight	3.0 pounds (1.36 kg)

POWER REQUIREMENTS

TABLE 1-2

Power	+12 VDC ± 5%, 1.5A
	+5 VDC ± 5%, 0.7A
Typical Power Dissipation	15W Operation
	6W Standby

ENVIRONMENTAL

TABLE 1-3

Parameter	Characteristics
Operating Temperature	40° to 115°F (4.4°C to 46.1°C)
Relative Humidity	20 to 80% (noncondensing)

DATA CAPACITY UNFORMATTED (K BYTES)
TABLE 1-4

Parameter	Single Density (FM)		Double Density (MFM, M^{2}FM)	
	51	52	51	52
Track	3.13	3.13	6.25	6.25
Disk	125	218.8	250	437.5

RECOMMENDED CONNECTORS – P1
TABLE 2-1

TYPE OF CABLE	MANUFACTURER	CONNECTOR P/N	CONTACT P/N
Twisted Pair 26 Flat Cable	AMP 3M "Scotchflex"	583717-5 3463-0001	1-583616-1 N.A.

SECTION II

2. INSTALLATION AND CHECKOUT

2.1 Scope. This section provides the information and procedures necessary to place Model 51/52 Flexible Disk Drives into operation.

2.2 Unpacking. During unpacking, care must be exercised to ensure that all tools are non-magnetic and do not inflict damage to the unit. As the unit is unpacked, inspect it for possible shipping damage. All claims for this type of damage should be filed promptly with the transporter involved. If a claim is filed for damages, save the original packing material. Most packing material may be reuseable if reasonable care is used in unpacking. Unpack the drive as follows:

a. Remove external packing material carefully.

b. Remove the drive from the container.

c. Remove internal packing materials, following instructions provided on the package.

d. Ensure that front access door opens and closes, and that the head-load arm raises when door is opened.

e. Ensure that bezel is secured.

f. Ensure that drive hub manually rotates freely.

g. Ensure that stepper motor/head carriage assembly is not binding at any point, by manually moving carriage back and forth.

2.3 Installation. Due to its small size and light weight, Model 51/52 can be installed or mounted in any convenient location or position. However, the drive must be installed in a location that will prevent the I/O cable from exceeding 10 feet in length. Refer to Figure 1-1 for dimensions and mounting provisions.

2.4 Hardware. The flexible disk drive is a precision device in which certain critical internal alignments must be maintained. Therefore, in keeping with rigid disk requirements, it is important that the mounting hardware does not introduce significant stress on the drive. Any mounting scheme in which the drive is part of the structural integrity of the enclosure is not permitted. Since the disk drive cannot be subjected to significant stress when it is slide mounted, this type of mounting generally satisfies the foregoing requirements. Mounting schemes should allow for adjustable brackets or incorporate resilient members to accommodate tolerances. Mounting schemes involving more than two hard mounting points and a third point should be avoided.

2.5 Dust cover. Since the flexible disk drive is not provided with a dust cover, the design of an enclosure should incorporate a means to prevent direct ingress of loose items, e.g., dust, paper punch waste, etc.

2.6 Cooling. Heat dissipation from a single disk drive is normally 15 watts (40 Btu/Hr). When the drive is mounted so that the components have access to free flow of air, normal convection cooling allows operation over the specified temperature range. When the drive is mounted in a confined environment, air flow may have to be provided to maintain specified air temperatures in the vicinity of the motors, PCB, and the diskette.

2.7 Drive separation. In addition to the cooling requirements specified in Paragraph 2.6., a minimum separation of 25.4 mm (1 inch) between drives is recommended. This is required to avoid electrical interference between the motors on one drive and the magnetic head of another drive. Closer mounting is allowable if a grounded sheet of steel at least 1.52 mm (0.060 inch) thick is interposed between units. However, use of this steel sheet may increase the cooling requirements.

2.8 Input/output cable. The I/O cable is an optional item and is supplied on order. Refer to Table 2-1 for cable connector part number and attachment. The maximum cable length from connector to connector is 10 feet. All inputs and outputs are paired, one line for function, one for ground. Figure 3-11 provides information relative to the connector pin/signal assignments for I/O cable. (MPI P/N 3-06001-001)

2.9 DC power. DC power to the drive is via connector P2/J2, which is located on the non-component side of the PCB near the spindle motor. The drive uses +12V dc and +5V dc. Table 1-2 outlines the voltage and current requirements. The connector is an AMP Mate-N-Lock Part No. 1-480424-0. (MPI P/N 3-06002-001)

2.10 Initial checkout. The following procedure should be used to determine that the Model 51/52 is operational. This procedure assumes that the drive is installed, I/O cable and power are connected, and that the steps in 2.2 have been completed.

a. Apply "Motor On" command and assure that spindle hub rotates in correct direction (clockwise from top of drive).

b. Load the diskette and apply a head-load command to the drive. Check that head-load solenoid actuates and indicator lights on front panel. Select proper device address.

c. Apply stepping and direction commands to the unit. Verify that the actuator steps as commanded.

d. Remove all command signals, turn power off and return diskette to its storage.

SECTION III

3. INTERFACING REQUIREMENTS

3.1 General. Communication between the host system and the Model 51/52 Flexible Disk Drive is established via two connectors. Connector J1 establishes a communication link for all input/output signals. These signals are TTL compatible. Connector J2 provides dc power to the device.

3.2 Input lines. The input control lines have the following electrical specifications:

a. True, Logical Zero = 0V ± 0.4V @ Iin = 48 ma (max).

b. False, Logical One = +2.5 to +5V (open collector @ Iout = 250 μa max).

3.2.1 Line termination. The signal interface used by Model 51/52 is of the "bus" or "daisy-chain" type. Only one 51/52 unit is logically connected to the interface at any given time. All input signals are terminated directly by a 150 ohm or a 220/330 ohm resistor network. In a daisy-chain configuration, only the last device in the daisy chain should have the terminating network; while in a star configuration, every device should be terminated.

3.2.2 Programmable shunt. The main function of this device is to assign the proper address to the drive in a multi-drive configuration. In addition, it also determines when the head-load solenoid should be activated by using either position 1-14 (with Select) or 7-8 (with Motor On). If position 5-10 is left shorted, the drive is essentially always selected, but the activity light will not come on, and the solenoid will not be activated until the drive position is selected. The programmable shunt is AMP P/N 435704-16 (MPI P/N 1-79600-001). For convenience, the programmable shunt could be replaced by a dip switch, AMP P/N 435166-14 (MPI P/N 1-79601-001). (If dip switch is used, maximum height is exceeded by .150.) The seven lines channeled through the shunt are:

	Designator	Pins
a. Head Solenoid w/Select	T1	1-14
b. Drive Select 1	T2	2-13
c. Drive Select 2	T3	3-12
d. Drive Select 3	T4	4-11
e. MUX (Grounded)	T5	5-10
f. Drive Select 4	T6	6-9
g. Head Solenoid w/Motor On	T7	7-8

3.2.3 Drive Select 1 to 4. The Select lines provide a means of selecting and deselecting one of the four disk drives attached to the controller. When the signal logic level is true (low), the disk drive electronics are activated, the head is loaded, and the drive is conditioned to respond to step or read/write commands. When the logic level is false (high), the input control lines and output status lines are disabled. A select line must remain stable in the true (low) state until the execution of a step or read/write command is completed. After the desired device is selected, allow a 35 msec delay before initiating a read (see Figure 3-2).

3.2.4 Motor on. This input is provided to extend the life of the dc spindle motor. The motor should be turned off if no activity is required of the Model 51/52 after 10 revolutions of the diskette. A minimum of 0.5 second is required before performing a read or write after a "Motor On" command is transmitted to the device (see Figures 3-2 and 3-4).

3.2.5 Direction select. The direction of motion of the Read/Write head is defined by the state of this input line. A true (low) level defines direction as "IN" towards center of the disk; a false (high) level defines the direction as "OUT" (see Figure 3-1).

3.2.6 Step. Together with the direction line, a single pulse on this input will move the Read/Write head one cylinder in or out, dependent on the state of the direction line. The motion of the head is initiated on the trailing edge of step pulse. A minimum of 0.2 μs pulse width at a maximum frequency of 200 Hz should be maintained to assure step integrity (see Figure 3-1).

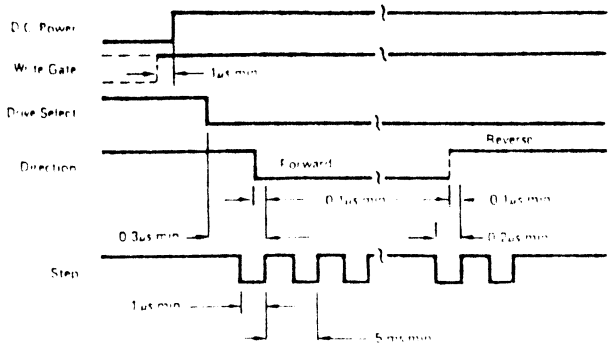


Figure 3-1 Track Access Timing

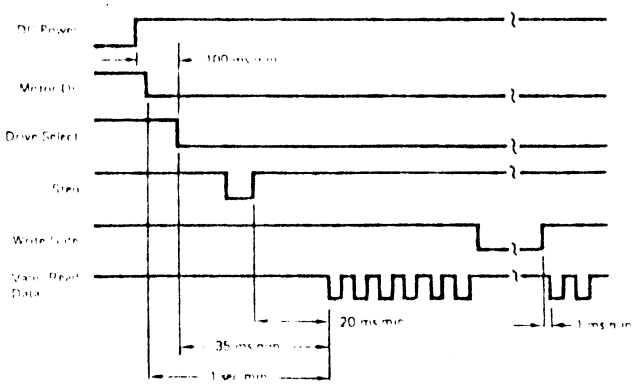


Figure 3-2 Read Initiate Timing

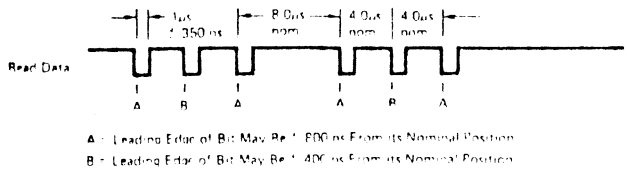


Figure 3-3 Read Signal Timing

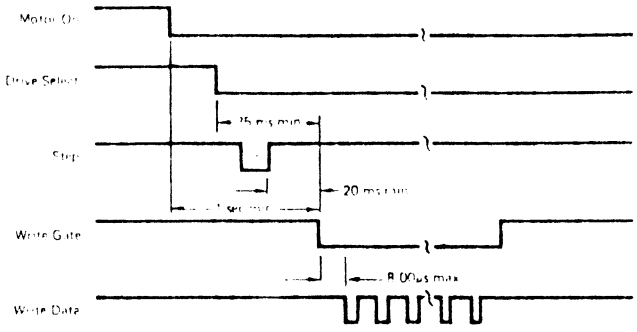


Figure 3-4 Write Initiate Timing

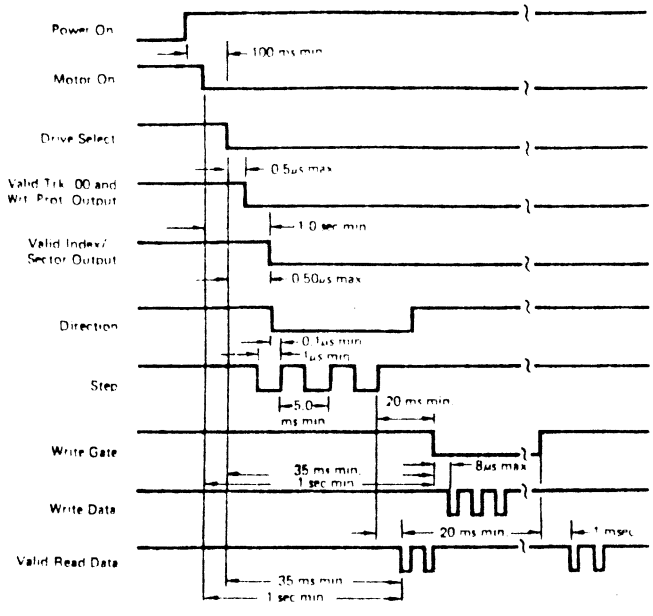


Figure 3-6 General Control and Data Timing Requirements (Head Load Solenoid is Activated with Drive Select)

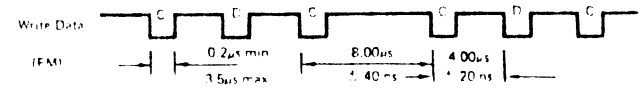


Figure 3-5 Write Data Timing

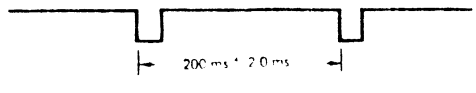


Figure 3-7 Index Sector Timing (soft sector)

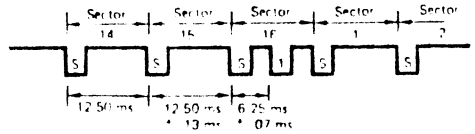


Figure 3-8 Index Sector Timing (hard sector)

3.2.7 Write gate. When true, this input line permits writing of data. When inactive, it permits transmitting data to the controller. Allow a minimum of 1 msec after dropping write gate before expecting valid Read Data (see Figures 3-4 and 3-6).

3.2.8 Write data. This input, in conjunction with the write gate input, provides data to be written on the diskette. The frequency of the write oscillator should be held within 0.1% with a pulse width of a minimum of 0.2 μsec and maximum of 3.5 μsec. The frequency is dependent upon the encoding scheme used and the density option exercised (see Figures 3-4 and 3-5). It is recommended that the first leading edge of Write Data occurs no sooner than 4 μsec and no later than 8 μsec after leading edge of Write Gate. The same recommendation exists for the last Write Data and trailing edge of Write Gate.

3.2.9 Side select. This input is used to select either the upper or lower head. A 35 msec delay should be allowed for the read amp to recover after a head select event occurs. Only then will valid data be present. (For Model 51, this line should always be high.)

3.2.10 In use (optional feature). This line is connected to a driver which could be used for an indicator light, or a solenoid for latching the front door.

3.3 Output lines. The control output signals are driven with an open-collector output stage capable of sinking a maximum of 48 ma at logical zero as true state with maximum voltage of 0.4V measured at the driver. When the line driver is in a logical one or false state, the collector cutoff current is a maximum of 250 μa.

3.3.1 Track 00. This output, when true, indicates that the Read/Write heads are located over Track 00.

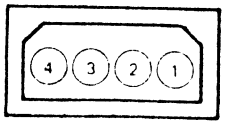
3.3.2 Index/sector. Once every revolution, a pulse is transmitted to the controller indicating the beginning of a track, but only if a single hole diskette is used. If multi-hole media is used in conjunction with the index, sector pulses (10, 16) will also be transmitted to the host system. Leading edge of sector to leading edge of index is 6.25 msec ± .07 msec for 16-sector media (see Figures 3-7 and 3-8).

3.3.3 Write protect. This interface signal is provided by the drive to give the user an indication that a write protected or read-only diskette has been installed. This output is false when the diskette is not write protected. This line may easily be used as a Disk Installed Indicator, if only write protected disks are used.

3.3.4 Read data. This output represents digitized data as detected by the drive electronics. Information transmitted will be in the encoding scheme used. Pulse width of both clock and data bits will be 1 μsec ± 350 nsec. Maximum bit shift for a clock is ± 800 nsec while that for data is ± 400 nsec from their nominal bit positions (see Figure 3-3). The leading edge of each Read Data pulse represents the true position of the flux transition on the recording media.

3.4 Connector J2. The dc power connector is located on the non-component side of the printed circuit board. The recommended mating connector is AMP P/N 1-480424-0 using AMP pins P/N 60619-1.

3.5 Connector J1. Connection to J1 is through a 34-pin PCB edge connector. Even numbered pins are located on the component side while odd numbered pins are located on the solder side. A key slot is provided between pins 4 and 6. The recommended connector is 3M Scotchflex P/N 3463-001, or AMP P/N 583717-5 using AMP contacts P/N 1-583616-1.



Pin 1 +12V DC
Pin 2 12V Return
Pin 3 5V Return
Pin 4 +5V DC

Figure 3-9 DC Power Connector, J2

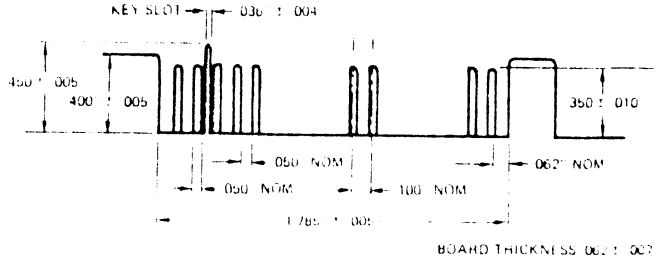
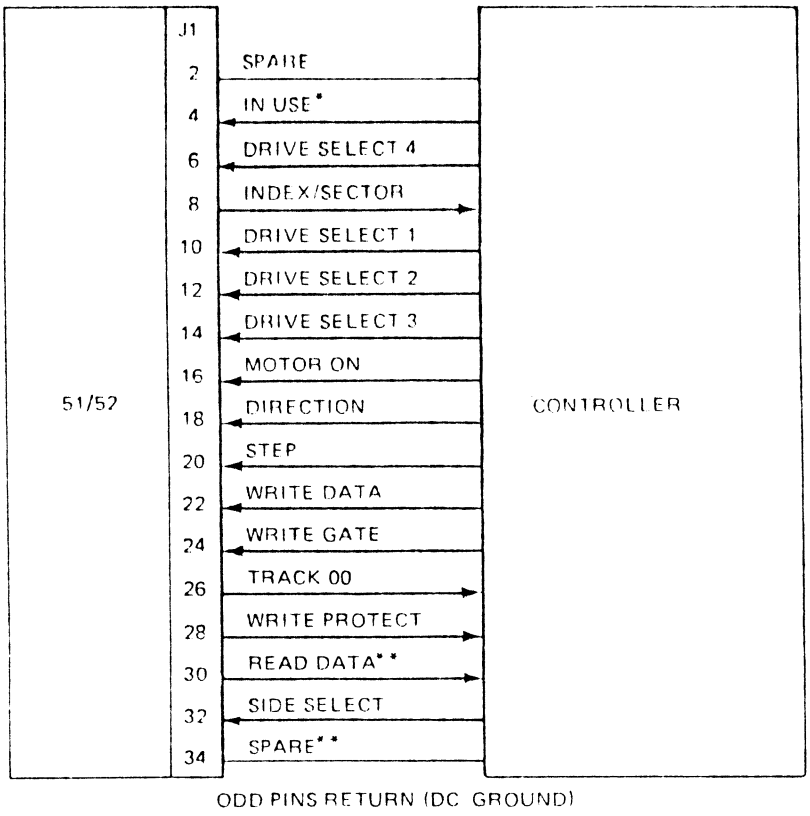
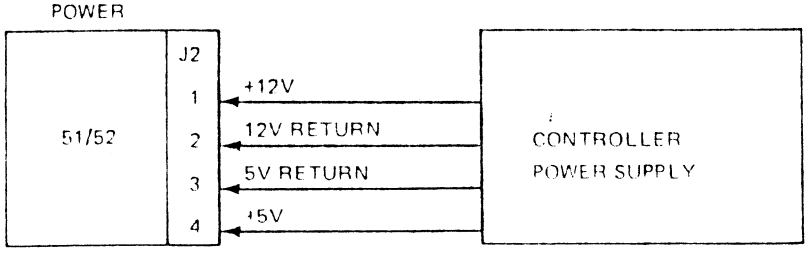


Figure 3-10 J1 Connector Dimensions





* In use may be configured as Door Lock or Activity Light.

** With the optional Data Separator installed, Pin 30 is Separate Clock and Pin 34 is Separate Data.

Figure 3-11 Interface Signals – 51/52

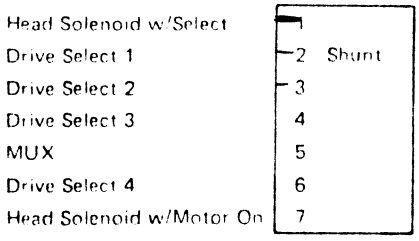


Figure 3-12 Shunt Configuration

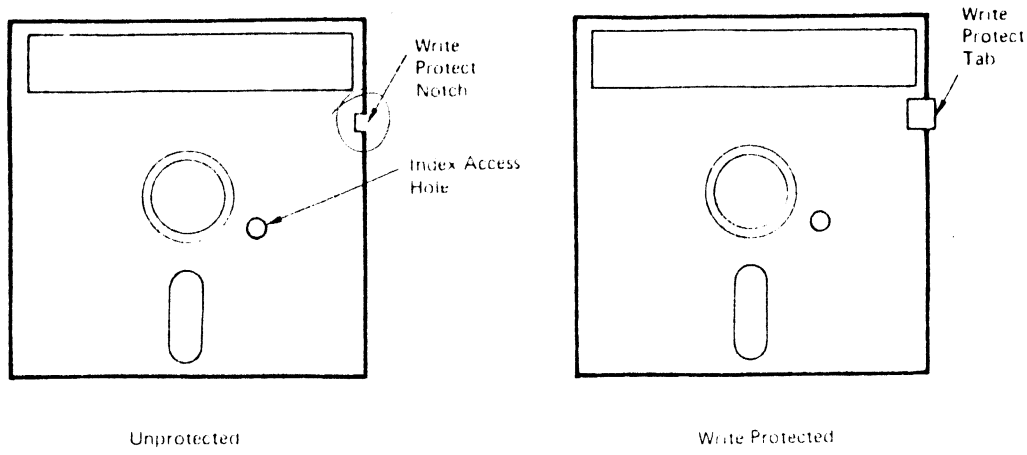


Figure 3-13 Write Protect Option

SECTION IV

4. OPERATION

4.1 General. The Model 51/52 Flexible Disk Drive is under direct control of the interface and power sources. No special start-up procedures are necessary.

4.2 Operating instructions. Secure both power and I/O connectors prior to disk loading.

4.2.1 Flexible diskette loading.

a. Apply dc power to drive.

b. Open drive door by pushing door latch button.

c. Remove diskette from its storage envelope and insert in the drive. The index hole must be on the left side of the jacket and the label on the right towards the door. Push the diskette forward until a "click" is heard. (See Figure 4-1).

d. Close door by pushing door down until latch secures the door.

4.2.2 Flexible diskette removal.

a. Open the drive door by pushing door latch button. The flexible diskette will automatically be ejected to a position where it can be easily removed.

b. Always store the diskette in its storage envelope in order to maintain the highest data integrity.

c. Close drive door.

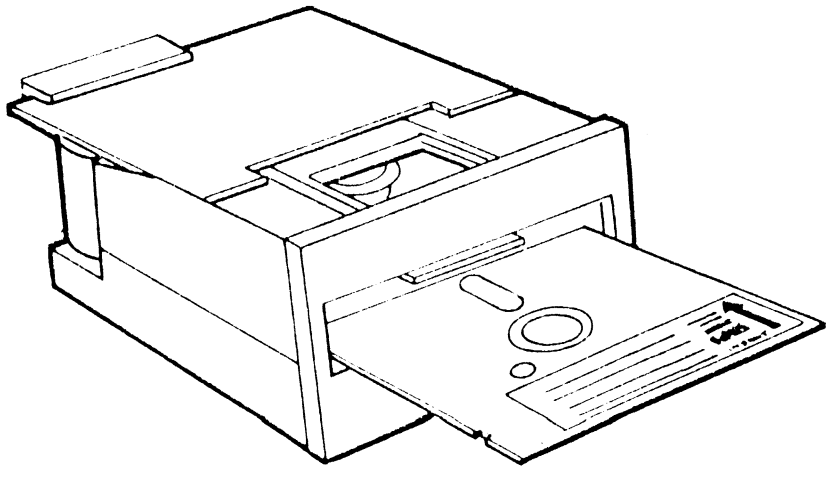


Figure 4-1 Diskette Orientation

4.3 Diskette handling recommendations. Since the recorded diskette contains vital information, reasonable care should be exercised in its handling. Longer diskette life and trouble-free operation will result if the following recommendations are followed:

a. Do not use a writing device which deposits flakes (i.e., lead or grease pencils) when writing on a diskette jacket label.

b. Do not fasten paper clips to diskette jacket edges.

c. Do not touch diskette surface exposed by jacket slot.

d. Do not clean diskette in any manner.

e. Keep diskette away from magnetic field and from ferro-magnetic materials that may be magnetized.

f. Return diskette to envelope when removed from drive.

g. Protect diskette from liquids, dust and metallic substances at all times.

h. Do not exceed the following storage environmental conditions:

Temperature:	50°F to 125°F (10°C to 51°C)
Relative Humidity:	8 to 80%
Maximum Wet Bulb:	85°F (29.4°C)

i. Diskette should be stored when not in use.

SECTION V

5. THEORY OF OPERATION

5.1 General. This section describes the operation of Model 51/52 Flexible Disk Drives. Basic functions of the flexible disk drive are to record and read digital data on a diskette, and to receive and generate control signals necessary for completion of the Read/Write functions.

NOTE:

There is no difference between the PCB for Model 51 (single head) and the PCB for Model 52 (dual head).

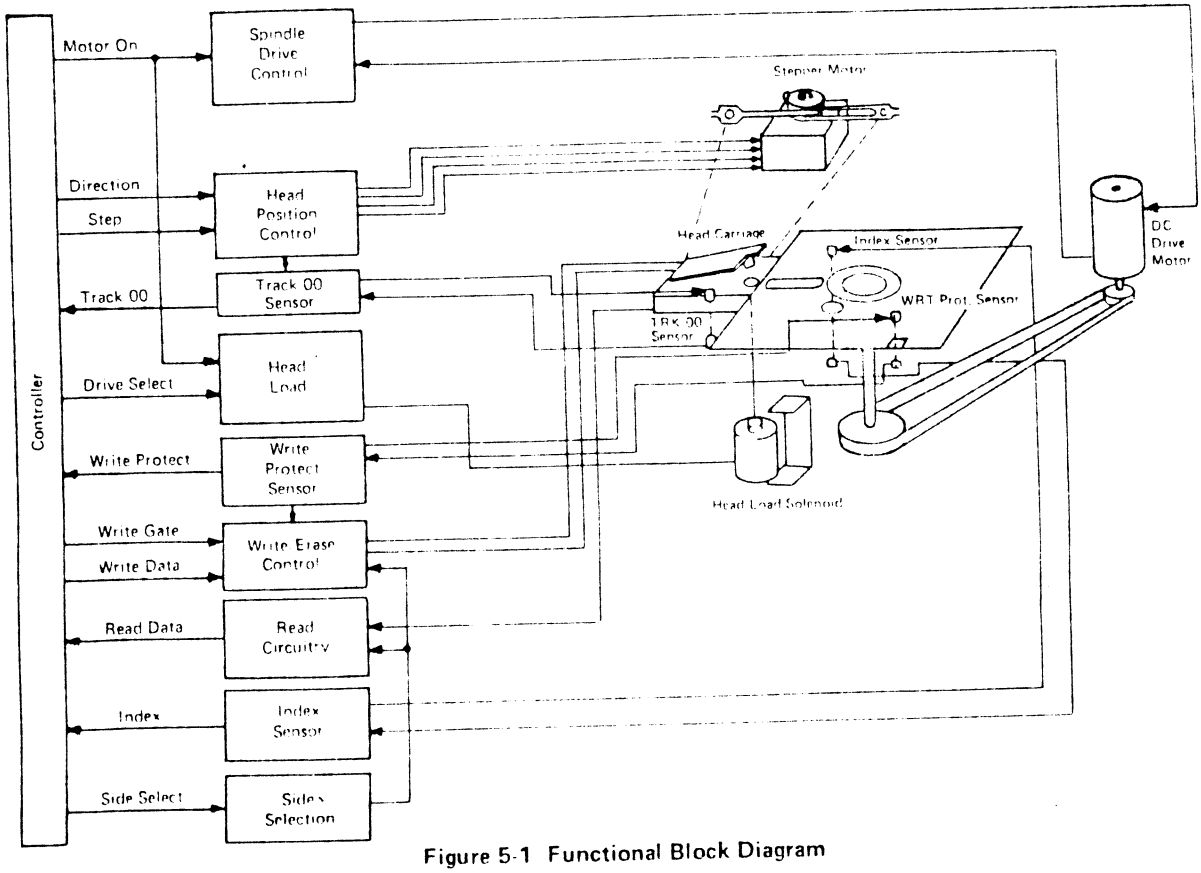


Figure 5-1 Functional Block Diagram

5.2 Mechanical and electrical. Figure 5-1 shows a functional block diagram of the mechanical and electrical groups included in the disk drive, as follows:

a. Spindle drive control.
b. Head load mechanism.
c. Track 00 sensor.
d. Head positioning control.
e. Write Protect sensor.
f. Write/Erase control.
g. Read circuitry.
h. Index sensor.
i. Side selection

Figures 5-2, 5-3 and 5-4 show electrical block diagrams for reference in this section.

5.3 Diskette spindle drive. The spindle is rotated, via a belt, by a dc motor/ac tachometer combination. The electronics for speed control takes timing information from the tachometer (a), compares this with a reference timer (b), and generates a driving voltage for the motor proportional to the difference between (a) and (b). When the Motor On interface line is true, the control circuit allows the motor to come up to speed. The circuit also includes a portion which disables the motor drive in case of no tachometer output for approximately 150 msec (i.e., binding spindle or motor). The diskette is held on the spindle hub by a clamping mechanism which actuates in conjunction with the front door.

5.4 Head load mechanism. The head load mechanism consists of a head solenoid and a head solenoid driver. The interface logic may be connected to energize the solenoid via Direct Select or Motor On (see Section III). Activating the solenoid causes the diskette to be pressed against a fixed platen and a spring-loaded load arm with a felt pad opposite the head, to press the media against the head. This load arm is lifted when the front access door is opened regardless of the state of the solenoid.

5.5 Track 00. The Track 00 sensor consists of a photo detector with the shutter on the head carriage, and circuits for converting to proper I/O levels. In conjunction with head-positioning logic, the sensor generates a low true level on the Track 00 interface line when the head is positioned at Track 00. This also inhibits the stepper-motor circuitry from responding to any "Step Out" command.

5.6 Head positioning control. This consists of a four-phase stepper-motor/pulley-band combination for conversion of rotational to linear motion. The band is attached to the head carriage and control logic necessary for proper motion response according to user commands. The stepper motor operates in a two-phase On Mode. One step on the motor equals a one track linear motion of the head. Thus, high accuracy and high step rates are achieved by the 51/52 series. The correct phases on for Track 00 is 4 & 1. To move the head toward the center of the diskette, with Direction line high, the correct phase sequence is:

TRACK 00	PHASE 4 & 1
TRACK 01	PHASE 1 & 2
TRACK 02	PHASE 2 & 3
TRACK 03	PHASE 3 & 4
TRACK 04	PHASE 4 & 1

5.7 Write protect sensor. This is a set of photo sensors positioned on opposite sides of the Write Protect notch in the diskette. If light from the LED is allowed to hit the photo-transistor, a false level on the interface line will be produced. If a Write Protected diskette is installed, the light beam is stopped and the Write Protect line will go true, thus also disabling the current sources for Write/Erase Control.

5.8 Index sensor. This is a set of photo sensors positioned on opposite sides of the index hole in the diskette, using the hole in the media as a shutter. When the lightbeam from the LED passes through the hole and hits the photo transistor, it will turn on and, through a shaping circuit, generate a true level on the Index Interface line. Location of the photo transistor is adjustable.

5.9 Data recording and retrieving. The drive uses a tunnel-erase head. The erase gap follows the Write/Read gap, and erases the edges of the written track to provide a guard band between tracks to allow for positioning tolerances. The electronics consist of a Write Current source, Steering Circuit, Erase driver, Read amplifier, differentiator, cross-over detector, pulse generator, and a Side Select circuit.

5.9.1 Data recording. When recording digital data, current passes through the winding on the Write/Read core and sets up a flux field across the Write/Read gap. This orients the iron-oxide particles on the diskette surface underneath the gap to the same polarity. The direction of the flux field is a function of the polarity of the Write current. Data are written by reversing the current in the head. Each flux reversal represents a data bit. The head in the drive uses a center-tapped Write/

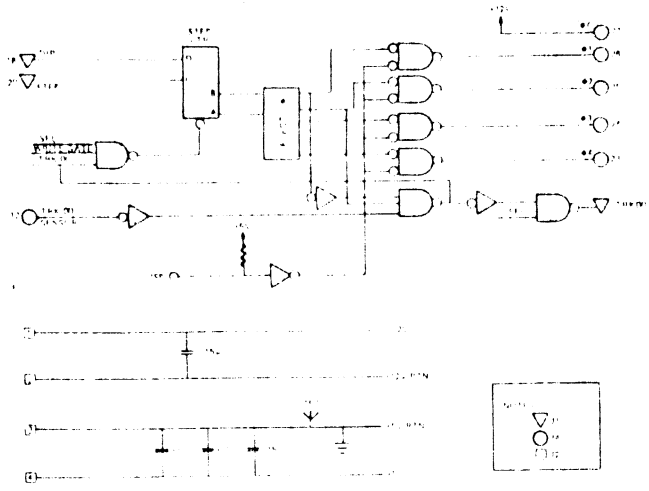


Figure 5-2 Stepper Motor Logic

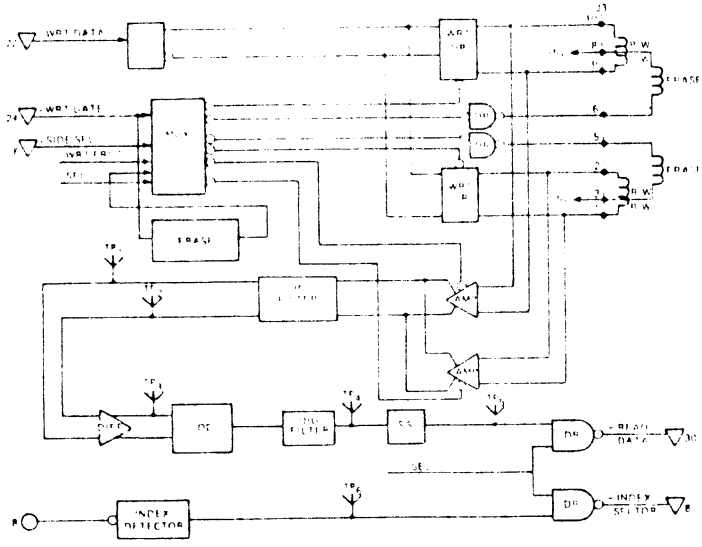


Figure 5-3 Read/Write Logic

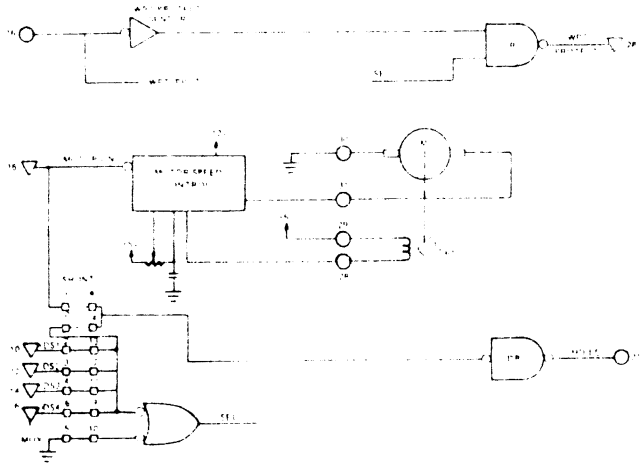


Figure 5-4 Drive Motor Control Logic

Read winding, where the current reversal is accomplished by steering the current through one or the other of the two halves of the winding. Figure 5-5 shows the basic recording technique. The following conditions must be established by the user system before recording can begin:

a. Spindle speed must be stabilized. This condition will exist 0.5 sec after Motor On command is issued.

b. Head/Media must be stabilized subsequent to Head Load command. This requires 35 msec.

c. Head must be settled subsequent to Step command. This requires 20 msec (5 msec for motion, and 15 msec for settling).

The above conditions may be overlapped. It is recommended that the first Write Data command be within 4 to 8 μs after Write Gate goes true, and the last Write Data be within 4 to 8 μs of Write Gate going flase. The Erase Circuit enables the erase current 430 μs after Write Gate goes true, and disables 850 μs after Write Gate goes false. These time relationships are optimized for proper erasure on both inner and outer tracks.

5.9.2 Data retrieving. The Read electronics consists of the following:

a. Read amplifier.

b. Linear filter.

c. Differentiator.

d. Cross-over detector.

e. Digital filter.

f. Pulse shaper.

Several conditions must be established by the user system before Reading can begin. The same conditions applicable to recording must be met. Additionally, if the previous operation was writing, 1 msec must be allowed after termination of Write Gate to allow for erase and circuit-settling time. Figure 5-6 shows wave forms in the Read sequence. The head generates a wave form with peaks corresponding to the flux transients. This is amplified, fed through a low-pass filter, and then differentiated to make the peaks occur at zero cross-over. This signal is next fed to the cross-over detector, which generates a pulse for each cross-over. These pulses are fed through a digital filter, which removes false pulses. Finally, the pulse shaper generates a 1 μs pulse corresponding to each flux transient. This composite Read Data is sent to the user via the Read Data interface line.

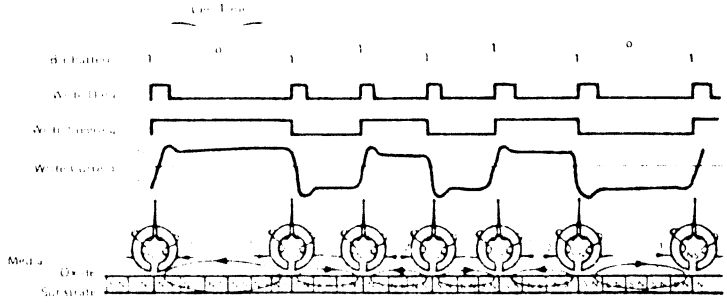


Figure 5-5 Basic Recording Technique

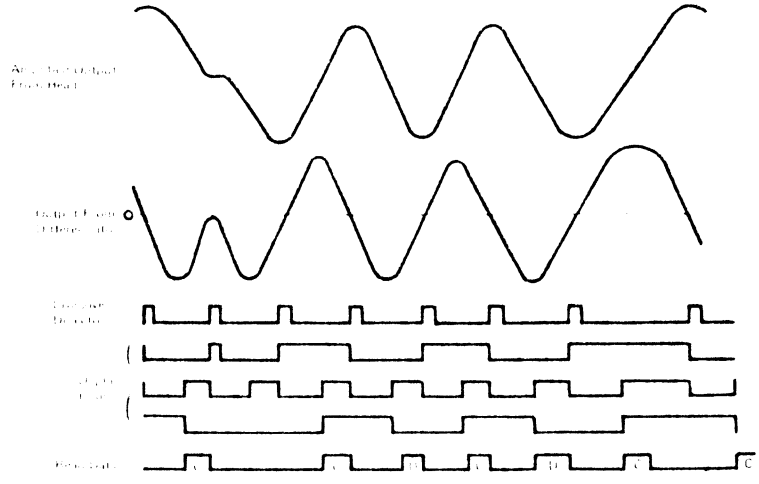


Figure 5-6 Wave Forms in Read Sequence

SECTION VI

6. ERROR RECOVERY

6.1 Seek errors. Unless the stepping rate of 5 msec is exceeded, seek errors rarely occur. However, in the case of a seek error, recalibration of track location is achieved by issuing repetitive Step and Direction Out commands to the drive until the Track 00 status is received.

6.2 Write errors. In order to assure data integrity, a Read after Write should always occur. If the data cannot be recovered on the first Read after Write operation, the Track/Sector should be rewritten and read again. If the data cannot be successfully read within four Write/Read retries, it is recommended that the track be labelled defective, and a different track (sector) assigned. If more than two tracks prove defective, discard the diskette.

6.3 Read errors. If the read after write scheme is followed as described in the previous paragraph, only soft errors are most likely to occur. A soft error is defined as a read error which can be recovered in less than 10 re-tries. However, if the read error cannot be recovered within 10 re-tries, step the carriage one step away from the track in the same direction previously moved and then step back. If the data cannot be recovered, the error is not recoverable.

SECTION VII

7. MAINTENANCE

7.1 General. The only recommended maintenance, which will ensure optimum performance, is periodic cleaning of the Read/Write head(s) and inspection of the load pad. In case repair is necessary, the following paragraphs describe required adjustment procedures:

7.2 Cleaning read/write head. Inspect the load pad (or top head) for excessive oxide, using a dental mirror.

CAUTION

DO NOT MOVE THE UPPER ARM ANY FURTHER THAN IS ALLOWED BY THE DOOR IN ITS OPEN POSITION.

To clean the heads, use a lint-free cloth or cotton swab moistened with 91% Isopropyl alcohol. Wipe the head(s) carefully to remove all accumulated oxide and dirt. Dry the head(s) using a lint-free cloth. (Order MPI Kit P/N 1-86000-001.)

7.3 Adjustment procedures. The following adjustments are required if the parts are being changed due to malfunction. It is recommended, in order to ensure data commonality between drives, that a master alignment diskette be kept, and that each alignment be verified to the master.

7.3.1 Radial-track alignment.

a. Apply necessary power and I/O controls to the drive for recalibration to Track 00.

b. Insert a CE alignment diskette (MPI Part No. 1-42000-001) and close the door.

c. Synch oscilloscope on leading edge on TP6. Connect two probes to TP1-TP2. Set the scope to 50mV/cm, ac coupled, channel A and B added, with B inverted, 200ms/div. Attach ground probes to TP7.

d. Load head and apply 16 stepping pulses, with Direction low. The carriage should be located around Track 16. The proper phase relation of stepper motor should be: phase 4 and phase 1, 0V; phase 2 and 3, +12V.

e. With power on, loosen the setscrew in the stepper pulley and position the pulley so that the cat's-eye appears on the scope with equal amplitude. Secure the pulley with 2 in.-lbs. torque. Command a return to zero and step back out to Track 16 to verify proper alignment.

7.3.2 Index-to-data alignment.

a. Verify radial alignment (see 7.3.1) and then move the head to Track 01.

b. Set oscilloscope to 50 μs/div.

c. The index sensor clamp screws are located at the bottom of the drive. Loosen the screws and slide the sensor such that the scope picture shows a data pattern starting 200 $\pm$ 50 μs from the leading edge of index.

d. Tighten the screws carefully, so no variations in the scope reading occur.

7.3.3 Track 00 sensor alignment.

a. Apply necessary power and I/O control to the drive and load head.

b. Connect oscilloscope to J4-12; set trigger to internal/auto.

c. Loosen the two screws and adjust for the conditions in d. and e.

d. When the carriage is located over Track 00, 01, and 02, J4-12 should be on 0.5 volts (max).

e. Command step-in to Track 03. J4-12 should go high (+4.0 volts min).

f. Tighten the screws.

7.3.4 Speed control.

a. Apply necessary power and I/0 control and load head.

b. Insert diskette and close door.

c. Turn the drive on its side to get access to the strobe mounted on the spindle pulley. Adjust R28 until a stable picture is appearing from the strobe.

7.3.5 Track 00 end stop.

a. Apply power and I/0 control and load head.

b. Command seek to Track 00.

c. Adjust setscrew located on the left-hand boss in the rear of the drive to approximately 0.010 inch from the end of the carriage. Command maximum track seek, then return to zero. Assure that carriage does not hit the end stop.

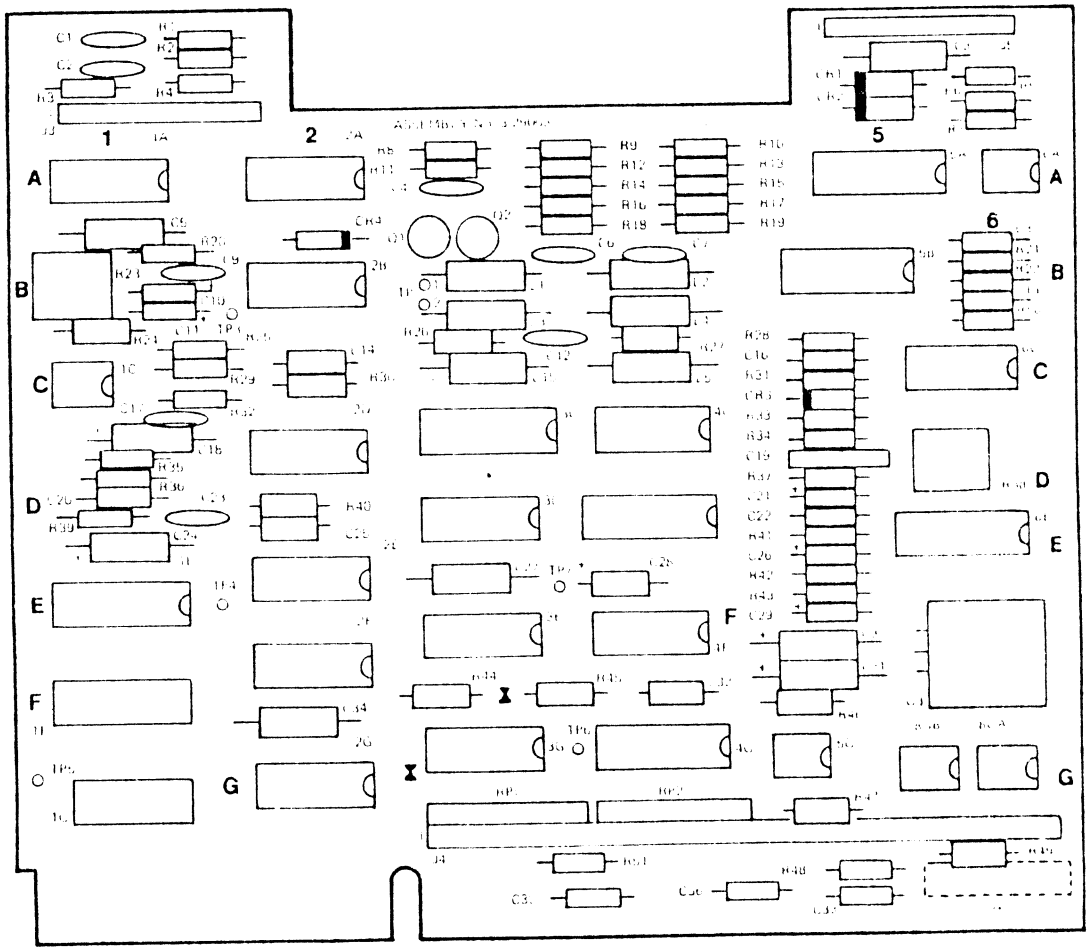


Figure 7-1 Component Location

ERRATA SHEET FOR MODEL 51/52 PRODUCT MANUAL

The following are changes that have been made in the MPI Manual:

1. Page 3, Section II 2.7 Drive separation. Entire paragraph to be deleted.

2. Page 3, Section II 2.8 Input/output cable. First sentence to be deleted. At end of paragraph MPI P/N 3-06001-001 to be deleted.

3. Page 4, Section III,3.2.2 Programmable shunt. Line 6 to be changed to read: by a dip switch, AMP P/N 4-35626-4 (MPI P/N 1-79601-001).

4. Page 4, Section III, 3.2.4 Motor on. Line 2 now to read: no activity is required of the Model 51/52 after 10 revolutions of the diskette. A minimum of 1.0 second is required...

5. Page 6, Section III, 3.2.9 Side select. Line 1 now to read: This input is used to select either the upper or lower head. A 35µ/sec delay should be allowed for the...

6. Page 13,Section VII, 7.2 Cleaning read/write head. Delete line 4, last sentence. (Order MPI Kit P/N 1-86000-001.)

7. Page 13, Section 7.3.1 Radial-track alignment. Line b is now to read; Insert a CE alignment diskette (MPI Part No. 1-01011- 200 double/MPI Part No. 1-01011- 100 single.)

8. Page 14, Section VII, 7.3.4 Speed control. Line c. now to read: Turn the drive on its side to get access to the strobe mounted on the spindle pulley. Adjust R38 until a stable picture is appearing from the strobe.

9. Page 14, Section VII, Diagram. (Change has been made in right G6 area, circut designator 8GB has been changed to 6GB and circut designator 8GA has been changed to 6GA).

See diagram on pg. 2

ERRATA SHEET DIAGRAM

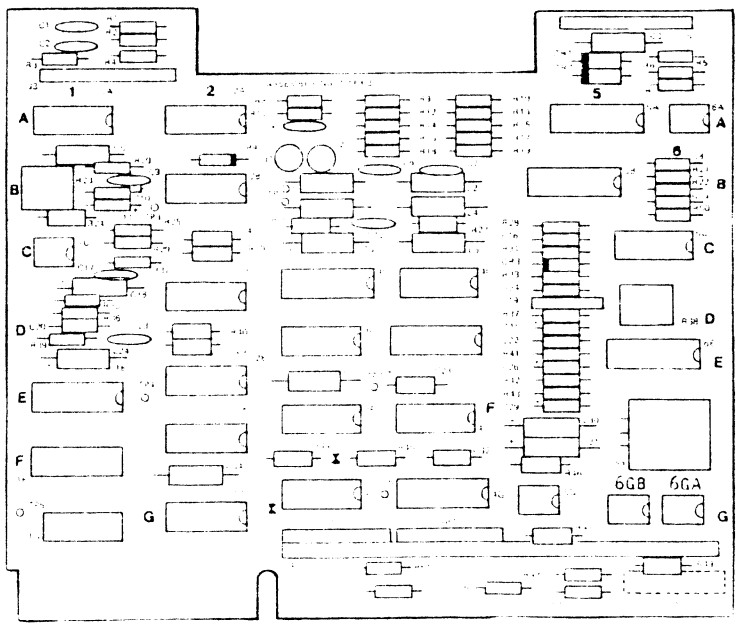
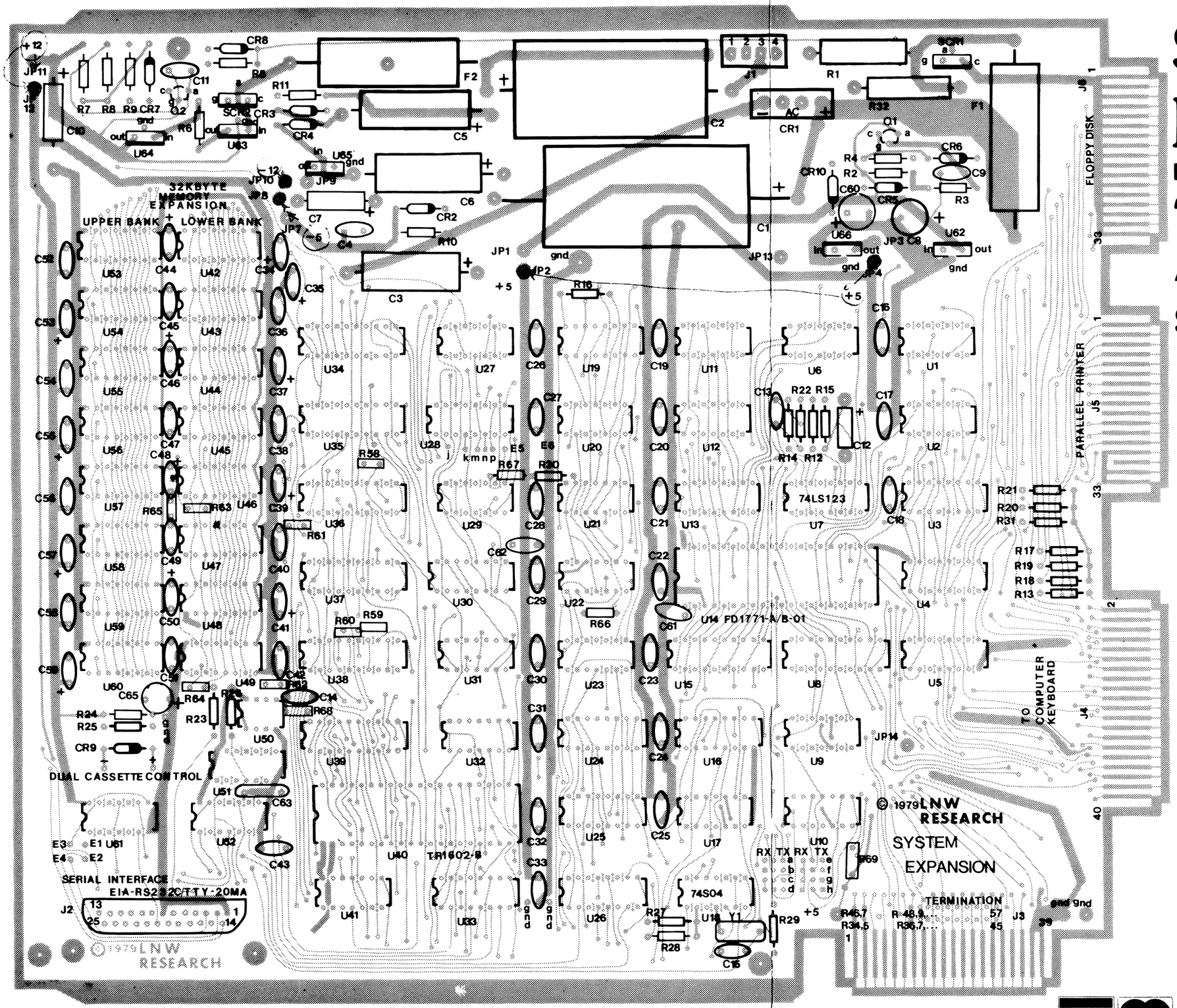


Figure 7.1 Component Location



SYSTEM EXPANSION

FOR THE

TRS-80™

AT

$69.95 [PC BOARD & USER MANUAL]

- SERIAL RS232C/20mA I/O
- FLOPPY CONTROLLER
- 32K BYTES MEMORY
- PARALLEL PRINTER PORT
- DUAL CASSETTE PORT
- REAL-TIME CLOCK
- SCREEN PRINTER BUS
- ONBOARD POWER SUPPLY
- SOFTWARE COMPATIBLE
- SOLDER MASK, SILK SCREEN

LNW RESEARCH

TO ORDER

P.O. Box 16216 Irvine CA 92713
Add $3 for postage and handling.
CA residents add 6% sales tax

VISA master charge

Card No. _____ Expiration Date_____ Signature _____

DOES PERFORMANCE + FEATURES = LOW COST ?

YES! With the 'LNW Research System Expansion', powerful features and high performance do add up to low cost. For '$69.95' the System Expansion Board features 32k BYTE MEMORY EXPANSION, FLOPPY DISK INTERFACE, PARALLEL PRINTER INTERFACE; SERIAL INTERFACE (RS-232-C, 20 mA), DUAL CASSETTE INTERFACE, SCREEN PRINTER BUS AND POWER SUPPLY ON BOARD. And all based on 'no-compromise' engineering and high quality PC design to provide the highest performance possible. Plus, by building the System Expansion yourself you can combine the performance and features of this remarkable board for a fraction of the price of a Radio Shack Expansion Interface.

SERIAL INTERFACE--STANDARD

In order to interface to modems, teletypes, serial printers, and other TRS-80's**, you need a bidirectional Serial Interface. That's why it's standard on the System Expansion. The Interface is implemented with RS-232-C, as well as, 20 mA (TTY) at the standard baud rates. Software compatibility has been maintained and listings of driver programs are supplied.

QUIET MEMORY DESIGN

The 16k dynamic RAM's susceptibility to noise can cause erratic and mystifying behavior. There is no substitue for GOOD PC LAYOUT TECHNIQUES, ADEQUATE SUPPLY BYPASSING AND GROUNDING, and SERIES TERMINATION OF THE ADDRESS AND CONTROL LINES. By adhering to these standards, we created a memory array that requires NO HAND SELECTED MEMORY PARTS, EXHIBITS NO MYSTERIOUS BEHAVIOR, AND CAN BE RELIED ON FOR ACCURATE DATA STORAGE.

ACTIVE TERMINATION

ACTIVE TERMINATION and SCHMITT TRIGGER RECEIVERS are used to provide the utmost in data integrity. Even in an electrically noisy environment and without special buffered cables, the System Expansion Board will operate with "rock-solid" performance.

**TRS-80 is a product of Tandy Corporation.

BUILD WHAT YOU NEED

We know that everyone may not need all the features of our System Expansion Board, and why pay for something you don't need? By offering the bare PC Board and providing PARTS LISTS BY SECTION you can build the board according to your current needs and expand later. This MODULARITY serves to further reduce the cost of your interface.

SUPERB DOCUMENTATION

With every circuit board comes a COMPREHENSIVE USERS MANUAL. This detailed manual features Parts Lists, Assembly Instructions, Testing Sections, Circuit Descriptions, Troubleshooting Information and Schematics.

SOFTWARE COMPATIBLE

Since the System Expansion Board is fully SOFTWARE COMPATIBLE with the TRS-80**, no patches or special software is required.

If you've been searching for the ultimate interface that combined the powerful features and high performance that you need, at a price you can afford, your search is over. The LNW Research System Expansion Board is available today.

Contact your local computer retailer or 'LNW Research'.

LNW RESEARCH

SYSTEM EXPANSION

— SPECIFICATIONS —

I. ELECTRICAL

A. SERIAL INTERFACE

1. EIA RS-232-C or 20mA (TTY)
2. Jumper Selectible Baud rates:
   a. 110, 150, 300, 600, 1200, 2400, 4800, 9600 Baud.
3. Parity:
   a. Even, Odd, or Disable.
4. Word Length:
   a. 5, 6, 7 or 8 bits.
5. Jumper Selectible as Data Terminal Equipment or Data Communication Equipment.

B. MINI FLOPPY CONTROLLER

1. Controls up to four (4) drives.
2. FD1771B-01 Floppy Disk Formatter/ Controller.

C. MEMORY EXPANSION

1. Support 0k, 16k or 32k bytes of expansion.
2. Utilize 16k x 1 dynamic RAM.

D. PARALLEL LINE PRINTER INTERFACE

1. Compatible with the Radio Shack/ Centronic printers.

E. DUAL CASSETTE PORT

1. Relay Controlled.

F. REAL-TIME CLOCK

1. "Heartbeat" interrupt type.

G. POWER SUPPLY

1. Overvoltage protection.
2. Short circuit protection.
3. Thermal shutdown.
4. Four (4) supplies:
   a. +12v @ 300 mA
   b. + 5v @ 1.1 A
   c. - 5v @ 1 mA
   d. -12v @ 20 mA
5. Utilize Radio Shack's UL approved TRS-80** Computer Power Pack.

H. SCREEN PRINTER BUS

1. Extension of the TRS-80** 40-pin Bus.

II. MECHANICAL

A. CONSTRUCTED BOARD SIZE

1. 9.6" x 11.5" x 2"

B. PRINTED CIRCUIT MATERIAL

1. Epoxy with solder mask and silk screened reference.

— ORDERING INFORMATION —

- SYSTEM EXPANSION including printed circuit board and user manual $59.95
- USER MANUAL. . . . . $ 6.95

On all orders, please add $3.00 for postage and handling. California residents add 6% sales tax.

LNW RESEARCH
P.O. BOX 16216
IRVINE, CALIFORNIA 92713

LET	DATE	BY	REV.	REL.

REFERENCE ONLY

SOCKET REAR VIEW

RADIO SHACK POWER PACK

MALE FRONT VIEW

19.1vdc

17vac

115vac

FUSE

J1

F1 2A F.B.

F2 .75 F.B

CR1

C1 15,000 16v

C2 3,300

SCR1

SCR2

R1 3.3 1W 10%

R32 3.3 1W

C66 .1

C67 .1

*HEAT SINK

U66 7805

U62 7805

U63 7805

U64 7812

C60 6.8

C8 6.8

CR10 IN4001

+5v JP3 JP4

+5v JP1 JP2

+12v JP11 JP12

R2 33 1/2w 10%

C9 .1

R3 1K

CR5 6.2v IN5234B

Q1 MPU131

CR6 IN914

R4 8.2 K

R6 10 1/2w 10%

C10 25

R5 1K

CR8 IN914

R7 100 1/2w 10%

C11 .1

CR7 14v IN5244

R8 1K

Q2 MPU131

R9 8.2 K

R10 220 1/2 W 10%

-5v JP7 JP8

C3 220

CR2 IN5231B 5.1v

C4 .1

R11 22 1/2W 10%

C5 220

CR3 IN4001

CR4 IN4001

C6 220

U65 7912

-12v JP9 JP10

C7 25

U16 74LS155

U32 74LS04

U41 74LS30

U23 74LS08

U40 TR1602 B.

U39 74LS244

U33 74LS367

U18 74S04

U50 75452

U26 74LS175

U51 1489

U61 1488

U52 1489

J3 IN OUT

J2

IN E9H

IN E8H

OUT EAH

OUT E8H

IN E8H

OUT EEH

TO U28 PIN 1

THRL DRR RRD SFD

RX BAUD

TX BAUD

D0 D1 D2 D3 D4 D5 D6 D7

CTS

DSR

CD

RI

RS232 SEND (DCE)
RS232 RECIEVE (DTE)

20 ma (Tx-)

20ma (Tx+)

SGND

PGND

RTS

20 ma (Rx-)

DTR

20 ma (Rx+)

RS232 RECEIVE (DCE)
RS232 SEND (DTE)

R23 220

R24 220

R25 47

R26 3.0K

R67 10K

E1 E2 E3 E4 E5 E6

U28 74LS 367

D3 PARITY INHIBIT

D4 STOP BIT SLCT

D5 WORD LENGTH 2

D6 WORD LENGTH 1

D7 EVEN/ODD PARITY

TO U16 PIN 6

SERIAL INTERFACE CONFIGURATION

NOTE: JUMPER AS FOLLOWS

DATA COMM. EQUIP: E3 to E4
E1 to E2

DATA TERMINAL EQUIP: E1 to E4
E2 to E3

JP4 +5v

U1,2,6,11, 21,22,23

U3,4,5,7,13,16, 19,24,25

U9,10,12,17

U8,15

U14

C16-25 .1

JP12 +12v

JP8 -5v

R66 33

C62 .1

C61 .1

JP2 +5

U18,20,27,29 31,32,41,51,52

U26,28,30,33

U42-49, 53-60

U34-39

U40

U50

C35 6.8

C26-33,43 .1

JP12 +12v

C34,59 C37,39,41, 53,55,57 6,8 ufd

C36,38,40 42,52,54, 56,58 .1ufd

JP8 -5v

C44-51 .1 ufd

C65 6.8 ufd

JP10 -12v

C63 .1

JP12 +12

U61

R30 1K

R31 1K

R14 1K

S5

S5-1

S5-4

U18 74S04

U20 74LS14

U32 74LS14

U1 7438

U23 74LS08

U23

U61 1488

U1

U51 1489

U51

U51

SPARES

UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE
BREAK ALL SHARP EDGES .005 MIN	DFTSN	
DIMENSIONS TO BE MET AFTER PLATING	CHK	
ALL SURFACES FINISH TO 125 MAX	ENG APP	
TOLERANCES ON FRAC. ± / X ± / XX ± / XXX ± / ANGLE ±	TOOLING	
MAT'L	INSP	
MAT'L SPEC	SALES	
FINISH	CAT REF	
HEAT TREAT	NEXT ASSY	
	CALC BOOK ____ LAYOUT ____	

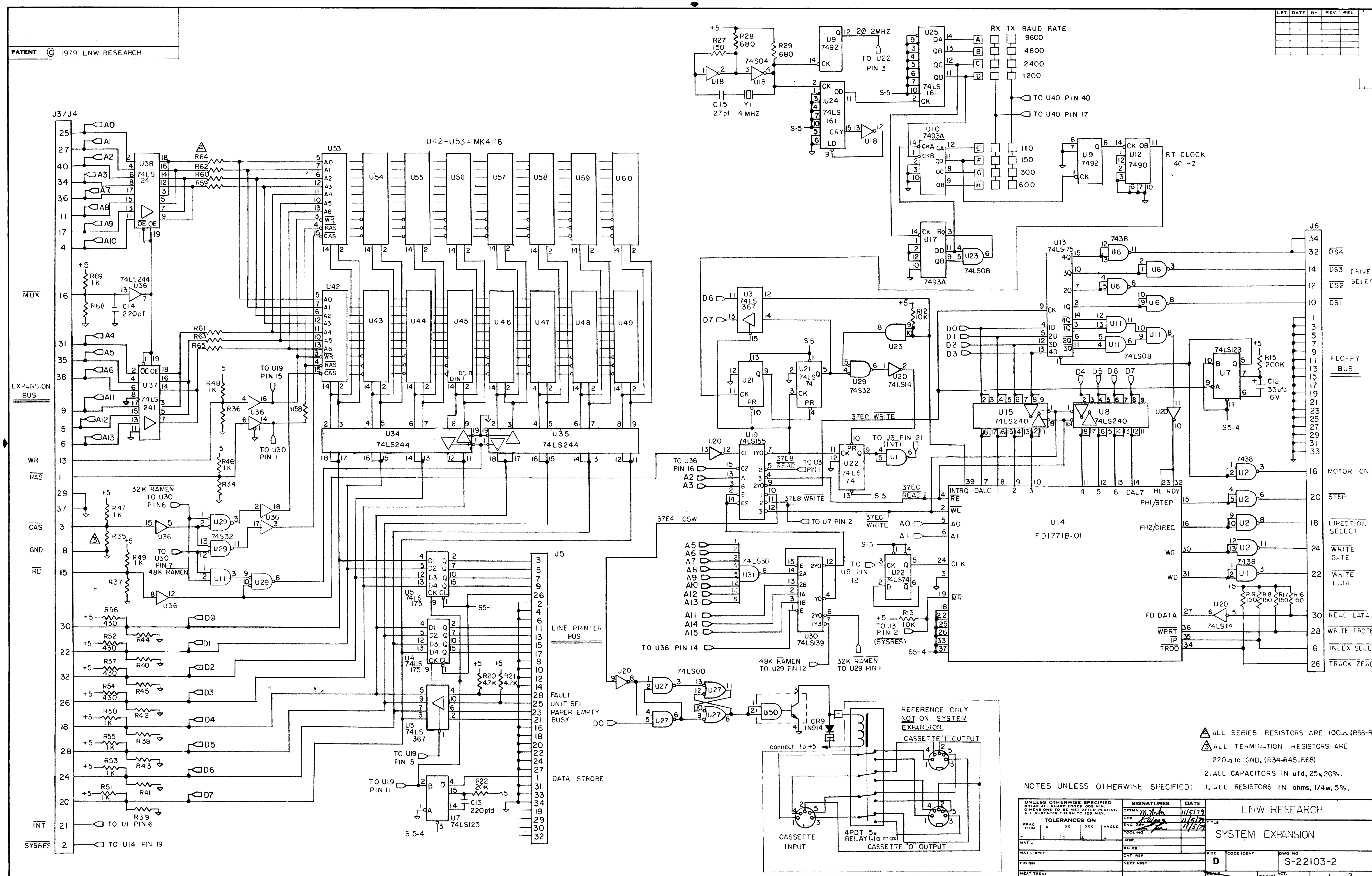
LNW RESEARCH

TITLE: SYSTEM EXPANSION

SIZE D | CODE IDENT. | DWG. NO. S-22103-2

SCALE | WEIGHT ACT CALC | SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-2046


PATENT © 1979 LNW RESEARCH
U42-U53 = MK4116
J3/J4
EXPANSION BUS
J5
LINE PRINTER BUS
FAULT
UNIT SEL
PAPER EMPTY
BUSY
DATA STROBE
RX TX BAUD RATE
9600
4800
2400
1200
110
150
300
600
TO U40 PIN 40
TO U40 PIN 17
RT CLOCK 40 HZ
J6
DRIVE SELECT
FLOPPY BUS
MOTOR ON
STEP
DIRECTION SELECT
WRITE GATE
WRITE DATA
READ DATA
WRITE PROTECT
INDEX SELECT
TRACK ZERO
U14
FD1771B-01
REFERENCE ONLY
NOT ON SYSTEM EXPANSION.
CASSETTE "1" OUTPUT
CASSETTE INPUT
4PDT 5v RELAY (1a max)
CASSETTE "0" OUTPUT
NOTES UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS IN ohms, 1/4w, 5%.
2. ALL CAPACITORS IN ufd, 25v, 20%.
3 ALL TERMINATION RESISTORS ARE 220Ω to GND, (R34-R45, R68)
4 ALL SERIES RESISTORS ARE 100Ω (R58-R65)
LNW RESEARCH
SYSTEM EXPANSION
SIZE D
DWG. NO. S-22103-2
SHEET 1 OF 2
BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-2046