3.1 Power Supply

3.1.1 Power Block

The power supply consists a fuse, zener diode for protection from overvoltage, rechargeable batteries, charging circuit, voltage detector circuit, RS-232C voltage circuit, and LCD voltage circuit as shown in the block diagram below.

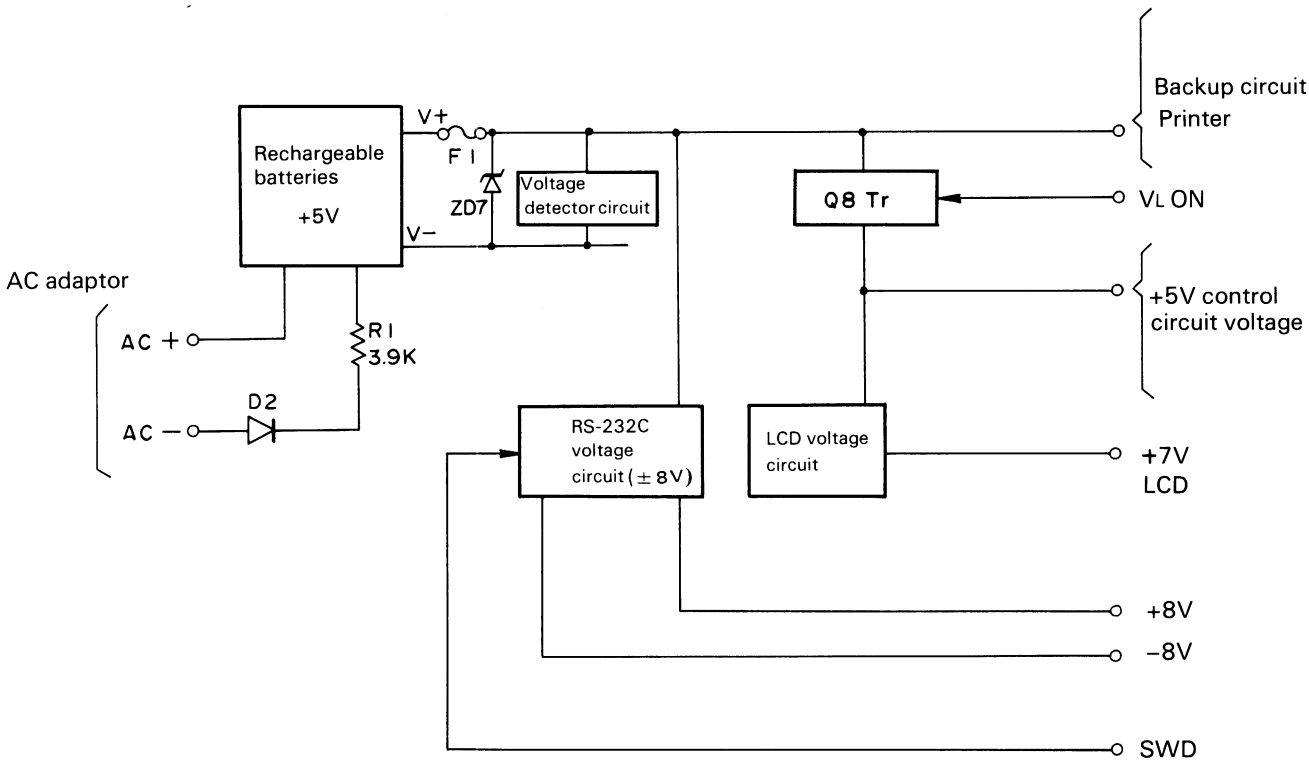


Fig. 3-1

(1) Fuse/zener diode: For protection from overcurrent and overvoltage.

(2) Rechargeable batteries: +5V batteries with capacity of approximately 1100 mAH.

(3) Voltage detector circuit: If the voltage drops below +4.5V, this circuit sends a $\overline{\text{POWER ABNORMAL}}$ signal to notify of its detection of battery voltage drop below the required level.

(4) RS-232C voltage circuit: This circuit generates ± 8V from the +5V.

(5) LCD voltage circuit: This circuit generates a voltage of approximately +7V for LCD from the +5V.

3.1.2 Backup Circuit

The backup circuit constantly supplies a drive voltage to the ICs that are used for protecting the data stored in the RAMs and keeping the power on circuit and reset circuit in operating condition regardless of whether power is on or off.

The elements that are backed up by the batteries are as follows:

LOCATION	IC TYPE	USAGE
4F	TC40H002	Reset and enable
5D	TC40H000	RAM R/W and CE
5E	TC40H004	Interruption circuit
5F	TC4011UBP	Clock and reset circuit
13C ~ 16C	HM6117	2K RAM x 4
12G ~ 15G	HM6117	2K RAM x 4
16D	TC40H138	2 CE outputs for RAM
6G	146818	Real Time Clock

(1) Backup bias

- The battery voltage V_B is applied to the collector of an NPN transistor Q10. It is also applied to the base of Q10 via R77 (470 kiloohms). Because a voltage difference occurs between the base and collector of Q10, the transistor turns on. Thus, the backup voltage of approximately +3V is supplied to the RAMs and some of the elements at all times.
  The reset switch is connected to the base of transistor Q10 and to the batteries via resistor R26 so that, when the reset switch is pressed, the backup voltage is forcibly output.
- If power is turned on normally, transistor Q7 is turned on by a $\overline{V_L ON}$ signal to output a voltage of approximately +5V so the backup from transistor Q10 is ignored and the +5V drive voltage is supplied.

3.1.3 Power Circuit

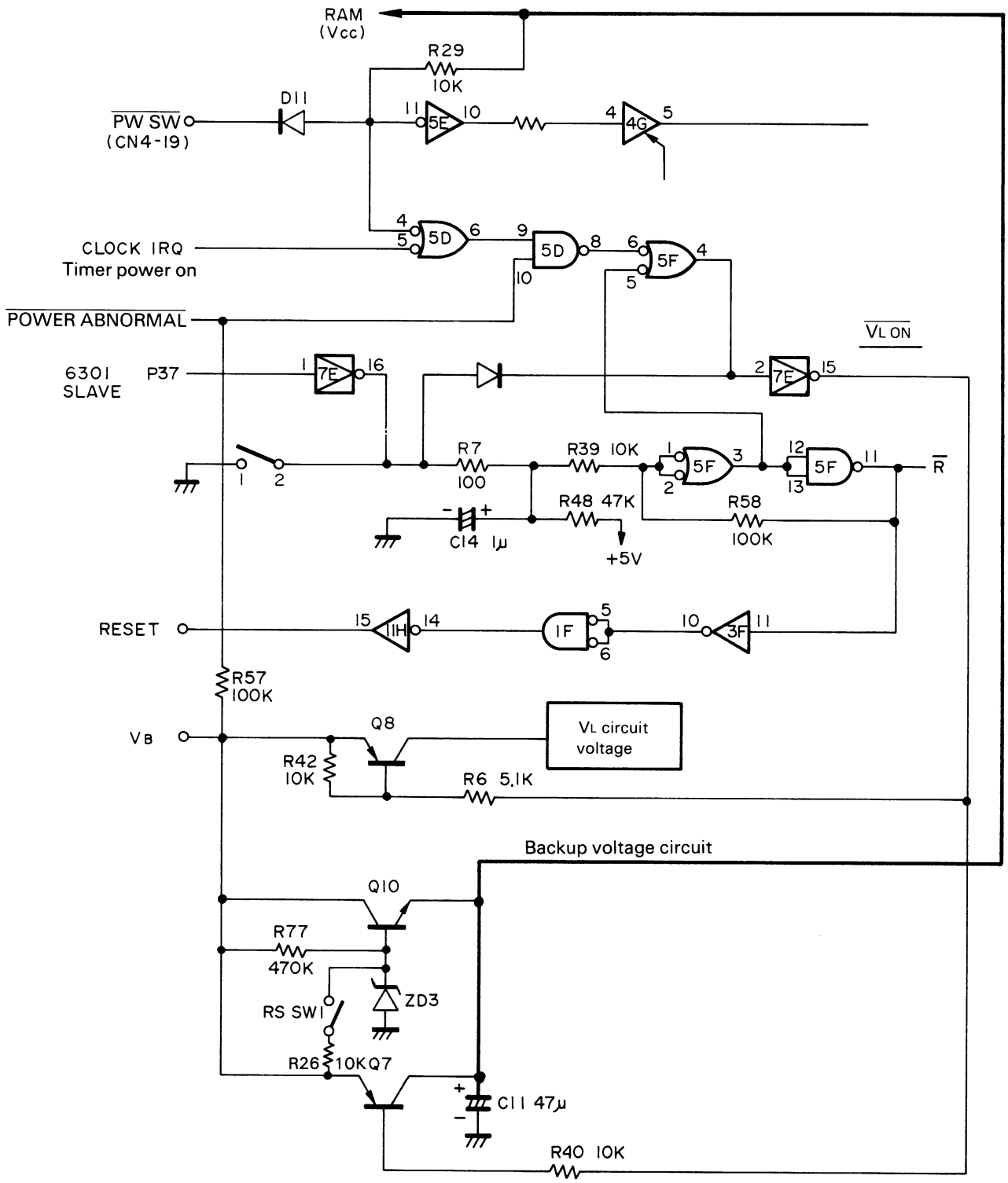


Fig. 3-2

3.1.4 Power On

When the power switch is pushed on, a $\overline{\text{PW SW}}$ (power switch) signal is output from the keyboard to two points, i.e., CN4-19 and CN5-18.

- The $\overline{\text{PW SW}}$ signal which is applied to CN5-18 turns transistor Q1 in the power supply to supply a voltage Vcc to IC 2B to operate the voltage detector circuit. This operation is for checking the battery voltage.
  The $\overline{\text{PW SW}}$ signal that is output to CN4-19 is routed via a diode D11 to Pin 4 of IC 5D so that Pin 6 goes high.
  If no $\overline{\text{POWER ABNORMAL}}$ signal (low-voltage status) is output by the voltage detector circuit at this time, Pin 8 of IC 5D goes low. As a result, Pin 4 of IC 5F goes high and a signal $\overline{\text{VL ON}}$ is output to Pin 15 of IC 7E.
- The $\overline{\text{VL ON}}$ signal turns on transistor Q8 in the power supply, and supplies the line voltage V_L to its collector so that the voltage Vcc is supplied to each element on the control circuit board to permit operation.
- Once power is turned on, the line voltage is supplied to resistor R48 in the reset circuit so, after reset operation, Pin 3 of IC 5F goes low and a power on signal is applied to Pin 5. Even if the battery voltage drops and a $\overline{\text{POWER ABNORMAL}}$ signal is detected as a result, the $\overline{\text{VL ON}}$ signal will not immediately turn off. Thus, the words CHARGE BATTERY! are displayed on the LCD to warn the battery voltage drop. Power on by the reset circuit is sustained as long as the line voltage V_L is supplied. So, when turning power off, it is necessary to have Pin 2 of IC 7E go low.
- Of the $\overline{\text{PW SW}}$ signals output by CN4-19, the one which is routed via IC 5E is used for power switch off interruption to the main CPU.

3.1.5 Reset Circuit

The reset circuit prevents the circuit elements (including the main CPU) from uncontrolled operation when power is turned on, and initializes the individual elements while the reset circuit is operating.

- The reset circuit makes in the following cases only.
  1) Power switch on: A reset signal is output for about 30 msec after the power switch is pushed on.
  2) Reset switch: As long as the reset switch is being depressed and about 30 msec after releasing the reset switch.
- Power on reset
  When the circuit voltage V_L is supplied by the power switch signal $\overline{\text{PW SW}}$, ICs 3F, 1F and 11H in the reset circuit become ready to operate, and all the ICs of the reset circuit, including IC 5F which is backed up, are ready for operation. As the line voltage V_L is also applied to resistor R48, a charging current flows to capacitor C14 via R48 after power is turned on, and the positive potential of C14 is gradually raised as shown in the Fig. 3-3.

The delay time till the positive potential of C14 exceeds the threshold level of IC 5F is used as a reset signal.

- Reset switch

  If the reset switch is pressed, the positive side of C14 is forced to ground level. Thus, a reset signal is output as long as the reset switch is being depressed and till C14 begins to be recharged again after the reset switch is released.

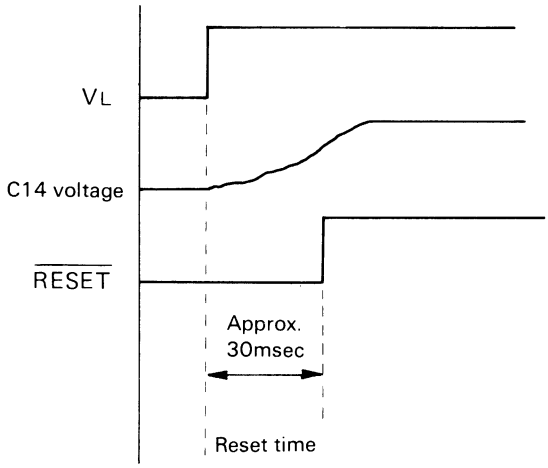


Fig. 3-3

3.1.6 Reset Signal Circuit

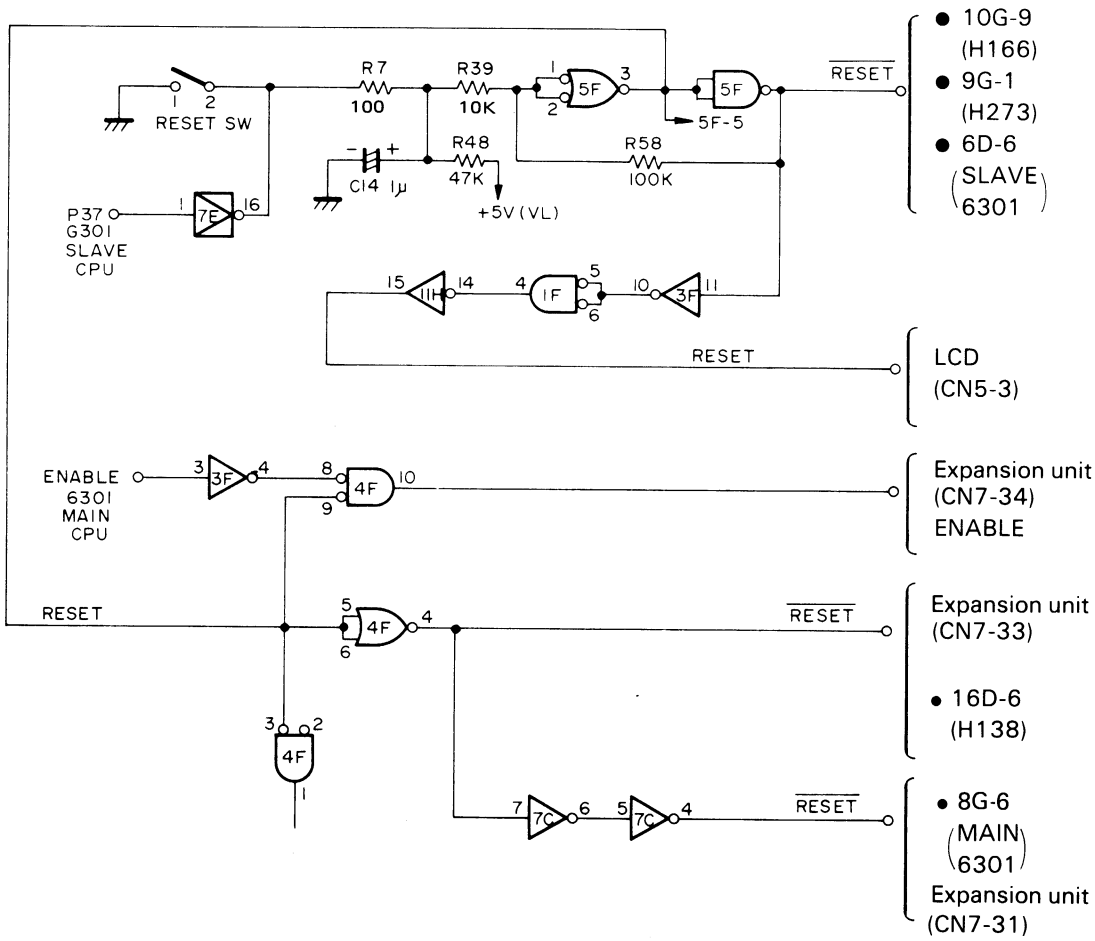


Fig. 3-4

A reset signal is output only when power is turned on or when the reset switch is pressed. The reset signal output to the control circuit board, LCD unit, and extension units initializes the control circuit (and the control program) to prevent erroneous operation.

3.1.7 Voltage Detector Circuit

When the power switch is pushed on, the $\overline{\text{PW SW}}$ signal turns transistor Q1 on to supply the voltage V_B to the Vcc of 2B (MB 3761), making MB 3761 ready for voltage detection.

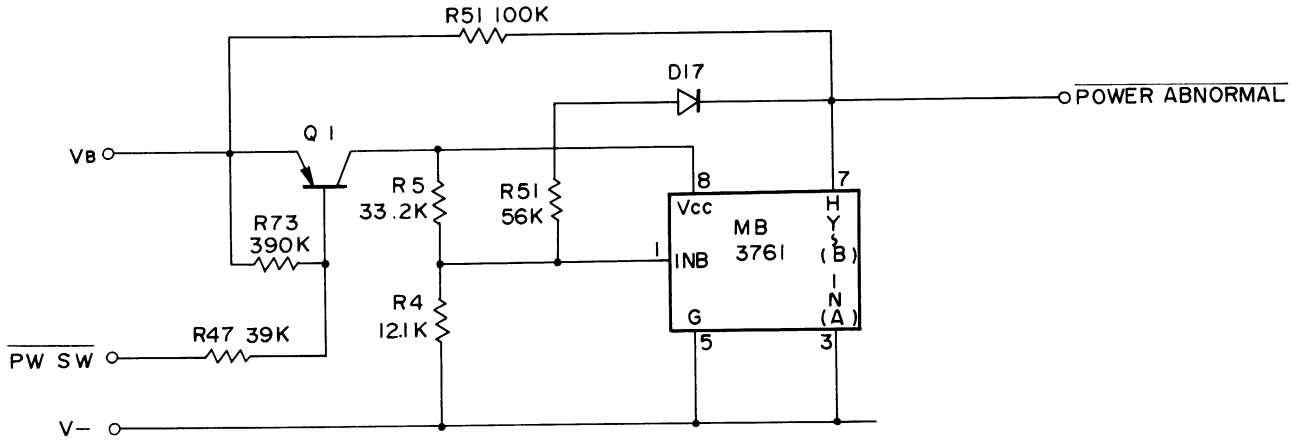
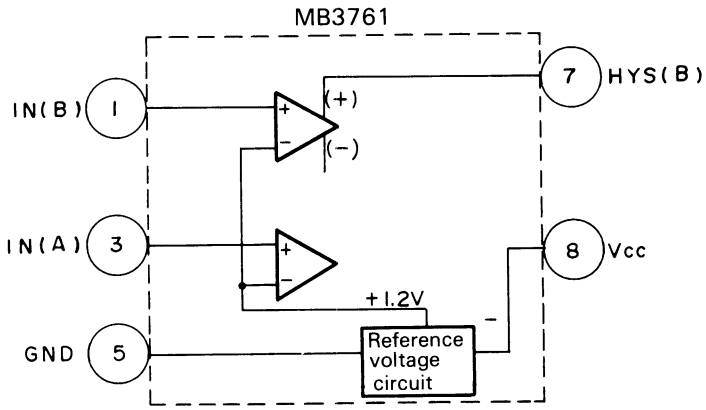


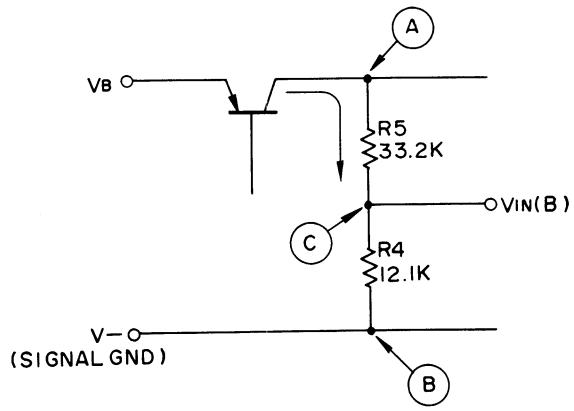
Fig. 3-5



MB 3761 generates a comparison voltage of +1.2V from Vcc with its built-in reference voltage circuit.

Fig. 3-6

When the voltage Vcc is supplied to MB 3761, the comparator is ready to operate, and the reference voltage (+1.2V for comparison) is generated. The voltage V_B supplied from transistor Q1 is routed via resistors R5 and R4 to V- (signal ground). This voltage dividing circuit generates a comparison voltage for feedback.



1. Total resistance (Ⓐ – Ⓑ)

   R5 R4

   33.2 K + 12.1 K = 45.3 (KΩ)

2. Comparison voltage $V_{IN\,(B)}$ (Point Ⓒ)

$$V_{IN\,(B)} \fallingdotseq \left(\frac{Vx}{VR5 + R4}\right) \times R4$$

$$\fallingdotseq \left(\frac{Vx\,(V)}{45.3\,(K\Omega)}\right) \times 12.1\,(K\Omega)$$

Fig. 3-7

The comparator MB 3761 compares the input voltage $V_{IN\ (B)}$ with the reference voltage +1.2V, and outputs the result to Pin 7 (HYS (B)).

Condition	Pin 7 output	Meaning
$V_{IN\ (B)} > +1.2V$	HIGH	Normal voltage
$V_{IN\ (B)} < +1.2V$	LOW	Voltage too low

$V_{IN\ (B)}$ of +1.2V is the limit in abnormal voltage (voltage drop) detection so the bettery voltage in this case can be calculated by the following equation.

$$V_{B\ (X)} = \frac{1.2}{\frac{R4}{R5 + R4}} \qquad \left(V_{B\ (x)} \times \frac{R4}{R5 + R4} = 1.2\ (V)\ REF \right)$$

$$= \frac{45.3 \times 1.2}{12.1}$$

$$= \underline{\underline{4.5\ (V)}}$$

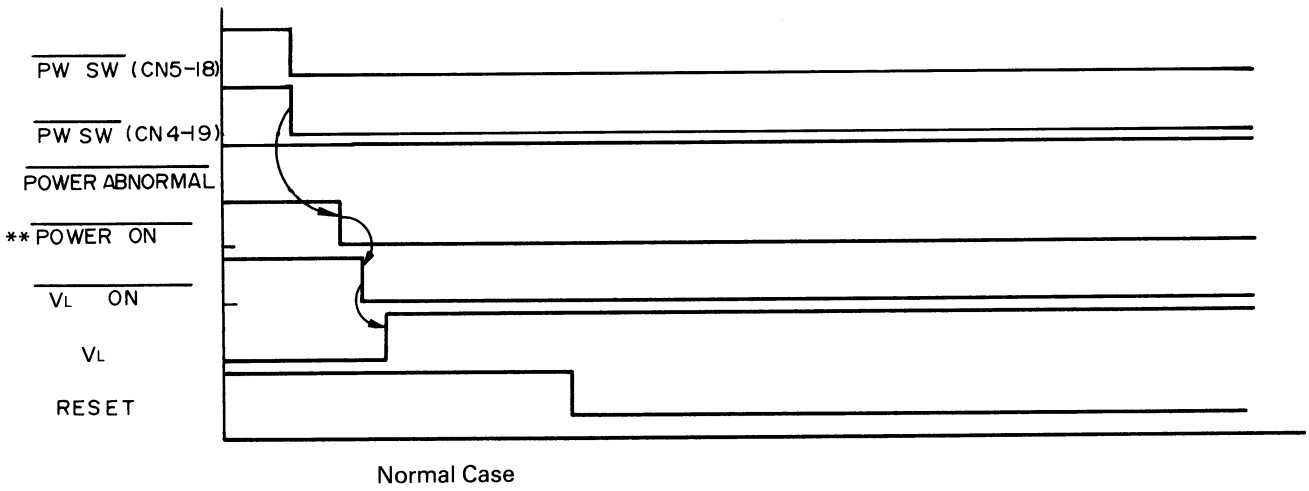
As shown above, +4.5V is the abnormal voltage detecting point.
When the battery voltage falls below +4.5V, the Pin 7 output of the comparator MB 3716 goes low ($\overline{\text{POWER ABNORMAL}}$), and this signal is sent to IRQ (Interrupt Request) and P14 of the main CPU. Upon detection of interruption by the $\overline{\text{POWER ABNORMAL}}$ signal, the CPU immediately stops operaion, flashes the warning CHARGE BATTERY! on the LCD screen about 60 times, and automatically turns power off.

Note:

The batteries discharge current until the voltage reaches + 4.0V so that, even if an abnormal voltage is detected, the data stored in the RAMs are kept unless some trouble occurs. It is necessary to recharge the batteries as soon as possible if the voltage drops to that level because, if the batteries are kept in that state for a long time, the voltage further drops, resulting in breakdown of the data stored in the RAMs and a shorter battery life.

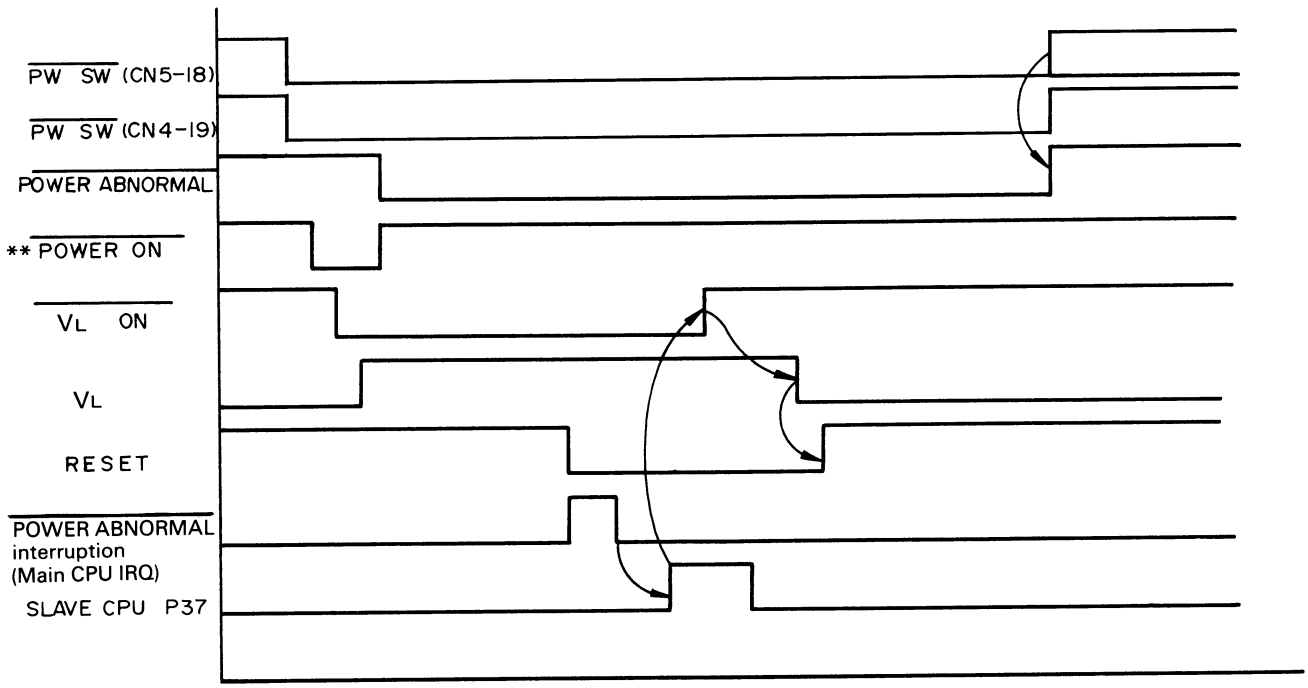
- Overvoltage is not detected, but if an overvoltage (above 6.8V) occurs, zener diode ZD7 is shorted so its protect the circuits.

3.1.8 Power On Timing



Normal Case

Fig. 3-8



Where Low Voltage is detected

Fig. 3-9

*The warning CHARGE BATTERY! flashes 60 times on the LCD screen from the detection of a $\overline{\text{POWER ABNORMAL}}$ signal till $\overline{\text{VL ON}}$ is off.

**$\overline{\text{POWER ON}}$ is output signal of IC5D PIN8.

3.1.9 Power Off

Power can be turned off by any of the following three methods.

1) Push the power switch off: Normal power off.
2) Push the power switch off and then press the reset switch:
   Power off in case of abnormal voltage drop or uncontrolled program execution.
3) Power is automatically turned off by the program after 30 seconds of voltage drop display CHARGE BATTERY!: Power off by program.

(1) Power off with power switch

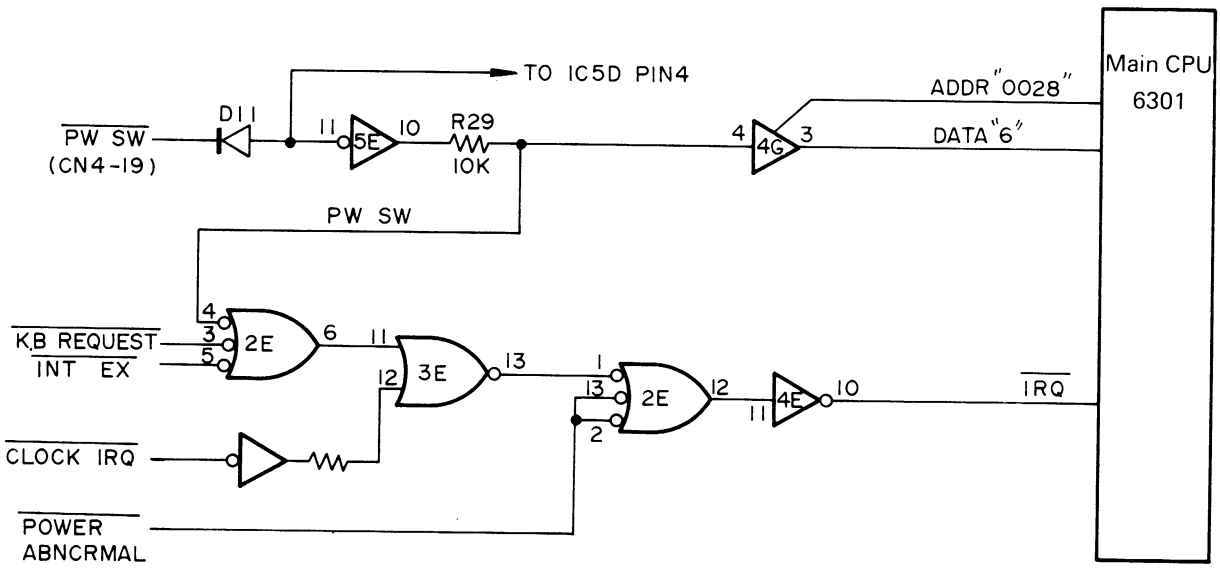


Fig. 3-10

When the power switch is pushed off, a $\overline{\text{PW SW}}$ (CN 5 - 18) signal goes out to turn off transistor Q1 in the power circuit so Vcc is no longer supplied to IC 2B (MB 3761), and the voltage detector circuit becomes ineffective.

A $\overline{\text{PW SW}}$ (CN4-19) signal is applied to Pin 4 of IC 5D so that the output $\overline{\text{POWER ON}}$ signal from Pin 8 of IC5D goes out. But $\overline{\text{VL ON}}$ cannot be turned off because of the reset signal from the reset circuit which is connected to Pin 5 of IC 5F. Therefore, power is turned off by program interruption. This circuit sends a $\overline{\text{PW SW}}$ signal to Pin 4 of IC 2E via IC 5E and R29. When the power switch is pushed off, Pin 4 of IC 2E goes low so that Pin 6 of IC 2E goes high, Pin 13 of IC 3E goes high, Pin 12 of IC 2E goes high, and Pin 10 of IC 3R goes low.

As a result, an $\overline{\text{IRQ}}$ signal (I/O request) is sent to request an interruption to the CPU. When the main CPU accepts the interruption, ports 13, 14 and 15 and I/O address 0028 are checked, and the kind of interruption is identified. In case of an interruption by the power switch ($\overline{\text{PW SW}}$), a 0028 output is sent to an address bus line, and an output is generated from Pin 11 of IC 9E (for I/O select) so the $\overline{\text{PW SW}}$ line signal is read from Pin 5 of IC 4G to data line 6.

Through the process described above, the main CPU confirms that the power switch is off, and gives a power off command to the slave CPU. When the slave CPU receives the power off command, port 37 of the built-in program is set to high level, and Pin 16 of IC 7E to low level.

As a result, Pin 2 of IC 7E goes low via IC 5F of reset circuit, causing Pin 15 to go high and turning the $\overline{V_L ON}$ signal off.

When the $\overline{V_L ON}$ is off, power transistor Q8 turns off to stop supplying the logic voltage V_L. When the logic voltage V_L is no longer supplied, R48 in the reset circuit is not pulled up and the output from Pin 3 of IC 5F goes high. At this point of time, the power on signal to Pin 4 of IC 5F is turned off, thus, completing the power off operation.

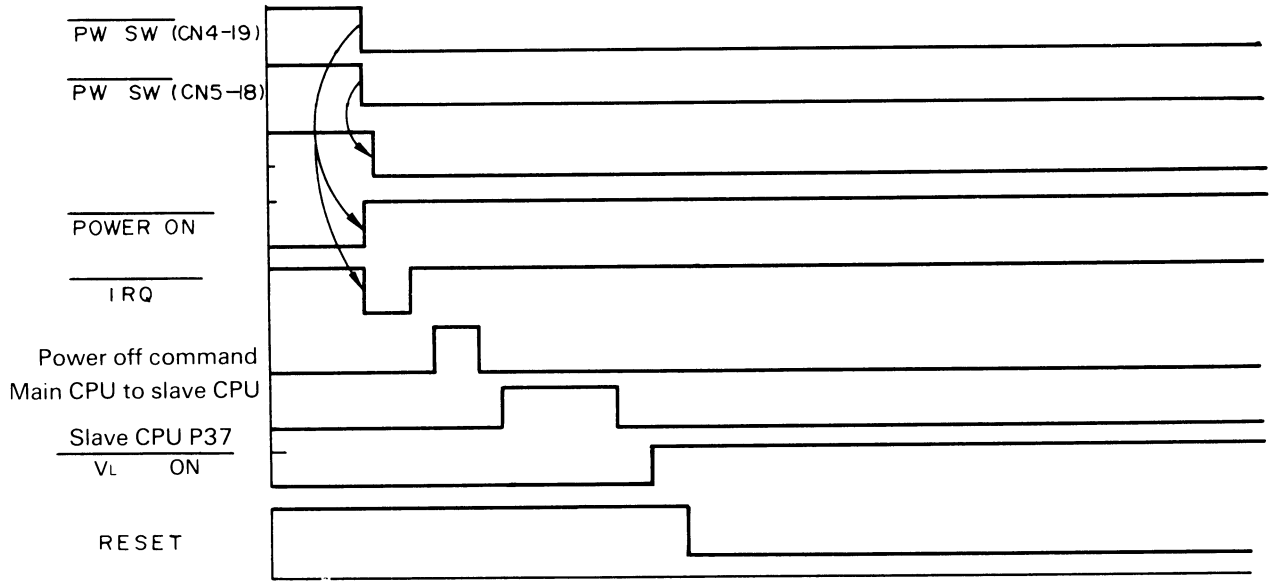


Fig. 3-11

(2) Power off with reset switch

Normally, power can be turned off by pushing the power switch off. In the following cases, however, power cannot be turned off by simply pushing the power switch.

In these cases, push the power switch off and then press the reset switch to turn power off.

- An interrupt request cannot be processed due to uncontrolled run of the main CPU program.
- An element failure has occurred in the $\overline{IRQ}$ signal line, RESET line, $\overline{PW\ SW}$ (CN4-19) signal line, main CPU or slave CPU.

Push the power switch off, and then press the reset switch. PIN5 of IC 5F goes high, so the $\overline{V_L ON}$ signal is turned off and the line voltage V_L is no longer supplied. Thus, power can be cut off. The reset switch is also connected to the voltage backup circuit in the power supply, and when the reset switch is pressed, transistor Q10 turns on compulsorily.

(3) Power off by program

If the voltage detector circuit detects a battery voltage drop below +4.5V, it sends a $\overline{\text{POWER ABNORMAL}}$ signal to the main CPU for program interruption. When the main CPU accepts this interruption, the warning CHARGE BATTERY! is flashed 60 times on the LCD screen, and a power off command is sent to the slave CPU. Port 37 of the slave CPU goes high to turn the $\overline{V_L \text{ ON}}$ signal off and power off. Even if the power switch is in the on position, the voltage detector circuit keeps sending a $\overline{\text{POWER ABNORMAL}}$ signal to hold Pin 10 of IC 5D in the power on circuit at low level, making the $\overline{\text{PW SW}}$ (CN4-19) signal ineffective. This prevents power from turning on again.

It is necessary, nevertheless, to push the power switch off because, unless it is in the off position, the batteries keep supplying the voltage to IC 2B and lose their stored charge.

3.1.10 RS-232C Voltage

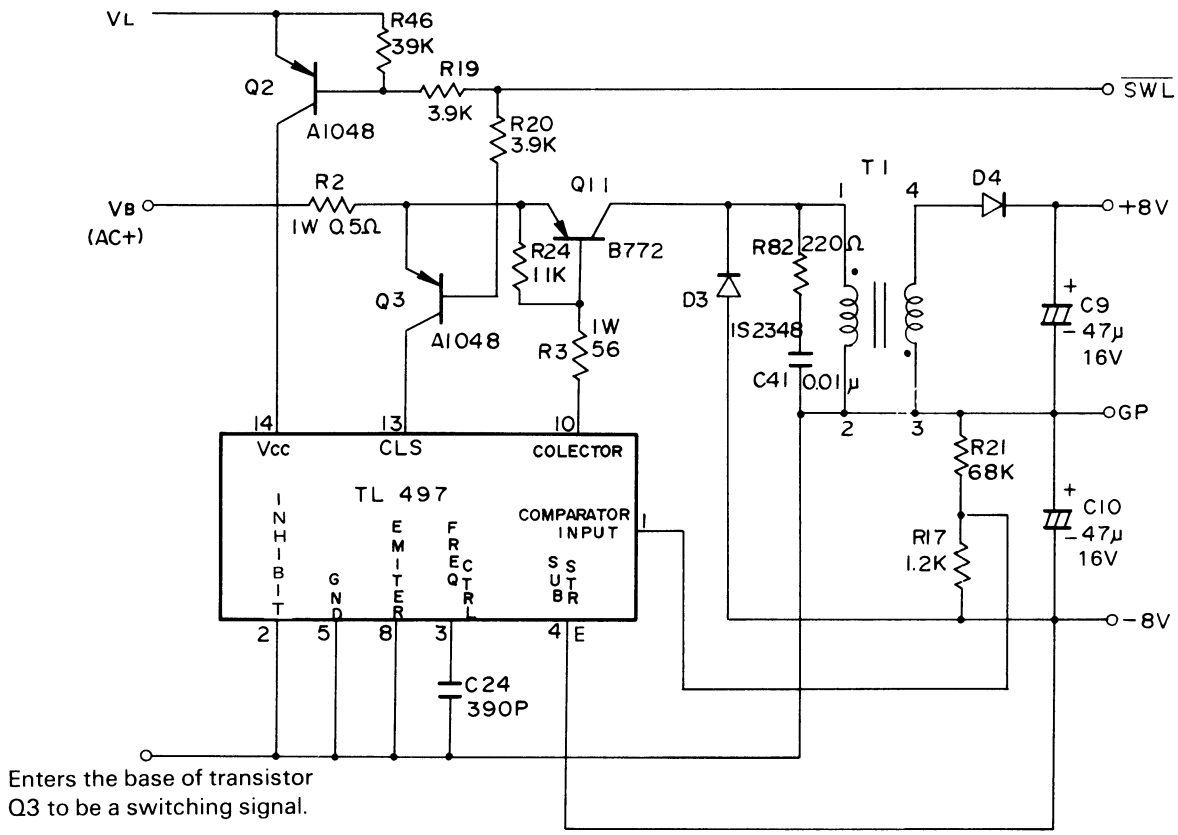


Fig. 3-12

- The built-in batteries keep supplying the DC voltage of 4.5 to 6.0V. The ± 8V is used only in data transfer with the serial interface or RS-232C. To minimize battery consumption, the system is designed to generate the ± 8V only when it is used.
- Voltage output

  If the power switch is on and normal power on reset operation is executed, the line voltage V_L is supplied. If an operation starts in the RS-232C mode (data communication using the output to the external printer or acoustic coupler) under this condition, a $\overline{\text{SWL}}$ signal is sent to turn transistor Q2 on. As a result, the voltage Vcc is supplied to TL 497 to make the switch voltage regulator TL 497 ready to operate. When the Vcc is supplied, a switching pulse with an on-time of about 32 μsec is generated by the external capacitor which is connected to Pin 3.

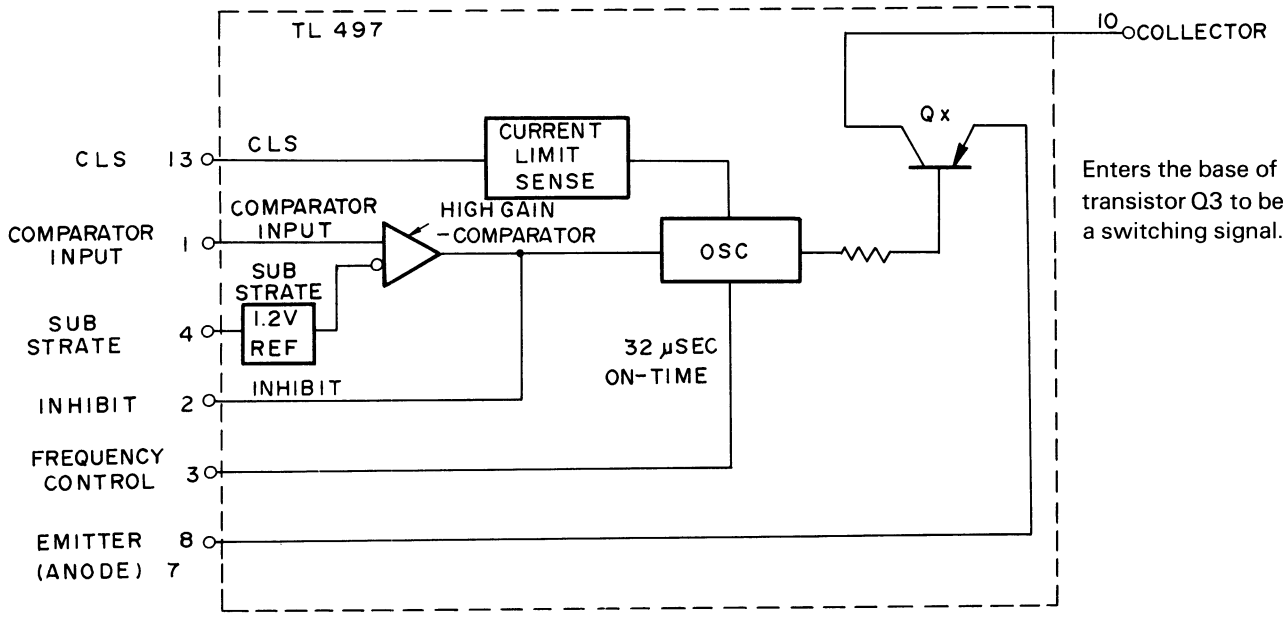


Fig. 3-13

At this point of time, the input to Pin 1 of TL 491 is 0V (because transistor Q1 is not on), the output of the high gain comparator actuates the oscillator circuit to switch the built-in transistor Qx. As a result, Pin 10 outputs a low level pulse to turn on transistor Q11, and supply a V_B pulse to transformer T1.

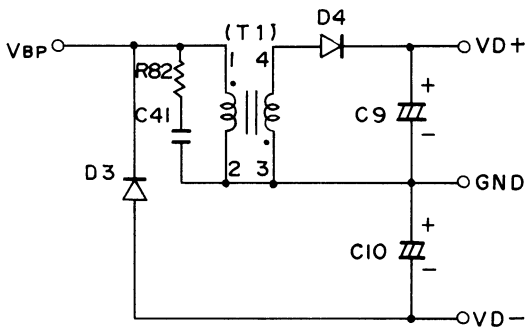


Fig. 3-14

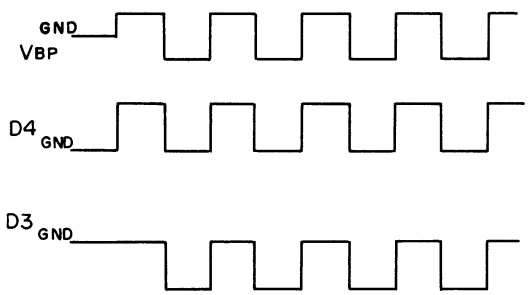


Fig. 3-15

The V_B pulse output to the coils of transformer T1 feeds a current to capacitor or C9 via diode D4 if Pin 4 of T1 is positive. If the primary side of transformer T1 goes negative, a current is fed from the capacitor via chopper diode D3.

Each output is smoothed by capacitors C9 and C10, and +8V and −8V are generated from the output terminal.

These output voltages are fed back to the regulator to stabilize them. The output voltage stabilization by feedback to the regulator is effected by utilizing the potential difference between the signal line that is connected to Pin 1 of TL 497 half way between R21 (6.8 kilohms) and R17 (1.2 kilohms) and the signal line that is connected to Pin 4 of TL 497.

If the VD output is normal (–8V), the potential difference is 1.2 V ($\frac{8}{68+.12} \times 1.2$). If the voltage is lower than normal, the potential difference will be less than 1.2V, causing the oscillator circuit of TL497 to operate to switch transistor Q11. If the voltage is higher than normal, transistor Q11 stops switching. It is in this way that the outputs are fed back to the regulator to maintain the +8V and –V at the rated level.

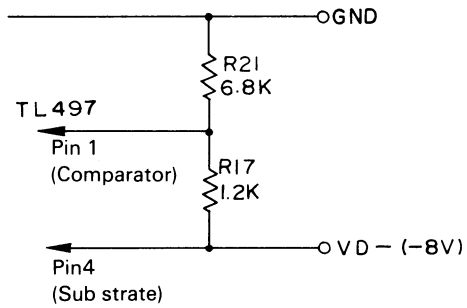


Fig. 3-16

- Overcurrent detector circuit

  This is a protecting circuit against output shortcircuit, etc. Resistor R2 in the circuit that connects V_B to transistor Q11 is an overcurrent detecting resistor. TL 497 has a built-in current limit sense circuit, which stops oscillation operation if it detects a voltage drop of 0.7V, thus stopping the ± 8V outputs.

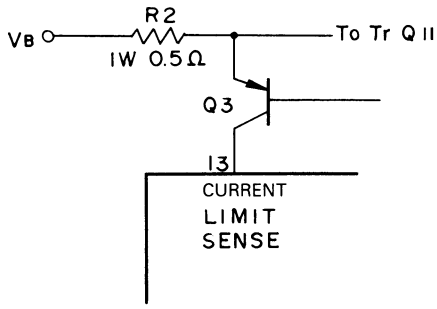


Fig. 3-17

*Overcurrent is 1.2A as calculated by the following equation.

$$\left\{\begin{array}{ll} I_{(A)} = \dfrac{0.7V}{0.5\Omega} & \cdots\cdots \text{CURRENT LIMIT SENSE} \\ & \cdots\cdots \text{Resistor R2} \\ = 1.2(A) & \cdots\cdots \text{Overcurrent} \end{array}\right\}$$

3.1.11 LCD Voltage

A voltage effect type LCD is employed so the voltage required for its control is generated form the battery voltage by DC-DC conversion.

LCD Voltage Circuit (DC-DC Converter Circuit)

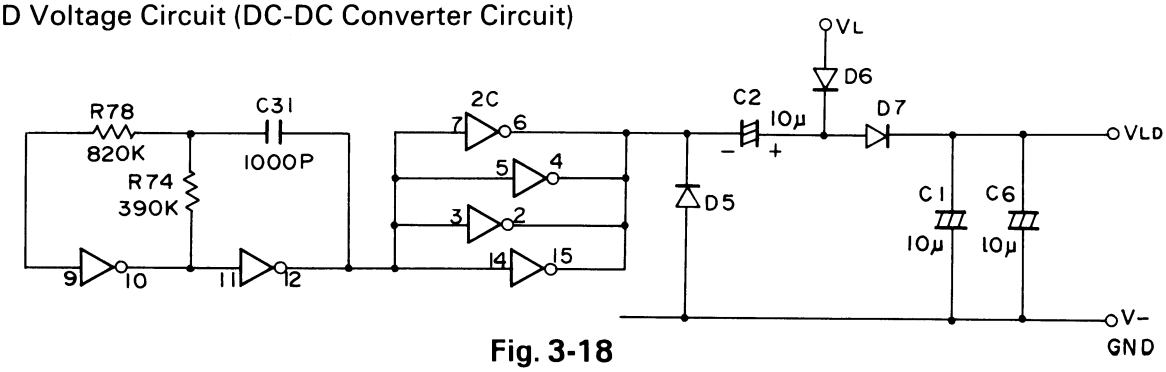


Fig. 3-18

The oscillator circuit shown in the left part of the above circuit diagram generates a pulse having a period of about 0.8 msec, which is fed to IC 2C, where its 4 drivers boost the pulse drive capacity. A capacitor C2 is installed on the output side of IC 2C. The output of IC 2C shifts the negative voltage of capacitor C2 so the positive voltage of C2 rises higher than V_L (+5V), causing the capacitor to discharge.
As a result, a voltage such as shown below is routed via diode D7 to capacitors C1 and C6 to be smoothed and output.

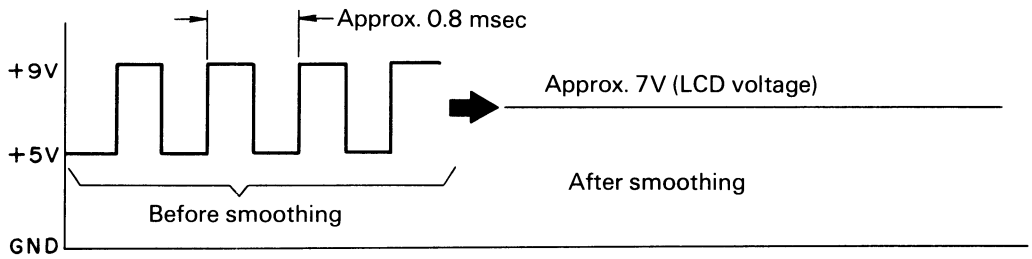


Fig. 3-19

3.1.12 Power Signals

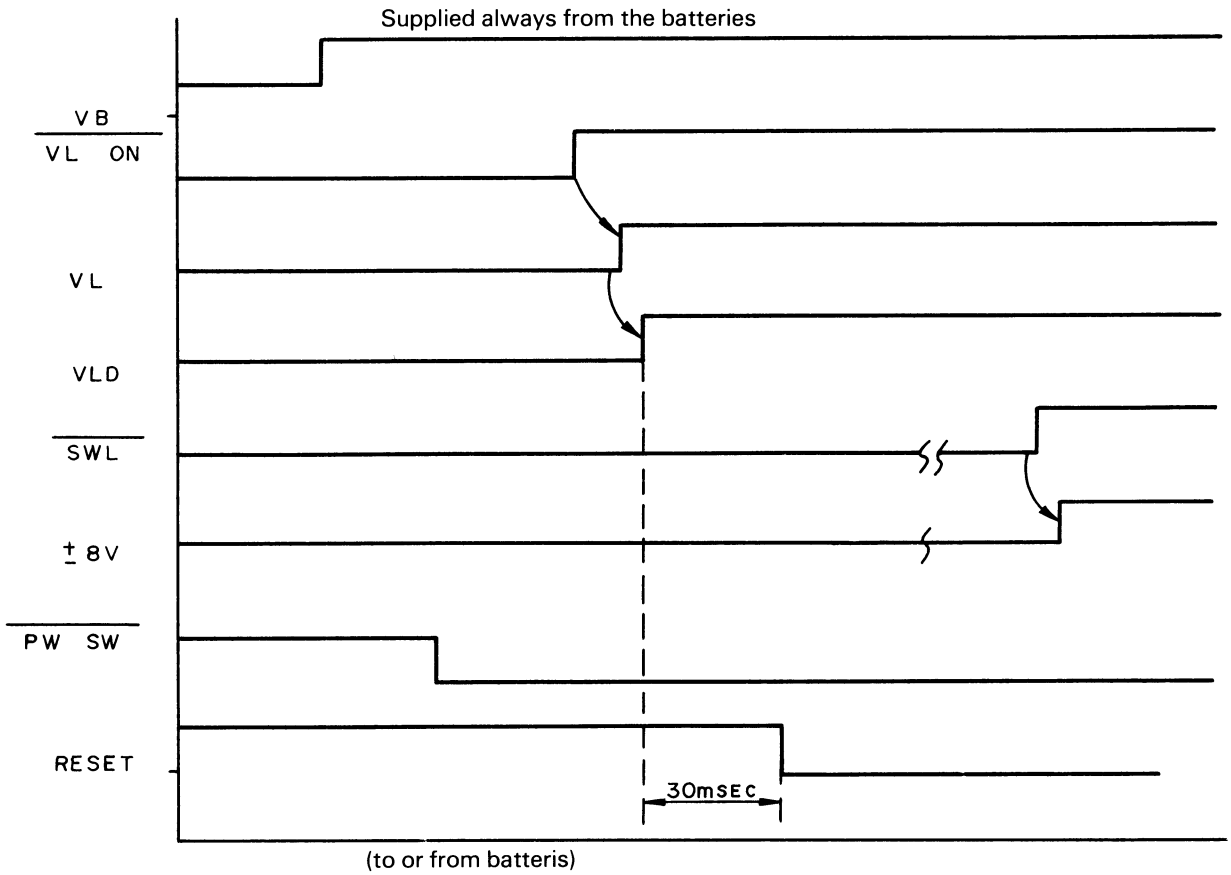


Fig. 3-20

Signal	Signal Direction	Meaning of Signal	NOTE
$\overline{\text{PW SW}}$	Incoming	Power switch signal	$\overline{\text{PW SW}}$ (CN4-19) ..... Interruption for power on or off $\overline{\text{PW SW}}$ (CN5-18) ..... Voltage detector circuit starts.
V_B	Outgoing	Backup voltage for C-MOS, RAM, etc. (for printer)	Battery voltage 4.5V to 6.0V (operating range)
$\overline{\text{VL ON}}$	Incoming	Power on signal	Output upon resetting after $\overline{\text{PW SW}}$ signal is output.
V_L	Outgoing	Line voltage on signal	Starts supplying after $\overline{\text{VL ON}}$ signal detection.
V_{LD}	Outgoing	LCD voltage	About 7V is generated for LCD from battery voltage.
$\overline{\text{SWL}}$	Incoming	± 8V power on signal	Output only when RS-232C is operating.
± 8V	Outgoing	RS-232C voltage	Output by $\overline{\text{SWL}}$ singnal.
RESET	–	Initializes circuits	

3.2 CPU Operation

3.2.1 Main CPU/Slave CPU

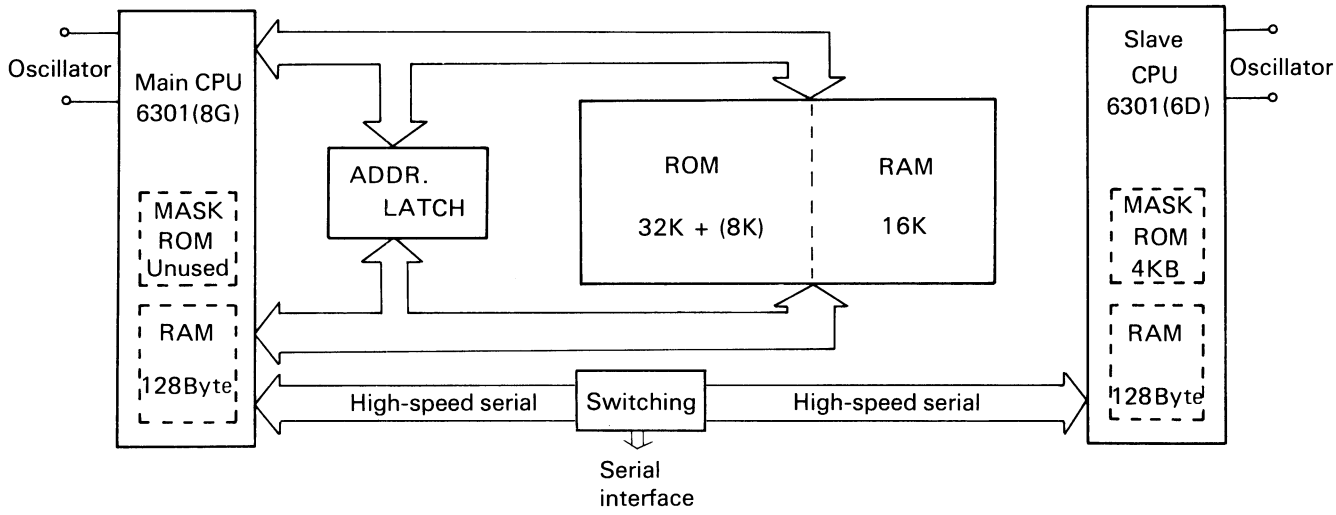


Fig. 3-21

The HX-20 is of a dual CPU system that uses two CPU 6301s to allow dispersed processing. The main CPUs are operated by the control program stored in the external RAM, and control 1) the keyboard, 2) liquid crystal display, 3) ROM and RAM addresses, 4) bar code reader, and 5) clock. The main CPUs do not use the built-in mask ROM, but only the program stored in the external ROM, for control purposes. The slave CPU has a control program in its built-in mask ROM (4 kb), and controls 1) audio cassette, 2) printer, 3) bar code reader, 4) RS-232C, 5) high-speed serial, 6) cartridge option, and 7) power off independently of the main CPUs. The slave CPU is connected to the main CPUs with 38,400 bps high-speed serial lines through which commands and data are sent and received as necessary for control.

3.2.2 CPU Timing

The CPU 6301s which play the central role in control operation are 8-bit microcomputer units (MCUs) that have a low power consumption mode and an error detection function, and execute commands at the timing shown on the next page.

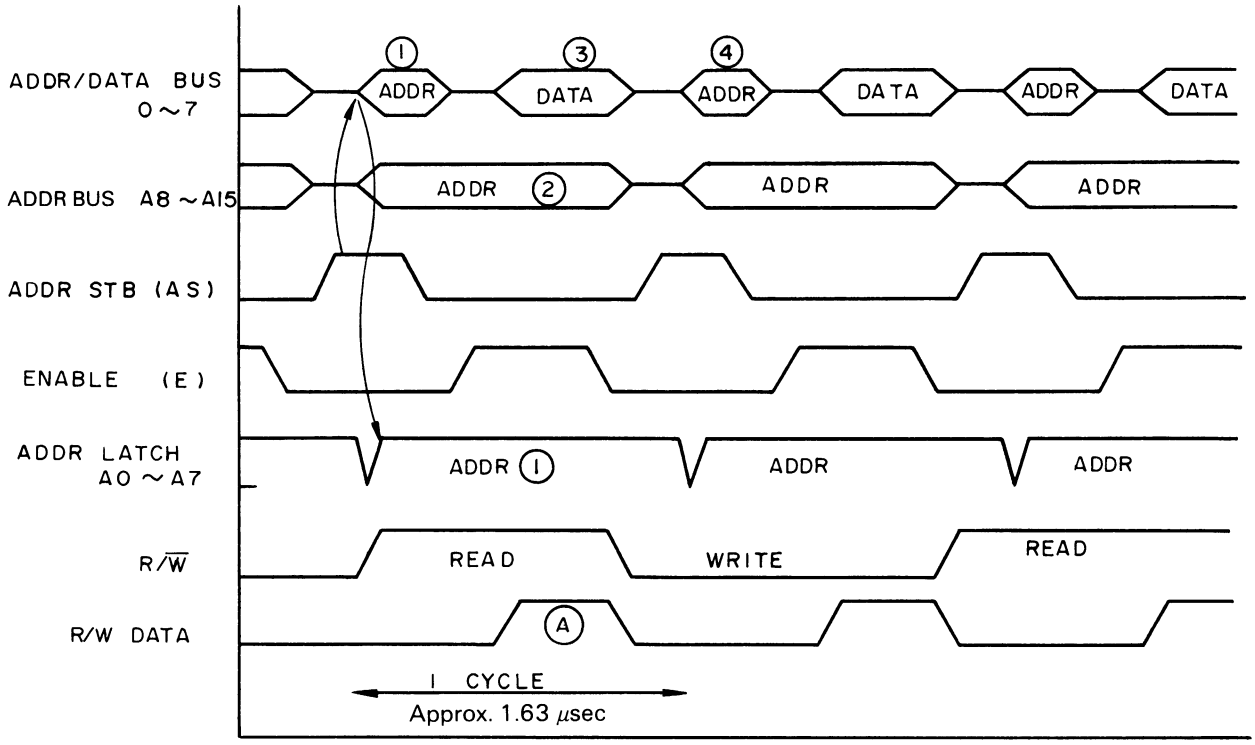


Fig. 3-22

The CPU is connected to an external oscillator from its pins 2 and 3. The clock pulse of 2.4516 MHz generated by the external oscillator is divided by 4 in the CPU to generate a system clock of about 1.63 μsec. In read operation, after an address strobe (AS) is sent out, address ① is output to the address data bus lines, and is held until address ④ reaches the address latches. When address ② is output, the desired ROM and its data address are designated. As an ENABLE (E) signal is output, 1 byte of data Ⓐ (program) is output to the data buses to be taken into the CPU 6301.

In write operation, a RAM address is designated as in read operation, and if data is output with the R/$\overline{W}$ signal at low level, data can be written into the designated I/O or RAM.

3.2.3 Address/Data Buses

The main CPU has 16 address lines (DA0 to A15) and 8 data lines (DA0 to DA7), and addresses of up to 64 kilobytes can be directly designated. The bus lines, CPU, and ROMs are connected one to another as shown below.

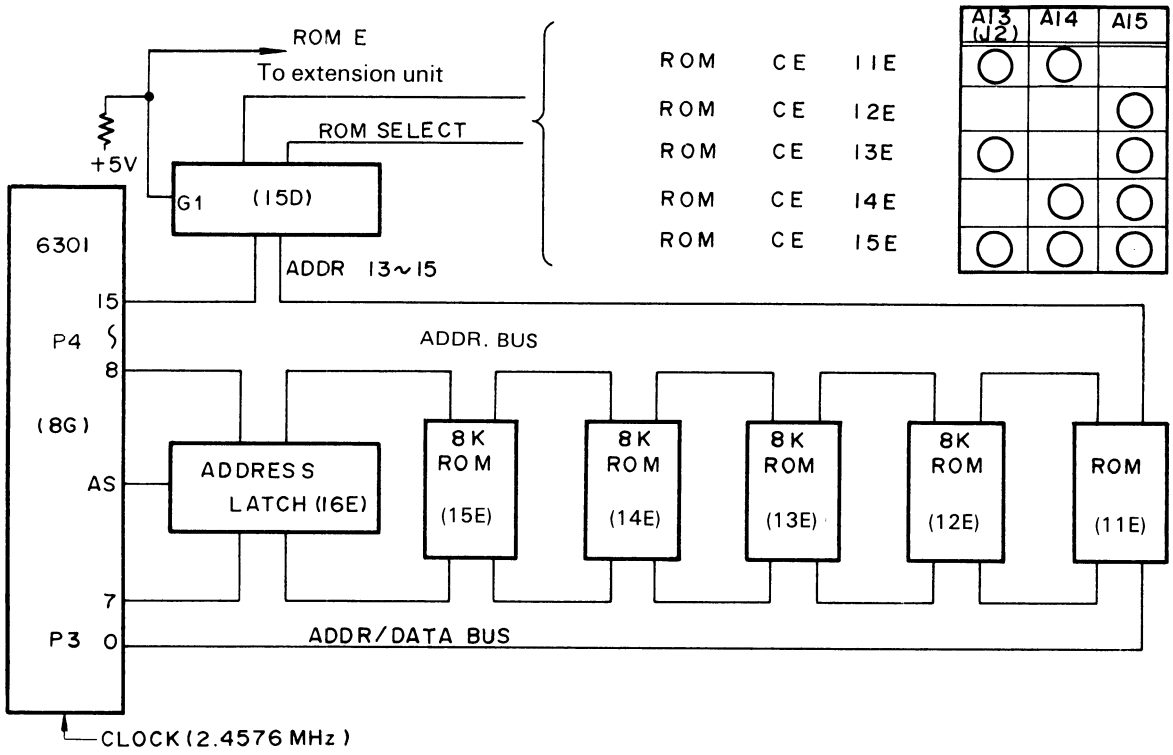


Fig. 3-23

Here, the main CPU operates in the expanded multiplex mode.
The address buses of the CPU 6301 share the lower bits 0 to 7 with the data buses. Therefore, addresses and data are separately used by means of an AS signal, and address latch 16E is used to hold the lower addresses. A decoder 15D is used for the upper addresses A13 to A15 to select ROM chips.
Other addresses A8 to A12 and lower addresses A0 to A7 are used for ROM address designation. (The 13 bits of A0 to A12 can be used for designating up to 8 kilobytes of addresses, which correspond to the chip capacity of one ROM.)

3.2.4 Initialization

Upon completion of resetting after power on, the main CPUs execute the program stored in the external ROM to initialize the system (from mode designaion to display of a menu on the screen) as illustrated on the Fig. 3-24, 25.

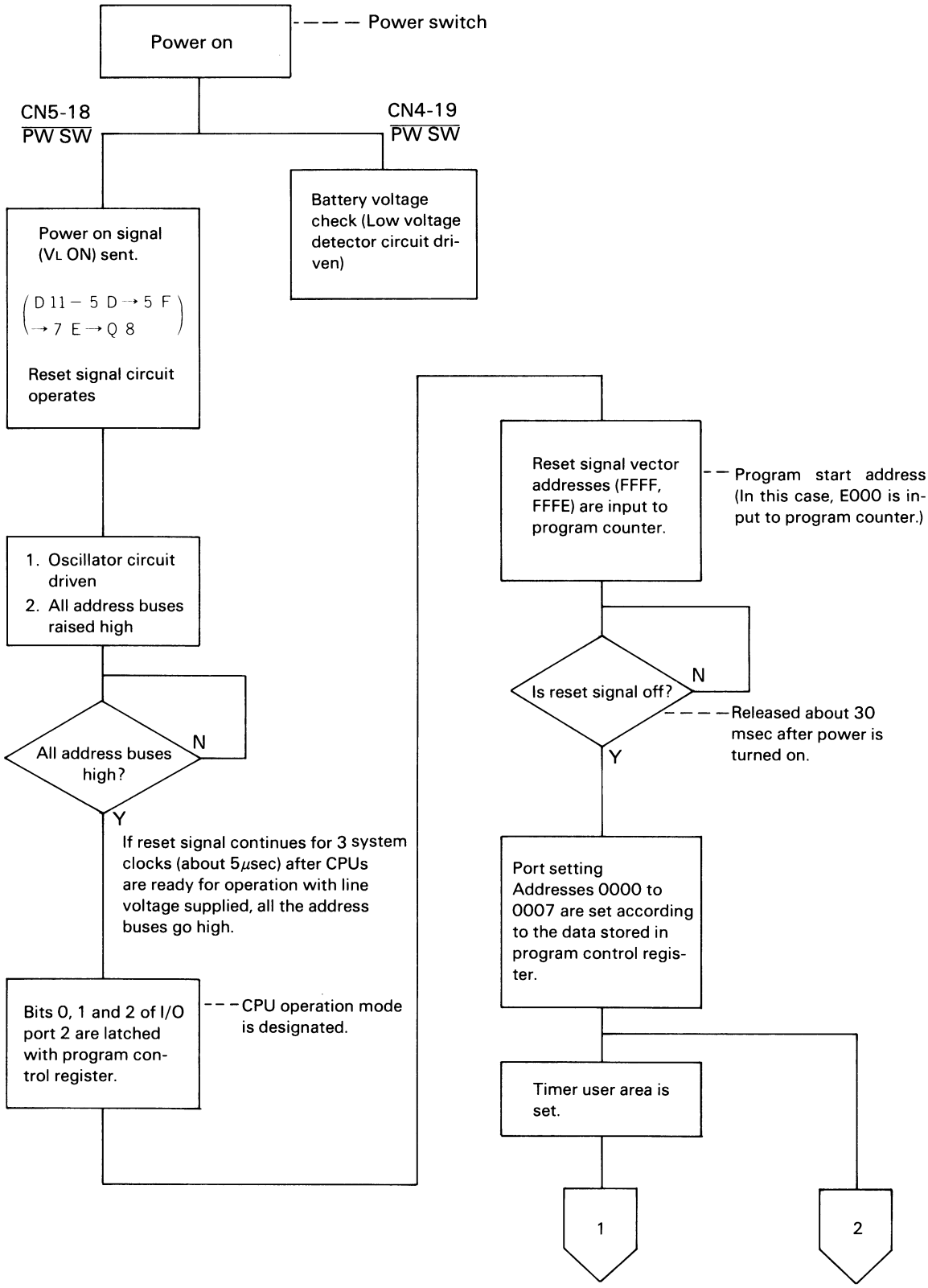

Power on
Power switch
CN5-18
PW SW
CN4-19
PW SW
Battery voltage check (Low voltage detector circuit driven)
Power on signal (VL ON) sent.
(D11 – 5 D → 5 F → 7 E → Q 8)
Reset signal circuit operates
1. Oscillator circuit driven
2. All address buses raised high
All address buses high?
N
Y
If reset signal continues for 3 system clocks (about 5μsec) after CPUs are ready for operation with line voltage supplied, all the address buses go high.
Bits 0, 1 and 2 of I/O port 2 are latched with program control register.
CPU operation mode is designated.
Reset signal vector addresses (FFFF, FFFE) are input to program counter.
Program start address (In this case, E000 is input to program counter.)
Is reset signal off?
N
Released about 30 msec after power is turned on.
Y
Port setting
Addresses 0000 to 0007 are set according to the data stored in program control register.
Timer user area is set.
1
2

Fig. 3-24

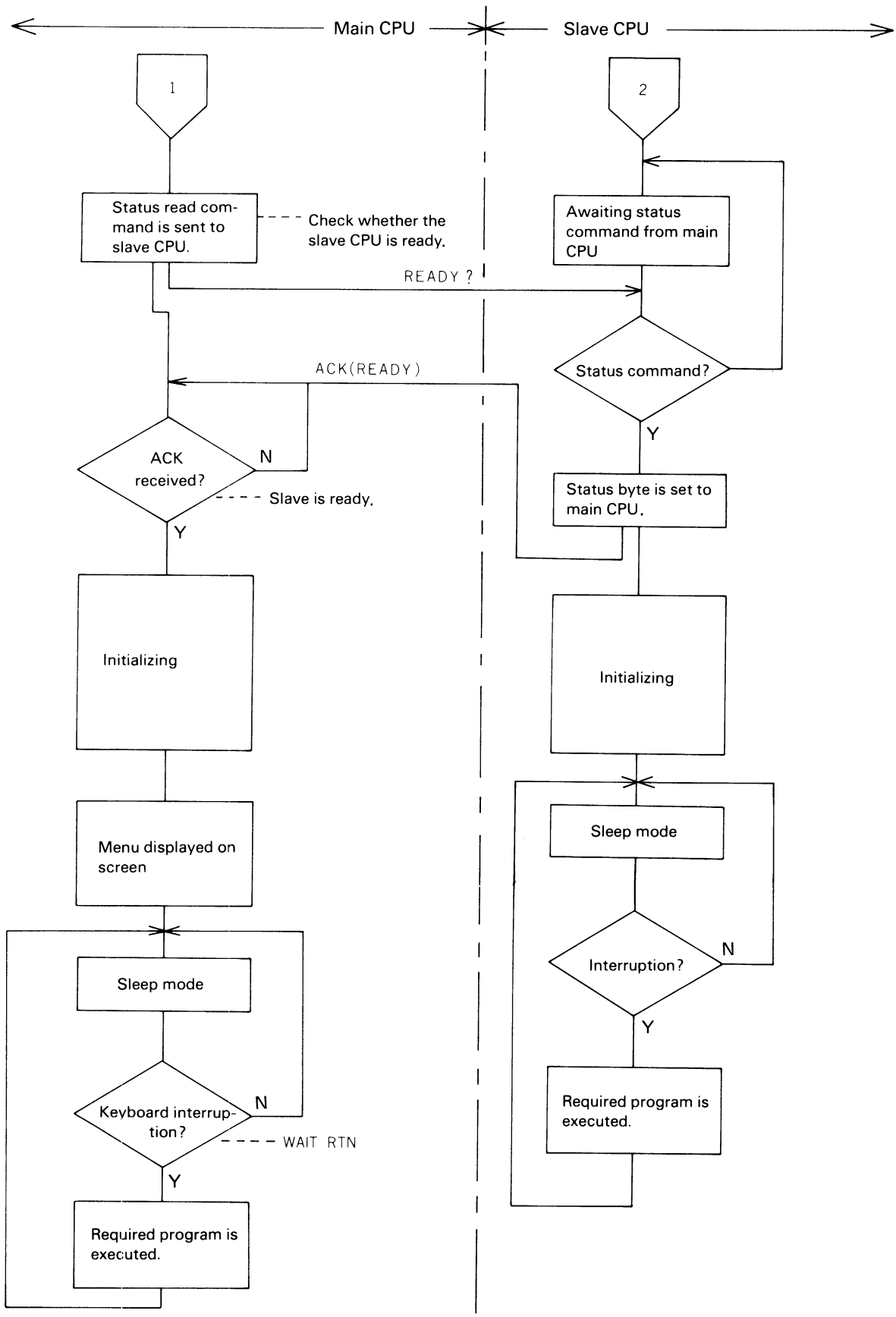

Main CPU
Slave CPU
1
2
Status read command is sent to slave CPU.
Check whether the slave CPU is ready.
Awaiting status command from main CPU
READY ?
Status command?
ACK(READY)
Y
ACK received?
N
Slave is ready.
Status byte is set to main CPU.
Y
Initializing
Initializing
Menu displayed on screen
Sleep mode
Sleep mode
Interruption?
N
Y
Keyboard interruption?
N
WAIT RTN
Y
Required program is executed.
Required program is executed.

Fig. 3-25

An outline of operation after power is turned on is as shown below. The same takes place when the reset is pressed.

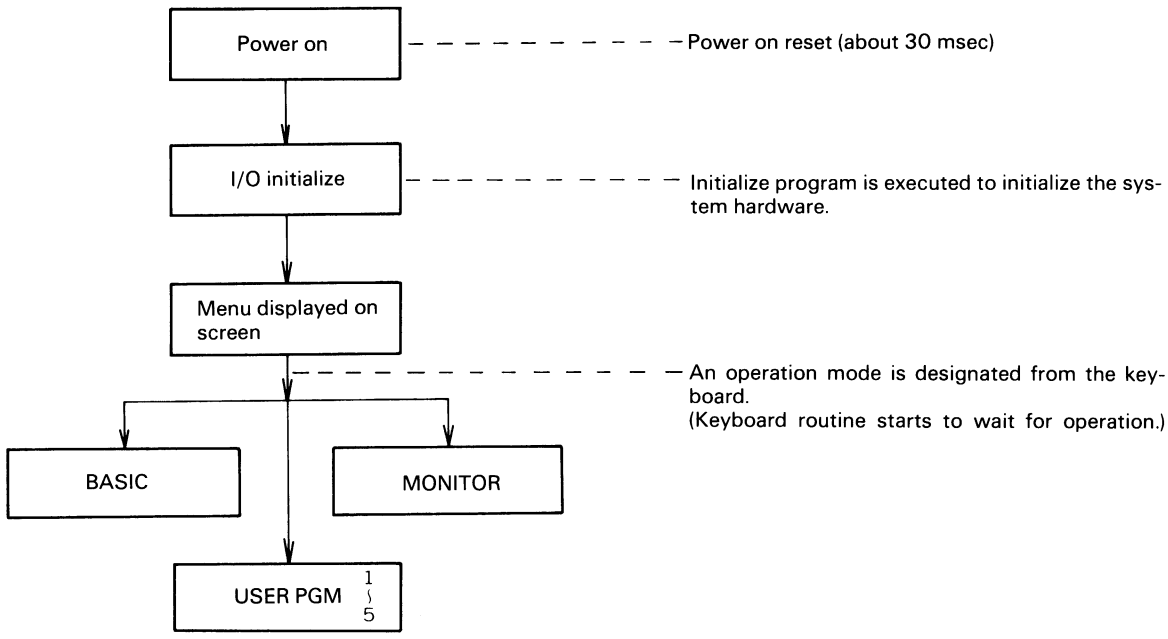


Fig. 3-26

The main and slave CPUs read operation mode selection data and program start address (a vector address corresponding to the reset signal) while the reset signal is in effect. After reset signal is released, the main and slave CPUs are initialized.

After initializing, the slave CPU immediately goes into the sleep mode. The main CPU goes into the sleep mode as the keyboard routine starts after a menu is displayed on the screen. After the menu display, both the main and slave CPUs are in the sleep mode. The sleep mode can be released only by key switch interruption. The purpose of this is to minimize power consumption while the CPUs are not being used.

3.2.5 Sleep Mode

(1) Because the HX-20 operates on battery power, it is designed to operate the CPUs not constantly but only when necessary for minimizing power consumption. CPU operation is stopped and turned into the sleep mode by executing a SLP command. Power consumption is reduced in the sleep mode to about 1/10 of the power consumed when the CPUs are operating.

- Operations in the sleep mode
  - The CPUs stop operating, but the data stored in the registers are kept intact.
  - The peripheral functions other than the CPUs do not stop.
  - ENABLE and AS signals are output.
  - All the address and data bus lines go high.
- Sleep mode release
  - Reset signal detected
  - Interruption signal detected

(2) Control incidental to the sleep mode

The sleep mode is selected by executing the keyboard routine. The program which effects the sleep mode is located in addresses E000 to EFFF. The sleep mode can be released by interruption. Its control program is located in addresses F000 to FFFF. If an interruption occurs, CPU operation must start after the sleep mode is released.
Otherwise, the interruption will not be processed.

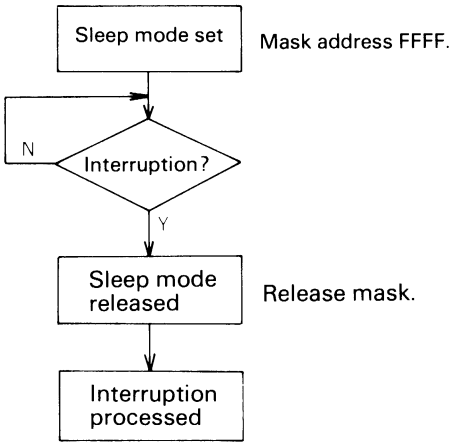


Fig. 3-27

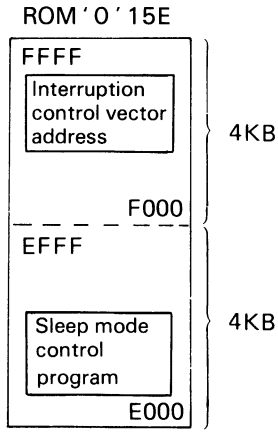


Fig. 3-28

When selecting the sleep mode, address XX2C is output so Pin 9 of IC 8E goes low to latch IC 8E. As a result, Pin 2 of IC 8E remains high after the selection of the sleep mode. All the address bus lines are at high level in the sleep mode.
If an interruption occurs under this condition, an FFFF (reset/trap error) is output as a vector address. If no control is performed then, it is processed in a way different from the normal interruption processing.
Because IC 8E is latched when the sleep mode is selected, the FFFF (A12) output lowers the output from Pin 3 of IC 8E, causing the G2A signal from IC 15D to go high.
Thus, no ROM select is output and vector address FFFF is ignored.
Then, the CPUs execute the sleep mode control program in addresses E000 to EFFF to release the sleep mode. In this case, address line A12 will not turn on so ROM selection is possible and the program can be executed. IC 8E is released from its latched state when address XX26 is output.
Now interruptions can be processed. If an interruption occurs, it is processed by using a vector address.

(3) RAM/ROM select circuit

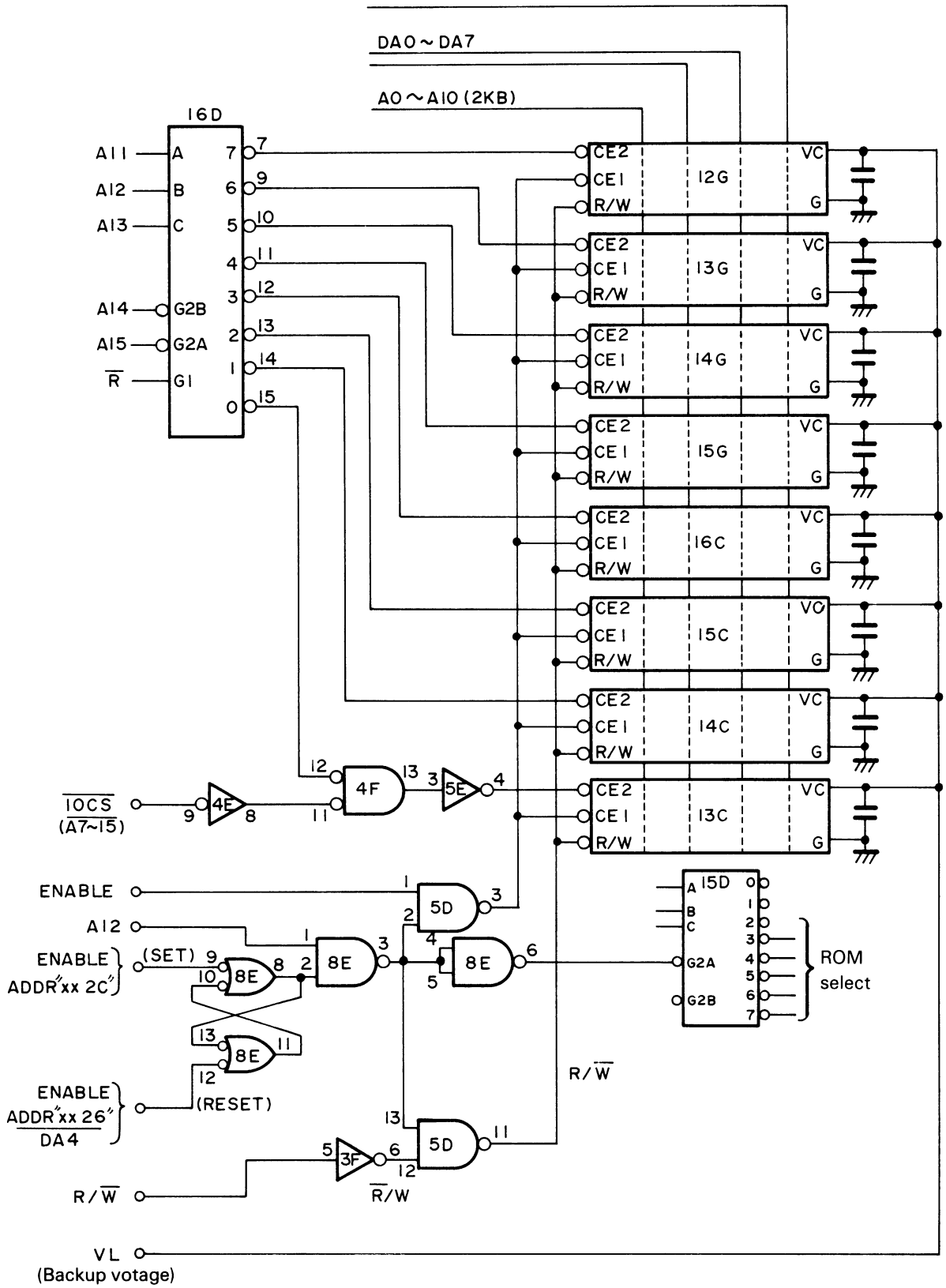


Fig. 3-29

3.2.6 Memory Map

After power is turned on, or when executing a program, the control programs control all input and output operations by means of addresses and interruptions. That is, the system components are controlled by outputting the required data to the addresses (I/O equipment) shown below, or receiving data or interruptions.

(1) ROM addresses

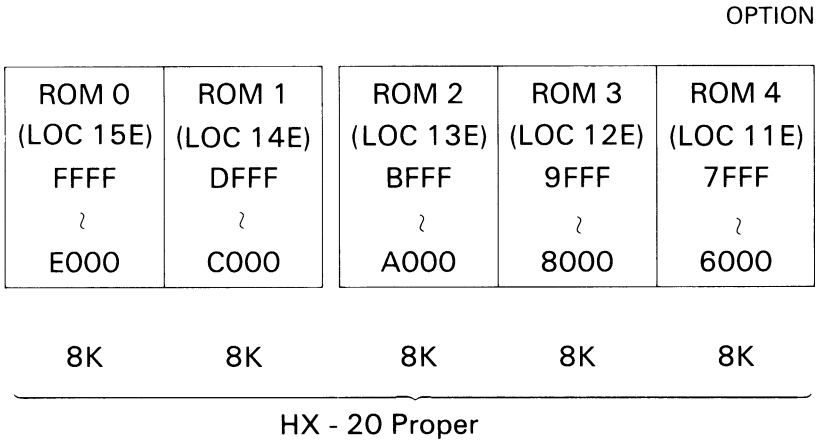


Fig. 3-30

The HX-20 can mount 40K of ROMs (standard 32K, option 8K). ROM 0 (monitor) and ROM 1 (utility) have the following control programs built in.

- Keyboard : Data input
- Display : LCD and TV monitor character display, cursor control, etc.
- Character generator : Character pattern
- Clock : Clock and alarm set and read
- Printer : Print, paper feed, screen copy
- Speaker : Sound frequency and length control
- ROM cartridge : Program read
- Microcassette : Read/write, search
- Audio cassette : Read/write
- RS-232C : Data send/receive
- Disk : Read/write
- Monitor : Memory dump, memory set, etc.

(2) Main CPU address map

Addresses 0000 to 00FF are in the main CPUs and address 0100 and subsequent addresses are in the external RAM (13C to 16C, 12G to 15G, and extension unit).

Address	Meaning
0000 ~ 0007	Port control and register PORT 1 — PORT ADDR 0002 — DIRECTION REG. 0000 (RS-232, etc.) PORT 2 — PORT ADDR 0003 — DIRECTION REG. 0001 (Serial, RS-232, bar code) PORT 3 — PORT ADDR 0006 — DIRECTION REG. 0004 (A0 ~ A7, D0 ~ D7) PORT 4 — PORT ADDR 0007 — DIRECTION REG. 0005 (A8 ~ A15)
0008 ~ 000F	Timer control and data registers 0008 : Timer control 0009 ~ 000A : Free running counter ..... CPU R/W 000B ~ 000C : Output compare register ..... R/W 000D ~ 000E : Input capture register ..... READ 000F : P3 control register
0010 ~ 0013	Serial control and registers 0010 : Serial speed rate 0011 : Serial control status 0012 : Receive data register 0013 : Transmission data register
0014	RAM control : External RAM/internal RAM switching
0015 ~ 001F	Unused
0020	Keyboard scan KSC 0 to 7 outputs/SW6 read
0022	Keyboard inputs KRTN 0 to 7
0026	Cartridge interface/interruption mask release/LCD chip select/key mask
0028	Keyboard inputs KRTN 8 to 9, $\overline{\text{PW SW}}$, $\overline{\text{BUSY}}$ (SO)
002A	Serial clock generated by ANDing $\overline{\text{R}}$/W signal
0040 ~ 004D	Clock register 0040 : Sec — 0041 : Sec (alarm) 0042 : Min — 0043 : Min (alarm) 0044 : Hr — 0045 : Hr (alarm) 0046 : Day of week — 0047 : Date 0048 : Month — 0049 : Year 004A ~ 004D : Control register
004E ~ 007F	RAM RAM area for system 50 bytes

Address	Meaning
0080 ≀ 00FF	RAM built in CPU (128 bytes)
0100 ≀ FFFF	External RAM

(3) Slave CPU memory map

The slave CPU controls the printer and other I/O equipment with its built-in mask ROM (4 kb).

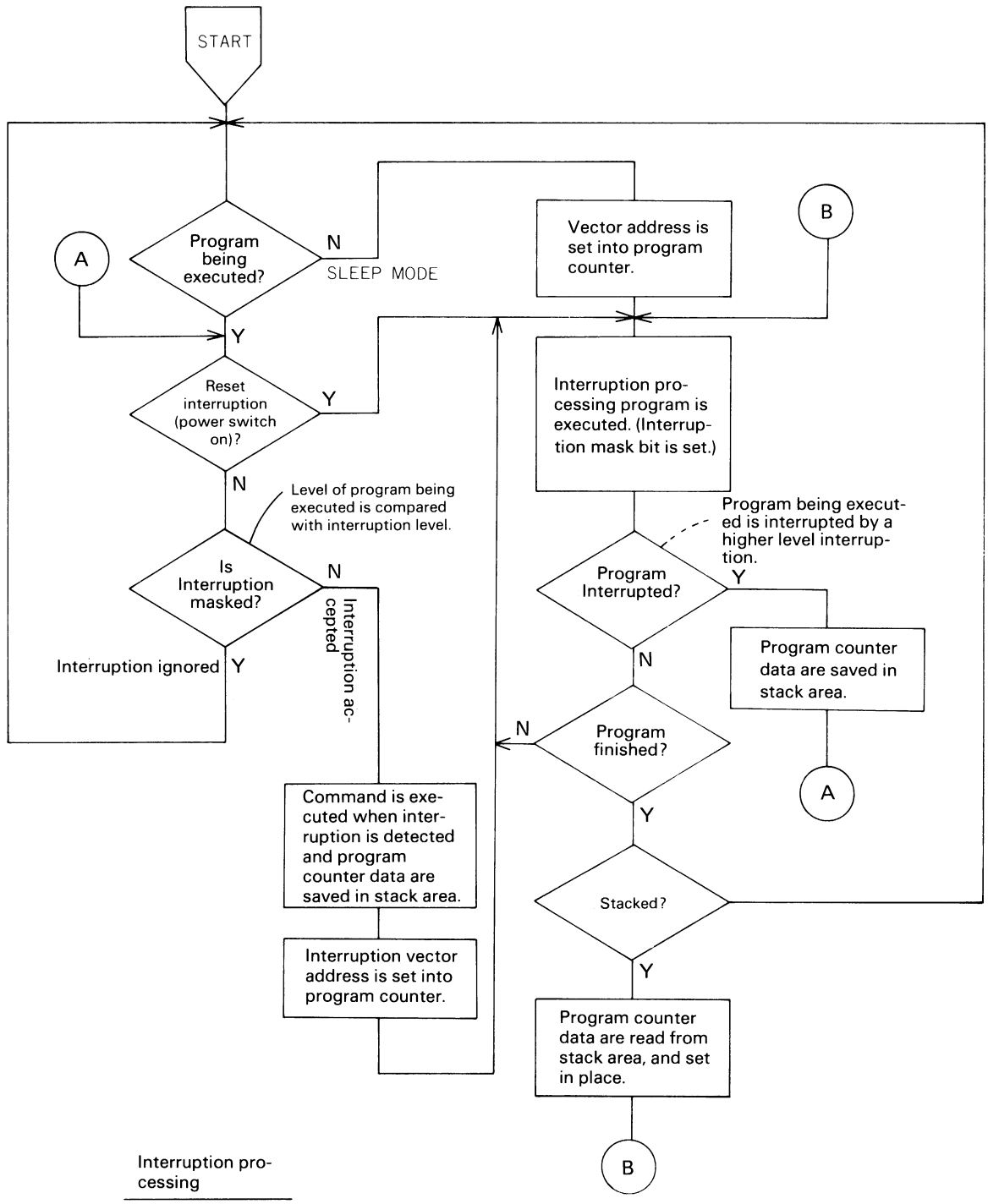
Address	Meaning
0000 ≀ 0007	Port control and register PORT PORT ADDR DIRECTION REG. 1 0002 0000 Printer, speaker 2 0003 0001 CPU COMM, etc. 3 0006 0004 RS-232C, cassette, etc. 4 0007 0005 RS-232C, cartridge
0008 ≀ 000F	Timer control and data registers 0008 : 0009 ~ 000A : 000B ~ 000C : 000D ~ 000E : 000F :
0010 ≀ 0013	Serial registers 0010 0011 0012 0013
0014	RAM control : External/internal RAM switching
0015 ≀ 007F	Unused
0080 ≀ 00FF	Internal RAM (128 bytes)
0100 ≀ DFFF	Unused (Addresses are not physically present.)
F000 ≀ FFFF	Internal ROM (4 kb)

3.2.7 Interruption Control

An interruption signal is used by an I/O equipment in requesting the CPUs for some processing.

As shown in the interruption table, there is the preset priority order according to the kinds of interruption. Each vector address has an address to start the program (interruption processing program) that is required for processing an interruption request. If an interruption request occurs, the level of the program being executed and the kind of the interruption are checked; and if the interruption request has a high level, the data of the program counter and registers are saved in the stack area, and the interruption request is processed.

Interruption acceptance and processing procedures are as shown in the flow chart below.



Interruption mask bit : Condition code register

Fig. 3-31

3.2.8 Main CPU Interruption Table

Interruption priority	VECTOR	Reason for Interruption
HIGHEST	FFFE FFFF	• Immediately after power up After reset
	FFFE FFFF	• Address error or operation code error (TRAP) ..... used for monitor
	FFFC FFFD	• Master clear by $\overline{\text{NMI}}$ signal interruption (Unused)
	FFFA FFFB	• Software interruption (Unused) ..... Only where developed unit is used.
	FFF8 FFF9	• Key input ($\overline{\text{K.B REQUEST}}$ signal) • Power on (PW SW signal) • Power off (PW SW signal) • Clock ($\overline{\text{CLOCK IRQ}}$ signal) • External interruption ($\overline{\text{INT EX}}$ signal)
	FFF6 FFF7	• Timer input capture (Unused)
	FFF4 FFF5	• Timer output capture (Keyboard)
	FFF2 FFF3	• Timer overflow (Microcassette)
LOWEST	FFF0 FFF1	• Interruption by serial communication interface (PIN signal)

3.2.9 Slave CPU Interruption Table

Interruption priority	VECTOR	Reason for Interruption
HIGHEST	FFFE FFFF	• Immediately after power on • After reset
	FFFE FFFF	• Address error or operation code error (TRAP)
	FFFC FFFD	• Master clear by NMI signal interruption
	FFFA FFFB	• Software interruption
	FFF8 FFF9	Unused
	FFF6 FFF7	• Timer input capture
	FFF4 FFF5	• Timer output capture
	FFF2 FFF3	• Timer overflow (Microcassette)
LOWEST	FFF0 FFF1	• Interruption by serial communication interface

3.3 Address Control Circuit

3.3.1 Memory Addressing

Addresses in the internal RAMs can be designated by CE2 (chip enable) signal from IC 16D, address lines (2 kb from A0 to A10) to each RAM chip, and CE1 signal; and addresses in the external RAM (in the extension unit) by address lines A0 to A15 (up to 64 kilobytes can be designated). The HX-20 uses an aditional RAM or buffer (main CPU/clock IC 146818/LCDμPd7227) which uses the same addresses. Thus, control signals are necessary to signal out the RAM to be used.

3.3.2 Address Control Signals

(1) The basic control signal is the $\overline{\text{IOCS}}$ signal that is output at Pin 8 of IC 2E. The $\overline{\text{IOCS}}$ signal is output where address lines are $\overline{\text{A7 – A15}}$ so if this signal is output, it indicates addresses 0000 to 007F.

(2) Auxiliary control signals include IC 9E and incidental I/O address control signals.

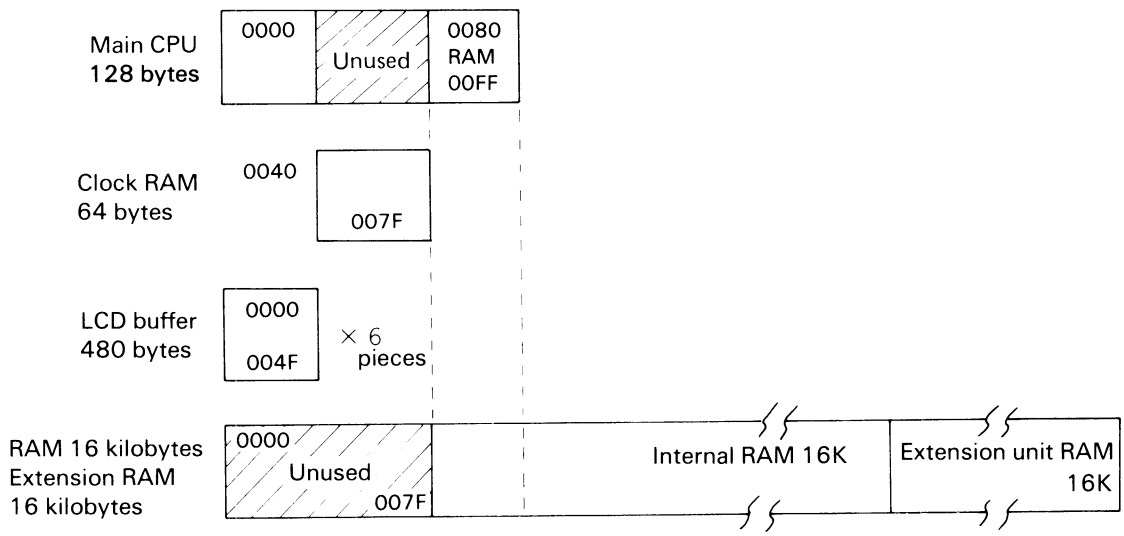


Fig. 3-32

- Main CPU

  Bit 6 of the RAM control register (address 0014) in the main CPU controls the RAM in the CPU or an external RAM.

  If bit 6 is on, the buit-in RAM in the CPU is used so no R/W operation is performed for the external memories.

- Built-in RAM/extension RAM

  If the $\overline{\text{IOCS}}$ signal ($\overline{\text{A7 – A15}}$) is output, it is applied to Pin 9 of IC 4E, and an inverted signal is output at Pin 8. RAM chip select IC 16D has its pin 15 at low level due to $\overline{\text{A11 – A15}}$, but Pin 11 of IC 4F is at high level ($\overline{\text{IOCS}}$ on) so that Pin 13 goes low and Pin 4 of IC 5E goes high. As a result, CE2 form RAM 13C is not turned and the built-in RAM cannot be designated.

  The $\overline{\text{IOCS}}$ signal is also supplied from connector CN7 to the extension unit so the RAM in the extension unit cannot be designated either.

  For the reasons described above, addresses 0000 to 007F represent the CPU RAM or LCD buffer or clock RAM.

- LCD buffer

  The LCD has a total of 6 buffers (480 bytes in total) that can be designated by addresses 0000 to 004F (80 bytes). These addresses are designated by setting the data pointer (made of 7 bits) in the LCD by the LID command (Load Immediate to Data Pointer), and each of the 6 buffers (80 bytes each) is designated by CS (chip select). Thus, the main CPU does not directly designate addresses. It uses only LCD addresses 0026 and 002A for addressing.

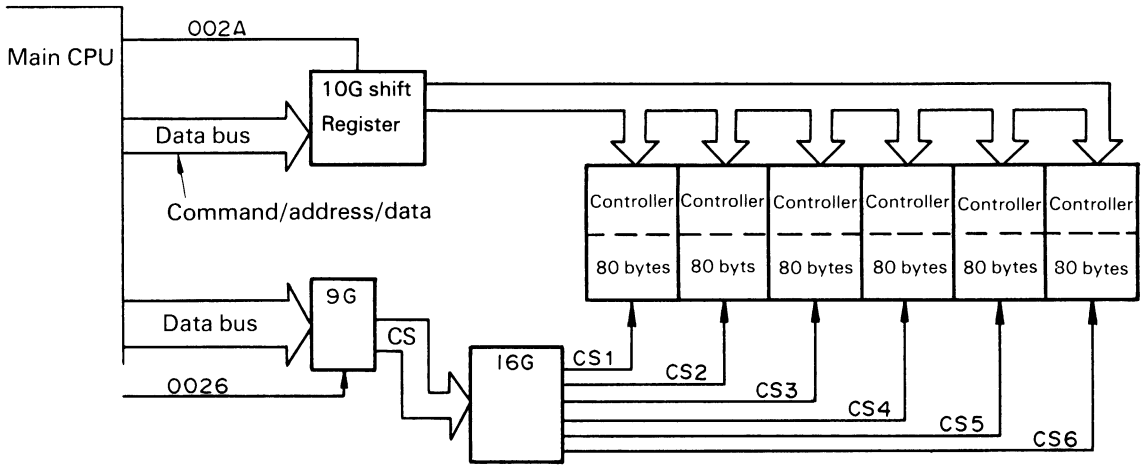


Fig. 3-33

- Clock RAM

  Access to the clock RAM is controlled by Pin 13 (E) of IC 6G. Its signal is supplied to clock IC 6G via Pin 8 of IC 1E, IC 4F and IC 5E only when $\overline{\text{IOCS}}$ ($\overline{\text{A7 – A15}}$) and A6 (address 0040 or higher) are on. While this address space is being selected, Pin 13 of IC 6G remains at low level, which permits read/write.

Address \ Bit	7	6	5	4	3	2	1	0
XX40	0	1	0	0	0	0	0	0
XX7F	0	1	1	1	1	1	1	1

Fig. 3-42

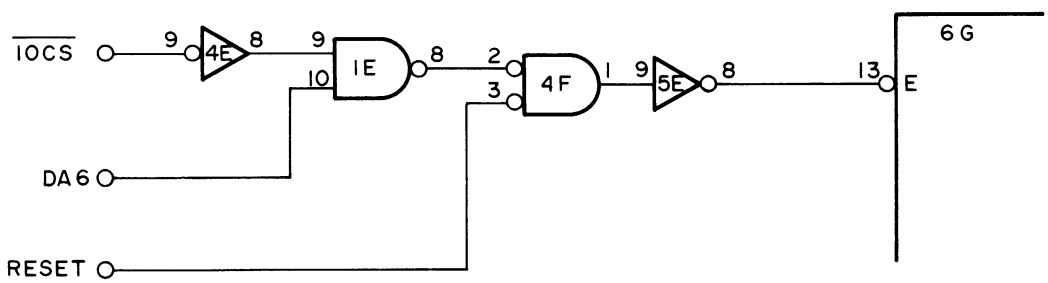


Fig. 3-34

3.3.3 RAM Address Circuit

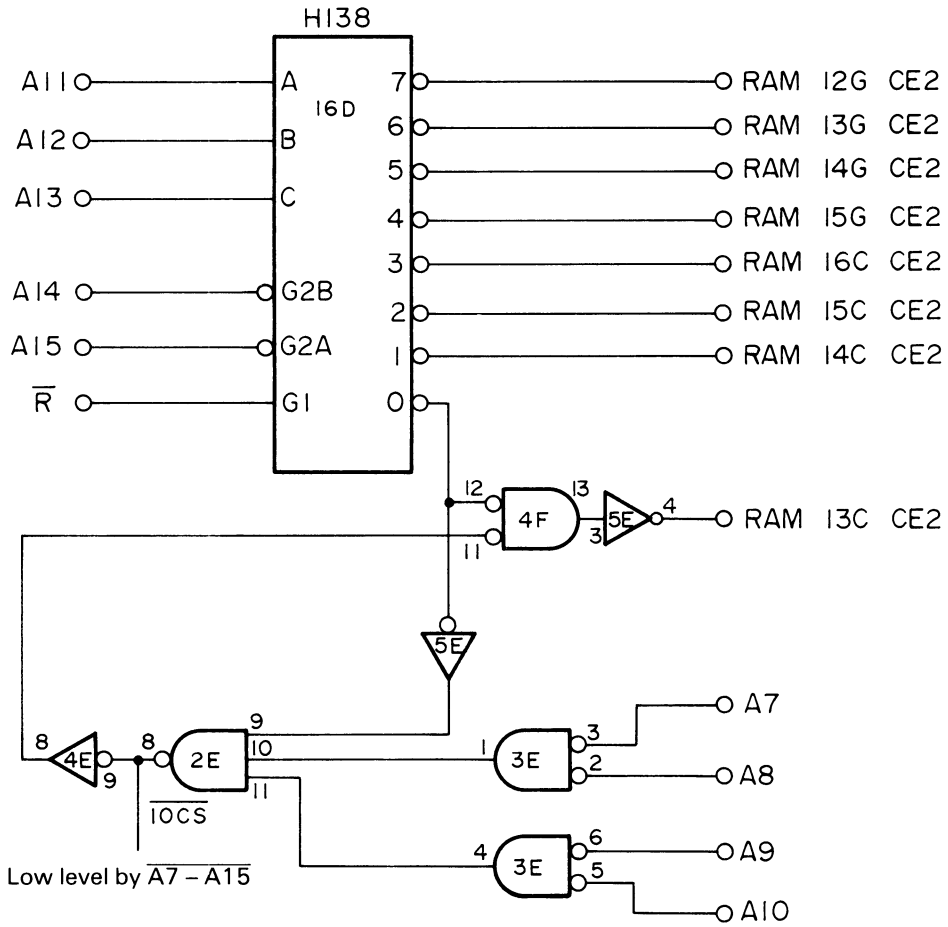


Fig. 3-35

Loc.	ADDRESS																RAM ADDR. RANGE
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
13C	●	●	●	●	●												0000 (0080) ~ 07FF
14C	●	●	●	●													0800 ~ 0FFF
15C	●	●	●		●												1000 ~ 17FF
16C	●	●	●														1800 ~ 1FFF
15G	●	●		●	●												2000 ~ 27FF
14G	●	●		●													2800 ~ 2FFF
13G	●	●			●												3000 ~ 37FF
12G	●	●															3800 ~ 3FFF

* No output is sent to those address bits marked with a black dot.

Fig. 3-36

3.3.4 I/O Select

I/O select plays the role of outputting a gate signal from IC 9E shown below to each I/O interface where the I/O addresses (I/O equipment) listed in the memory map are used.

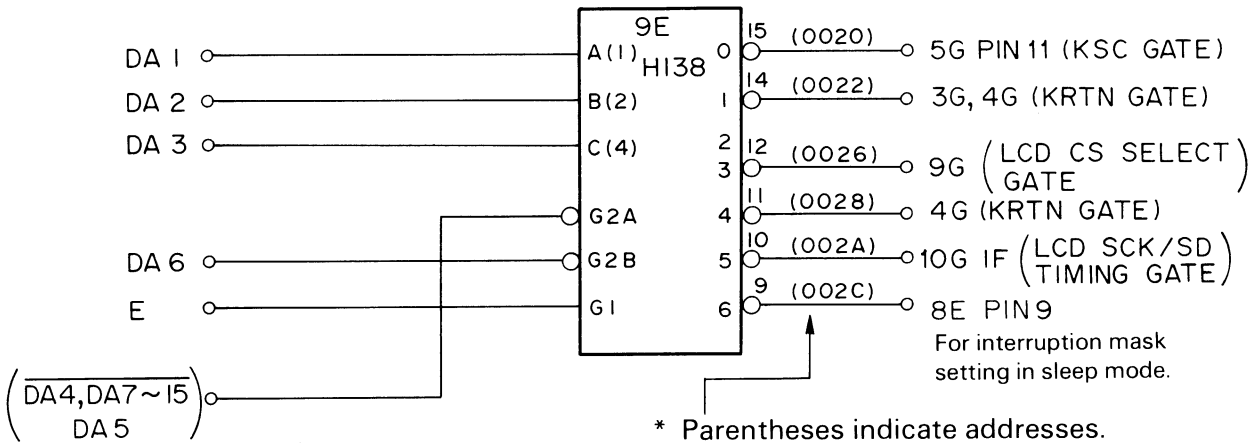


Fig. 3-37

0020 : Outputs an KSC signal output, and scans keyboard data and SW6 status.

0022 : Inputs KRTN signals 0 to 7, and reads the keyboard data scanned by the KSC signal to data buses.

0026 : LCD chip select/ROM cartridge control/interruption mask reset in sleep mode/masking interruption from keyboard by lowering Pin 12 output from IC 9G.

0028 : Reads KRTN signals 8 and 9, $\overline{PW\ SW}$, and BUSY (SO) signals to data buses.

002A : Outputs an $\overline{SCK}$ signal and SD (serial data) to LCD.

002C : Mask interruption by using IC 8E in sleep mode.

3.3.5 Clock Circuit

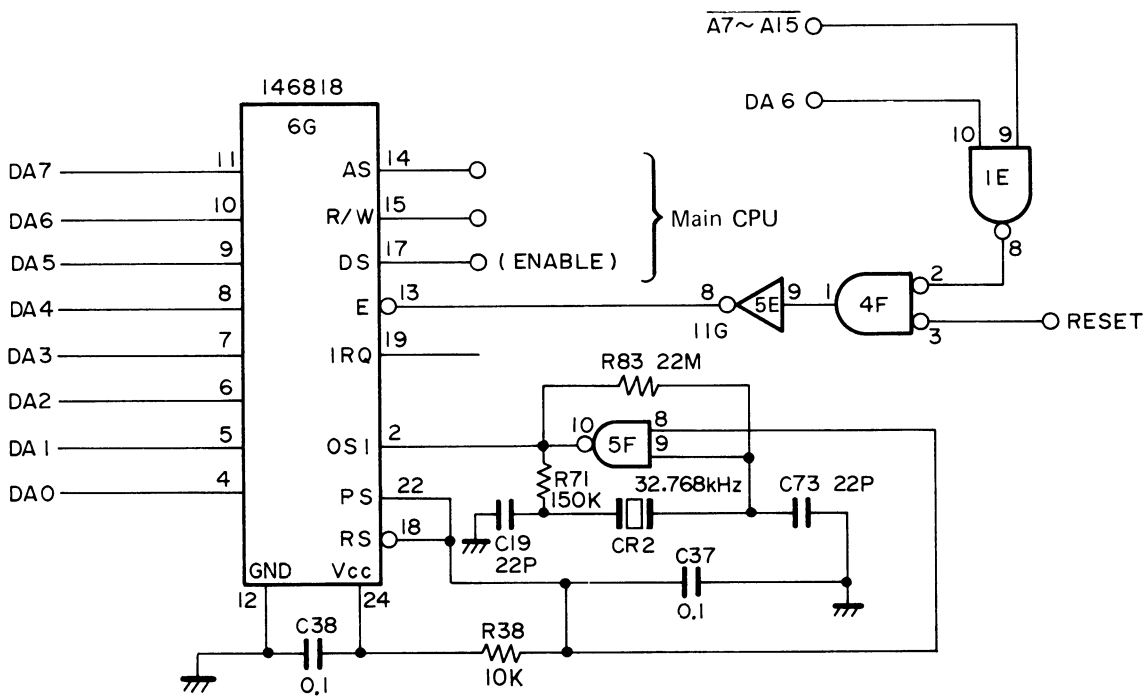


Fig. 3-38

The timer oscillator CR2 generates a basic clock of 32.768 kHz, which is amplified by IC 5F into a clock with a period of about 30 μsec. This clock is supplied to IC 6G to drive the clock IC. IC 146818 uses this basic clock to drive the clock to indicate year, month, day, hours, minutes, and seconds.

IC 146818 has a buit-in register (14 bytes) and RAM (50 bytes) with addresses 0040 to 004D (for the register) and 004E to 007F (for the RAM). Thus, if addresses 0040 to 007F are output, Pin 13 (E) turns on to send an R/W signal, which permits access to the register or RAM.

3.3.6 Dip Switch

(1) Switch 6 (Dip switch with 4 positions)

If a monitor program and a utility programs are in ROM locations 11E and 12E, an international character set can be selected by operating this switch.

These switch signals are read to data bus DA1 via the KRTN9 signal by KSC signals 0 to 3.

Country / Hex. code	U.S.A.	France	Germany	England	Denmark	Sweden	Italy	Spain
23	#	#	#	£	#	#	#	Pt
24	$	$	$	$	$	¤	$	$
40	@	à	§	@	@	É	@	@
5B	[	°	Ä	[	Æ	Ä	°	í
5C	\	ç	Ö	\	ø	Ö	\	Ñ
5D	]	§	Ü	]	Å	Å	é	¿
5E	^	^	^	^	^	Ü	^	^
60	`	`	`	`	`	é	ù	`
7B	{	é	ä	{	æ	ä	à	¨
7C	:	ù	ö	³	ø	ö	ò	ñ
7D	}	è	ü	}	å	å	è	}
7E	~	¨	ß	~	~	ü	ì	~

ASCII version international character set

Country / Hex. code	ASCII	France	Germany	Norway	Denmark	Sweden
23	#	#	#	#	#	#
24	$	$	$	¤	$	¤
40	@	à	§	É	É	É
5B	[	°	Ä	Æ	Æ	Ä
5C	\	ç	Ö	ø	ø	Ö
5D	]	§	Ü	Å	Å	Å
5E	^	^	^	Ü	Ü	Ü
60	´	´	´	é	é	é
7B	{	é	ä	æ	æ	ä
7C	:	ù	ö	ø	ø	ö
7D	}	è	ü	å	å	å
7E	~	¨	ß	ü	ü	ü

European version international character set

ROM version	Country	SW3	SW2	SW1
JAPAN	Japan	ON	ON	ON
	America	1	1	1
	France	1	1	0
	Germany	1	0	1
	England	1	0	1
	Demark	0	1	1
	Sweden	0	1	0
	Italy	0	0	1
	Spain	0	0	0
EUROPE	Norway	1	1	1
	France	1	1	0
	Germany	1	0	1
	Sweden	1	0	0
	Denmark	0	1	1
	France (ASCII)	0	1	0
	Germany (ASCII)	0	0	1
	Sweden (ASCII)	0	0	0

Note that France (ASCII), Germany (ASCII) and Sweden (ASCII) are for inputting ASCII characters using French, German and Swedish keyboard respectively.
See table 2 in 4.2.2 Characte set section for corresponding characters.

Input mode

ASCII and EURPE version
- ten key mode (NUM) ..... Lock
- graph (GRPH) ..... shift
- caps lock ..... lock

JAPAN version
- ten key mode (NUM) ..... lock
- kana mode (KANA) ..... lock
- graph mode (CNTL/KANA) ..... lock
- caps lock ..... lock

Normally set *SW4 OFF, and set it ON when the flopy drive TF-20 is interfaced.

3.4 Micro Printer (Model-160)

The EPSON Model-160 prints 24 characters (or 144 dots in graphic printing) per line, and operates at a printing speed of about 0.7 line per second.

3.4.1 Outline of Mechanisms

Fig. 3-39 illustrates exterior view of the EPSON Micro Printer Model-160.

The Model-160 is a mechanical type dot printer whose printing head having four print solenoids arranged in a line in the column moves in the column for a space equivalent to 36 dot-spaces. The printing head moving in the column direction performs one way printing as the four print solenoids are energized one after another.

At the time when the head set returns to the home position, paper is automatically fed by one pitch. The repetition of this operation makes it possible to obtain the prescribed print format.

These operations are performed mainly by a power transmission mechanism, a detecting mechanism, a printing mechanism, a paper feeding mechanism and a ribbon feeding mechanism.

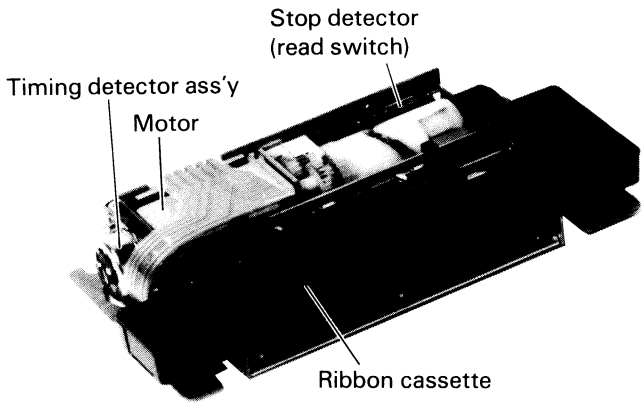


Fig. 3-39

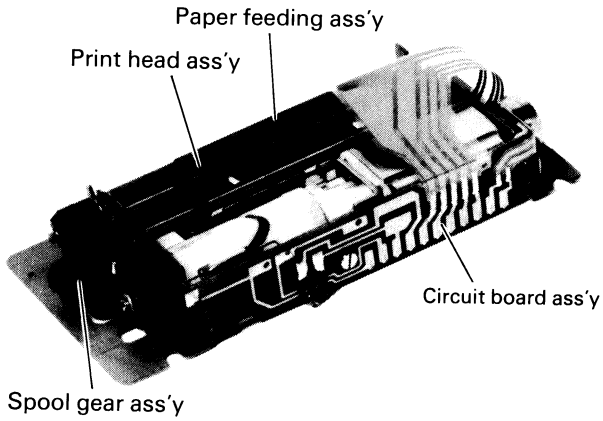


Fig. 3-40

3.4.2 Transmission Mechanism

The transmission mechanism is composed of a reduction gear train, a paper feeding gear train (a part of the paper feeding mechanism), and a ribbon feeding gear train (a part of the ribbon feeding mechanism).

(1) Reduction Gear Train

The reduction gear train consists a motor gear secured on a motor shaft, a reduction gear (large and small position) and an intermediate gear (large and small position) placed in a reduction unit, and an internal gear formed integral with a lead cam. The reduction gear (large) is in mesh with the motor gear. The reduction gear (small) is in mesh with the intermediate gear (large). The intermediate gear (small) is in mesh with the lead cam internal gear. The rotational speed of the motor is reduced to 1/18 at the lead cam by the reduction gear.

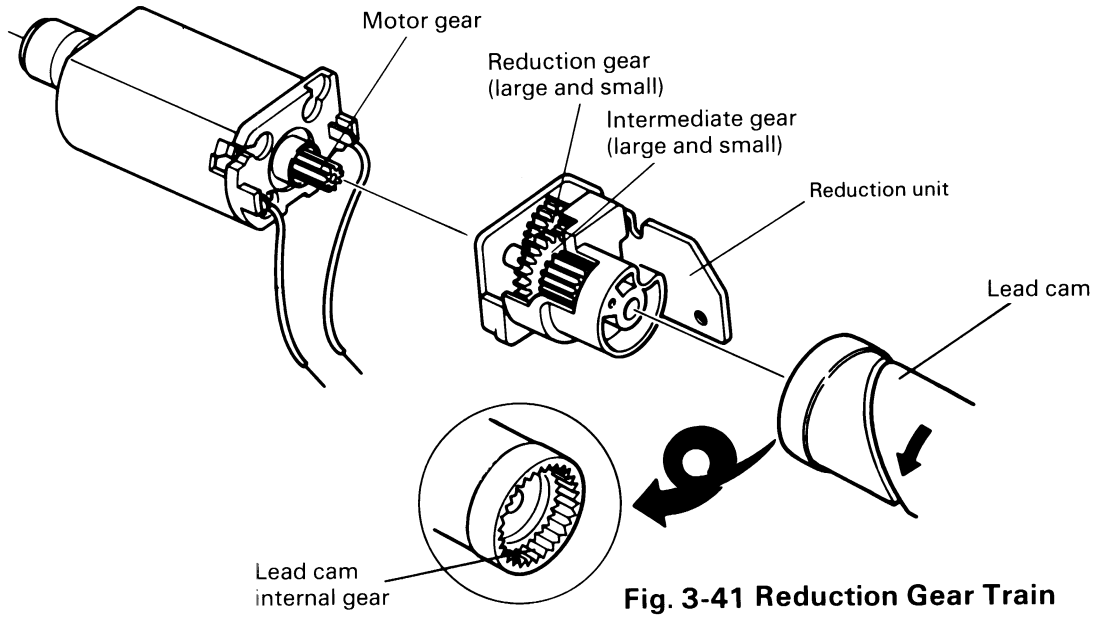


Fig. 3-41 Reduction Gear Train

(2) Ribbon Feeding Gear Train

The ribbon feeding gear train consists of a specially shaped ribbon feeding cam placed on a shaft, a ribbon feeding gear placed on a shaft on frame L side and consisting of a bevel gear portion and a small gear portion, and a spool gear placed on a shaft. These gears rotate in the directions shown by the respective arrows in Fig. 3-42. The reduction ratios are: ribbon feeding cam: ribbon feeding gear (bevel gear portion) = 9 : 1, and ribbon feeding gear (small gear portion): spool gear = 33 : 13. The ribbon is fed at a rate of 13.6 mm/sec.

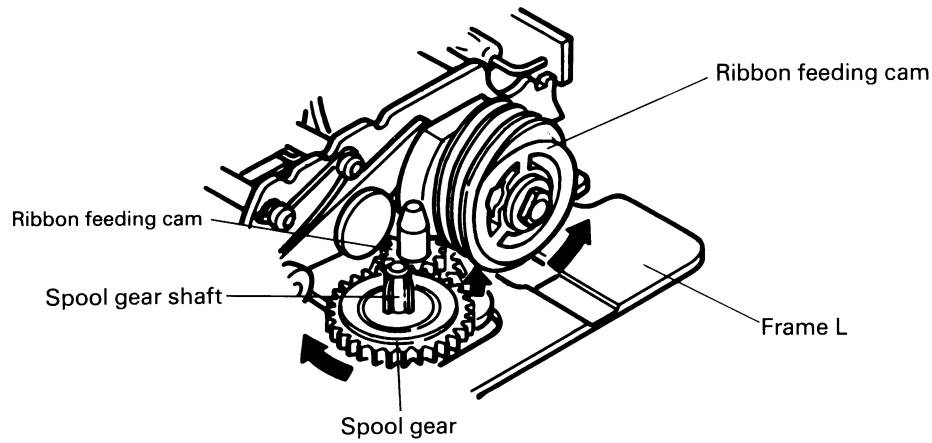


Fig. 3-42 Ribbon Feeding Gear Train

(3) Paper Feeding Gear Train

The Paper feeding gear train consists of a paper feeding transmission gear and a paper feeding gear both secured on a paper feeding roller shaft. The paper feeding gear is in engagement with a paper feeding lever, movements of the latter in directions A and B Fig. 3-43 causing the former to rotate in two directions. The paper feeding transmission gear enters into mesh with the paper feeding gear each time the latter rotates in direction C, and is made to rotate by one tooth in direction D.

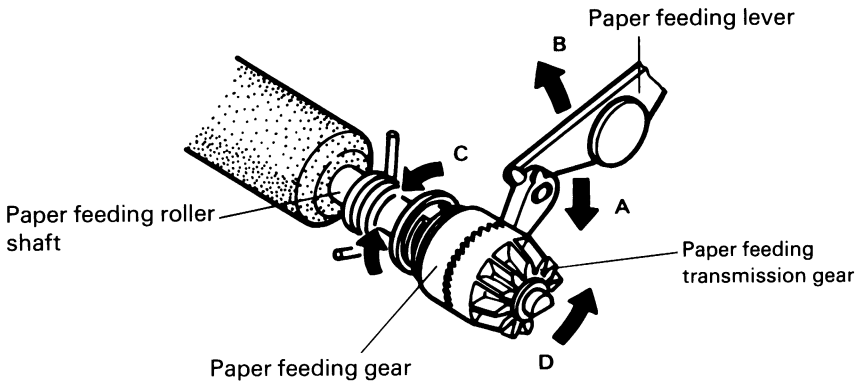


Fig. 3-43

3.4.3 Detecting Mechanism

The detecting mechanism of this printer consists of a timing detector and a resetting detector.

(1) Timing Detector

The timing detector is a tachogenerator coupled directly to the motor. It generates sinusoidal waves T_n (timing pulses: T_1 to T_{252} for each dot-line) of which the frequency is proportional to the motor speed.

(2) Resetting Detector

The resetting detector consists of a reed switch (normally open) and a permanent magnet fixed to the lead cam. It generates one pulse per dot-line. One reset pulse per print cycle is used for resetting the timing pulse counter.

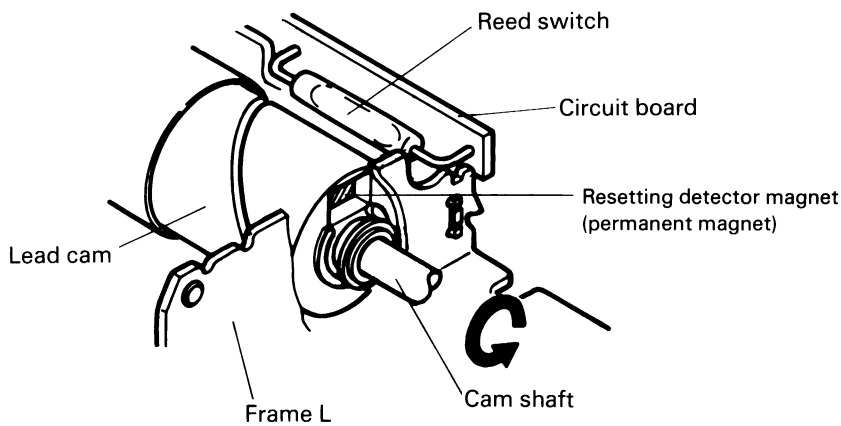


Fig. 3-44

3.4.4 Printing Mechanism

The printing mechanism has two functions: moving the print head, and printing.

(1) Moving the Print Head

As shown in Fig. 3-45, the print head is mounted on a carriage which smoothly moves reciprocatively between frames L and R along two print head guide shafts and in parallel with the platen.

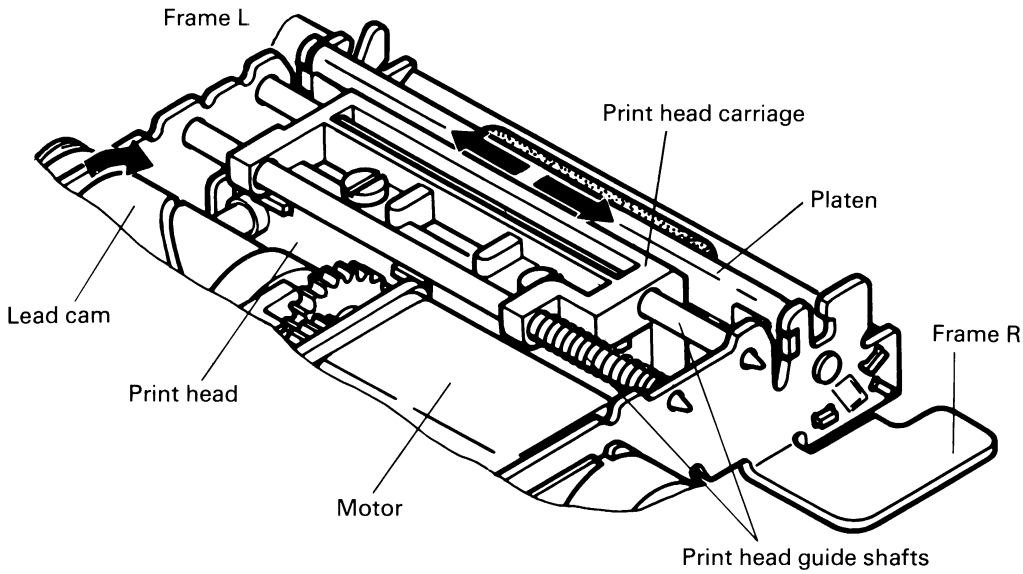


Fig. 3-45

Movements of the print head take place as follows:

① The lead cam has a groove (cam groove) formed as shown in Fig. 3-46 and a print head drive pin secured to one end of the print head is engaged in this cam groove. Rotation of the lead cam in direction A causes the print head drive pin to move along the cam groove and consequently the print head to reciprocate as shown by arrow B.

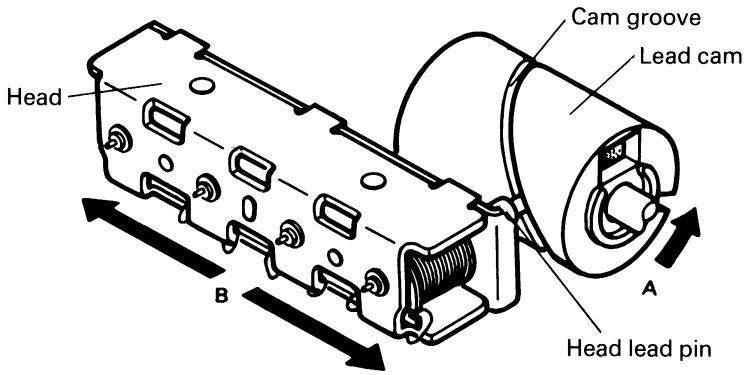


Fig. 3-46

② The print head is rigidly secured to the carriage by two screws and therefore they make reciprocative movement in just the same way.

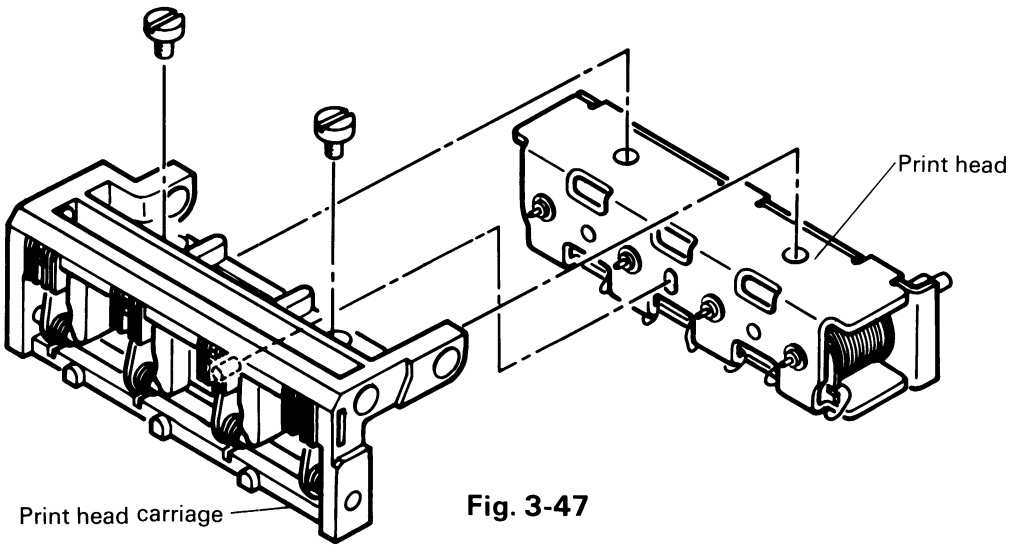


Fig. 3-47

(2) Printing Operation of Print Head

The print head contains four coil units, each of which consists of a core, a plunger and a push rod. In the print head carriage are provided four printing levers corresponding to the four coil units in the print head.

1) In printing a dot, the mechanism operates as follows:

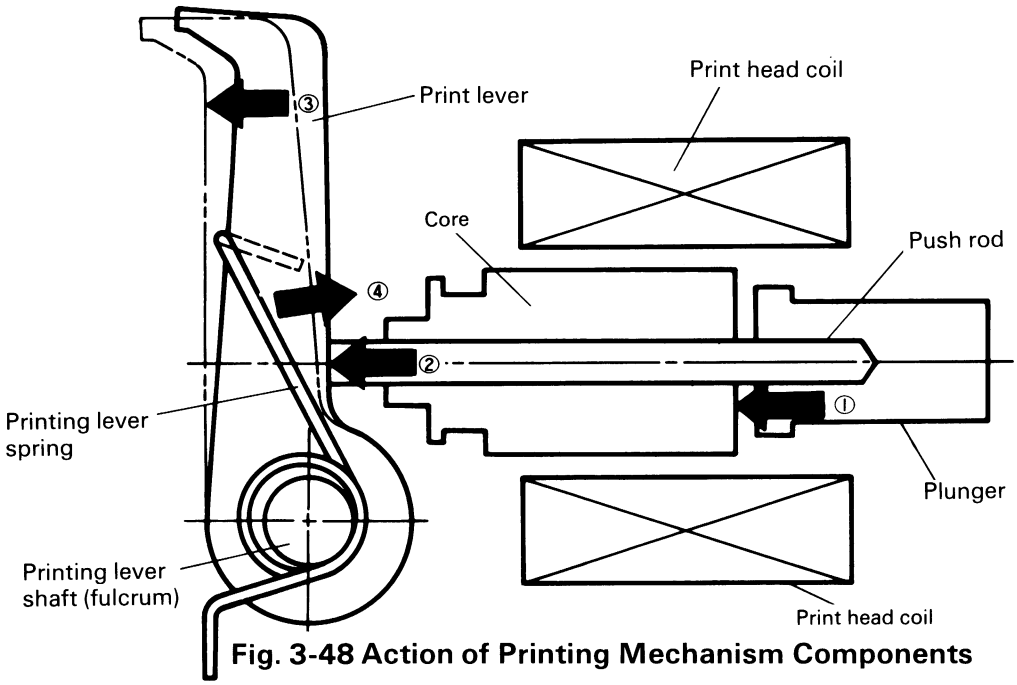


Fig. 3-48 Action of Printing Mechanism Components

① When the coil of a coil unit in the print head is energized, the associated plunger is attracted by the core (arrow ①). As the push rod is securedly fitted in the plunger, it is pushed by the plunger in the direction of arrow ② .

② The push rod then pushes the corresponding printing lever placed on a shaft (fulcrum) in the print head carriage in face of the platen, and consequently the lever is made to turn round the fulcrum in the direction of arrow ③ .

③ The printing lever thus pushed strikes the ribbon and paper against the platen to print a dot.

④ When the print head coil is deenergized, the printing lever is returned to home position by the action of spring (arrow ④).

2) In printing a dot-line, the print head operates as follows (with 5×7 dot-matrix):

① When the motor rotates, the tachogenerator directly coupled to it generates timing pulses of cycle time of approx. 0.6 msec (at 4.5V DC). Rotation of the motor also causes the lead cam to displace the print head approx. 0.33 mm in each 2.4 msec (at 4.5V DC).

How a dot-line is formed will be described referring to Figs. 3-49 and 3-50.

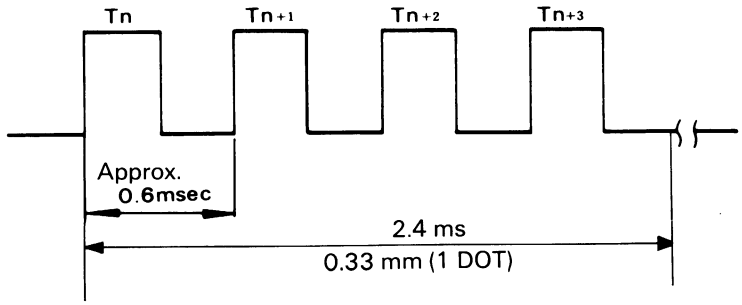


Fig. 3-49

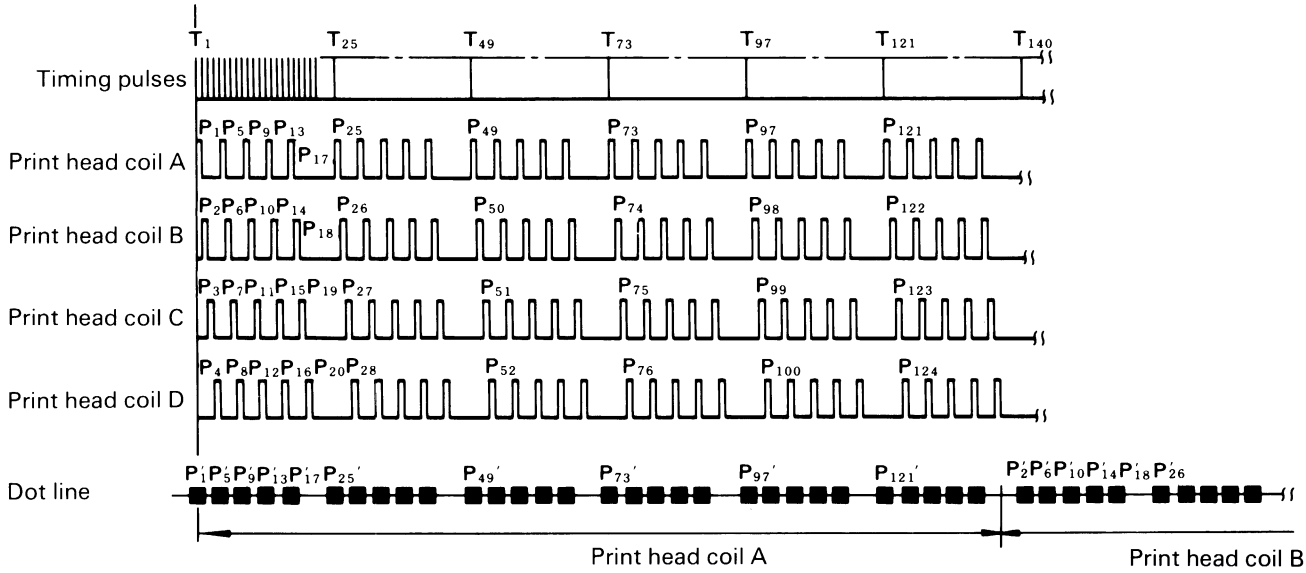


Fig. 3-50 Print Timing Chart

First, print head coil A is energized by print pulse P_1 to make dot P_1' be printed. Then print head coil B is energized by print pulse P_2 to print dot P_2'.

Coil C is then energized for dot P_3' and coil D for dot P_4', and then coil A for dot P_5 ..... Repetition of this cycle in necessary number makes a complete dot-line be printed. On completion of printing of a dot-line, the paper is fed 0.33 mm and the printing of the next line is ready to start.

3.4.5 Paper Feeding Mechanism

The paper feeding mechanism consisting of the components shown in Fig. 3-51 has normal paper feeding function and paper freeing function which permits drawing the paper out of the printer by pulling in the direction of feeding or the reverse direction. The arrows and encircled numbers in the figure below represent the directions of components' actions and the order in which the actions take place respectively.)

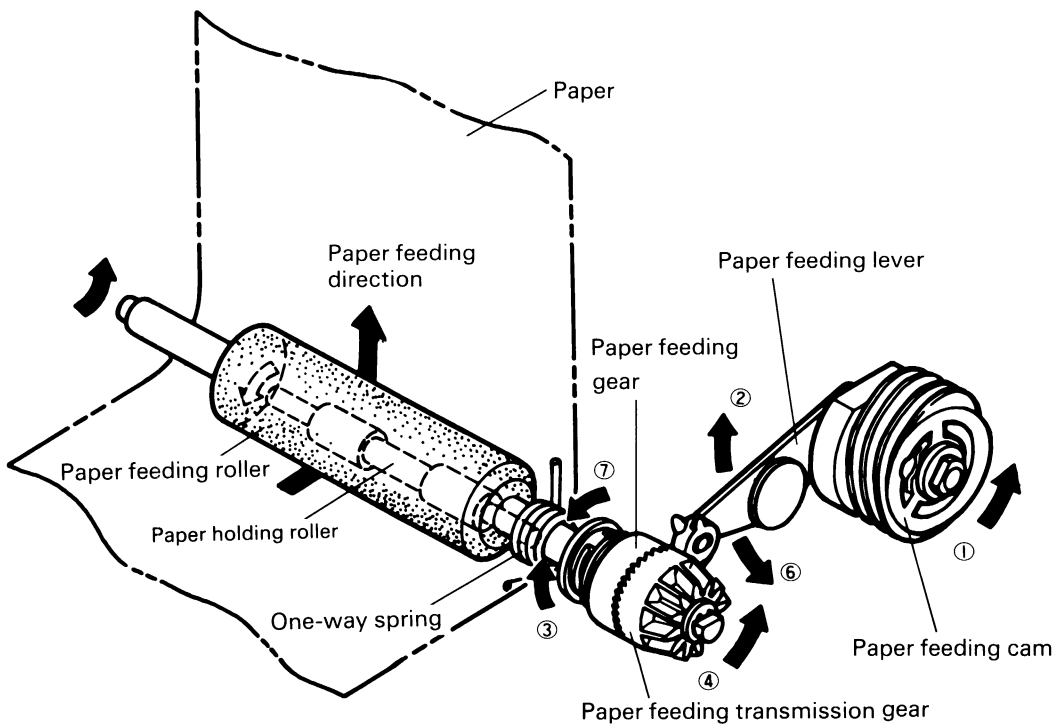


Fig. 3-51 Paper Feeding Mechanism

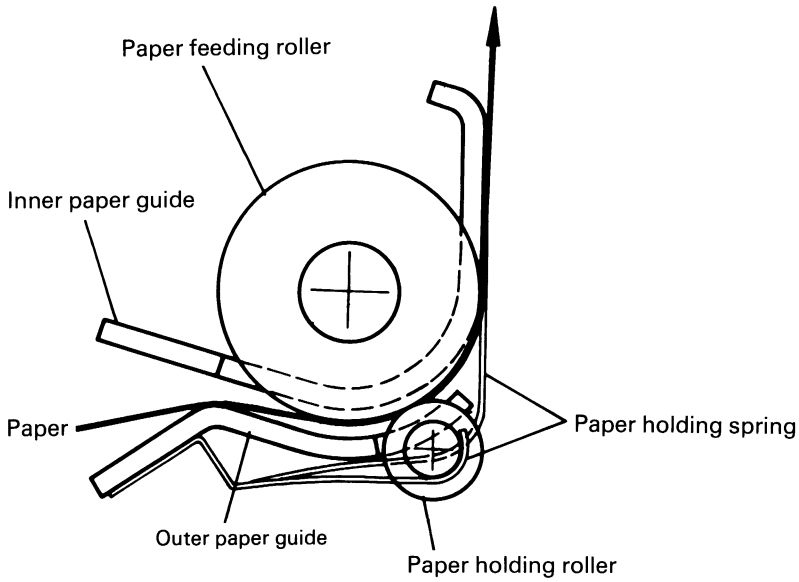


Fig. 3-52 Path of Printing Paper

(1) Operation of Paper Feeding Lever

A cam groove is formed internally of the ribbon feeding cam and the paper feeding lever is engaged in this internal cam groove at one end (A, Fig. 3-53). The paper feeding lever is thus moved round fulcrum C as the ribbon feeding cam rotates, and therefore the other end of the paper feeding lever shows a movement as shown by arrow B.

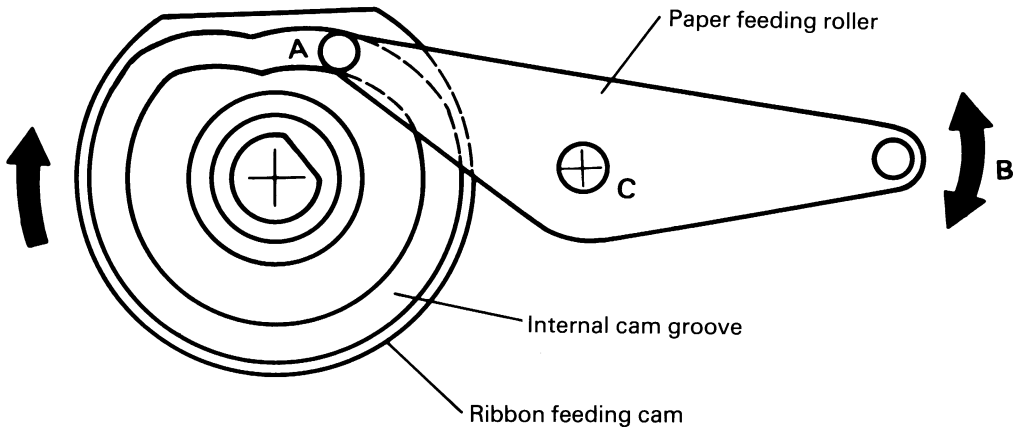


Fig. 3-53 Action of Paper Feeding Lever

(2) Operation of Paper Feeding Gear and Paper Feeding Transmission Gear

The paper feeding gear is driven in two directions alternately by the paper feeding lever, and the paper feeding transmission gear rotates intermittently by meshing with paper feeding gear only when the latter rotates in the predetermined one to the two directions.

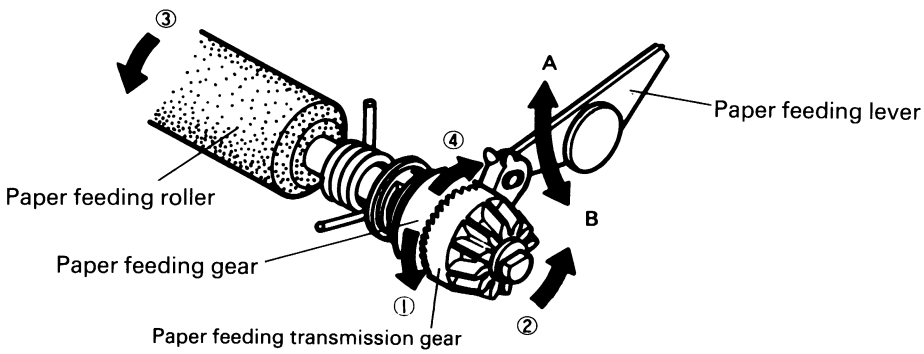


Fig. 3-54

① Paper feeding phase (refer to Fig. 3-54):

When the paper feeding lever moves in direction A, it rotates the paper feeding gear in direction ① and this gear enters into mesh with the paper feeding transmission gear, which is thus rotated one tooth in direction ② . Consequently, the paper feeding roller securedly placed on the same shaft as with the paper feeding transmission gear is rotated in direction ③ to feed the paper through a length of 0.33 mm.

② Return phase

Referring to Fig. 3-54, the paper feeding gear rotates in direction ④ when the paper feeding lever moves in direction Ⓑ. At this moment, the paper feeding transmission gear is prevented from rotating by the one-way spring placed on the paper feeding roller shaft and it goes out of mesh with the paper feeding gear (see Fig. 3-55).

Consequently the paper feeding gear alone rotates in the reverse direction and thus returns to the initial position.

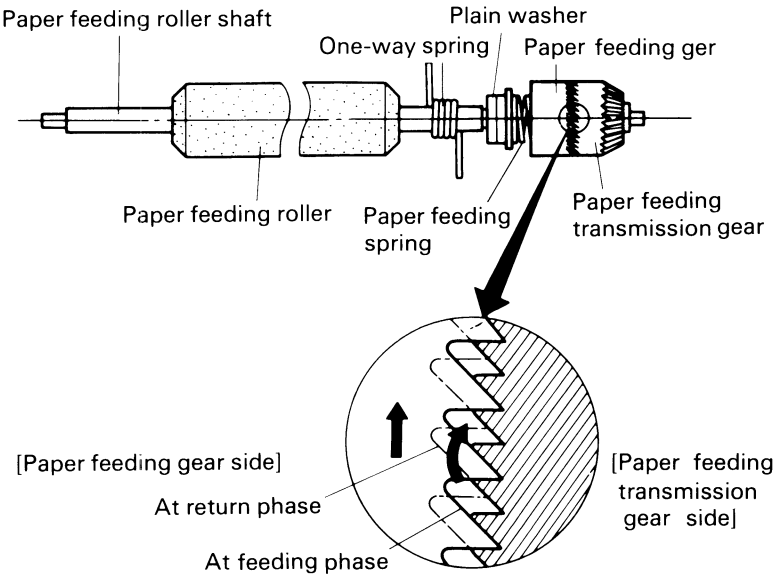


Fig. 3-55 Return Phase

3.4.6 Ribbon Feeding Mechanism

The ribbon feeding mechanism consists of the components shown in Fig. 3-56 (the arrows indicate the directions of the respective components' movements).

When the specially shaped ribbon feeding cam rotates in direction ① , the ribbon feeding gear in engagement with this cam and the spool gear rotate in direction ② and ③ , respectively. The rotation of the spool gear causes rotation of the spool gear shaft, which rotates only in the same direction as with the spool gear. The spool gear is in engagement with the ribbon feeding roller of the ribbon cassette, and therefore the ink roll securedly placed on the ribbon feeding roller rotates in direction ④ . The inked ribbon contained in the ribbon cassette is kept, by a holding spring, in contact with the ink roll under appropriate pressure over a part of its length, and therefore it can be frictionally driven (fed) in direction ⑤ . In the cassette is provided a brake spring for ensuring appropriate tension in the ribbon between points A and B.

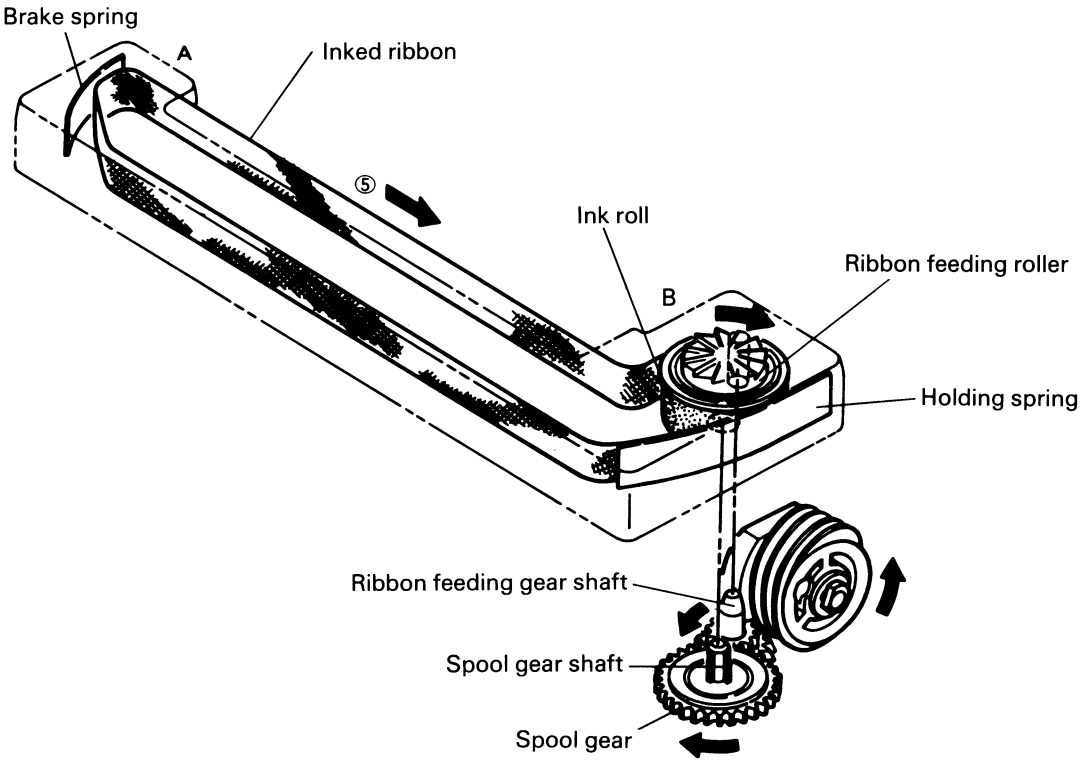


Fig. 3-56 Ribbon Feeding Mechanism

3.4.7 Printing Operation One Print Cycle

Fig. 3-57 and Fig. 3-58 show the timing chart of the pulse signals to perform a printing cycle.

(1) Printing and paper feeding

First, print solenoid A is energized by pulse P_1 lasting from T_1 to T_2 to print the top left dot for the character to be printed in No. 24 column. Then, print solenoid B is energized by pulse P_2 lasting from T_2 to T_3 to print the top left dot for the character to be printed in No. 18 column. Such operation is repeated, and print solenoid D is energized by pulse P_{140} lasting from T_{140} to T_{141} to print the top right dot for the character to be printed in No. 1 column.

After printing in the rightmost columns (Nos. 19, 13, 7 and 1 columns) to be covered by the respective solenoids, the print head is moved for another dot space and then returned to the home position while timing pulses T_{144} to T_{252} pass. At the same time, the paper is automatically fed one dot-line. The above operation is repeated continuously for seven dot-lines. Then printing in the seventh dot-line starts. After print solenoid D has been energized by pulse P_{1652} lasting from T_{1652} to T_{1653} to print the right lowermost dot desired for the character to be printed in No. 1 column for completing the 5×7 matrix character in No. 1 column.

Next, the paper is fed three dot-lines (eighth, ninth, and tenth dot-lines) to provide a character line spacing equivalent to three dot-spaces, and one print cycle ends at T_{2520}.

(2) Designation of reset pulses R_1 and R

The first reset pulse appearing after 95 timing pulses have been counted since application of motor drive signal is designated as R_1. The reset pulses to come first after another 95 timing pulses are designated as $R_2 - R_n$.

Initial setting for ascertaining that the printing head is in home position is automatically finished with detection of R_1. Timing pulse T_1 to indicate the line start position for each print cycle is determined through detection of R_1.

(3) Continuous printing or continuous paper feeding

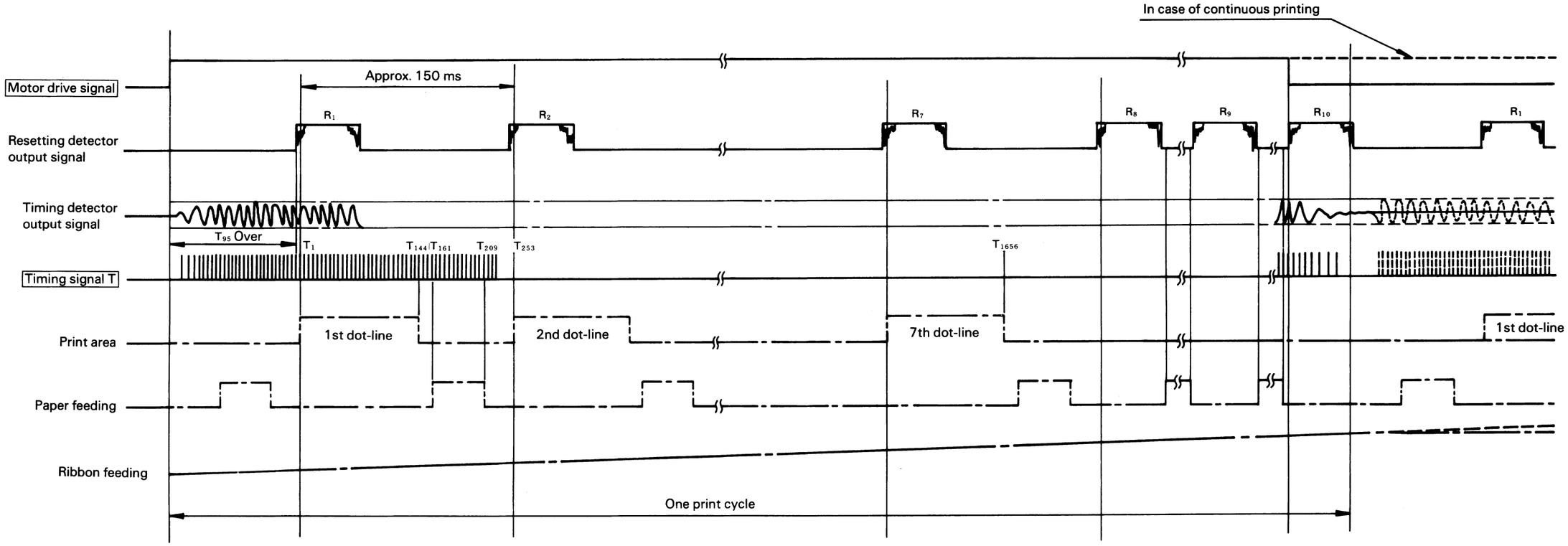
This can be performed by continuing application of motor drive signal for the desired period.

(4) Reset signal

It may occur that no reset pulse is generated when the print head is in halted state.

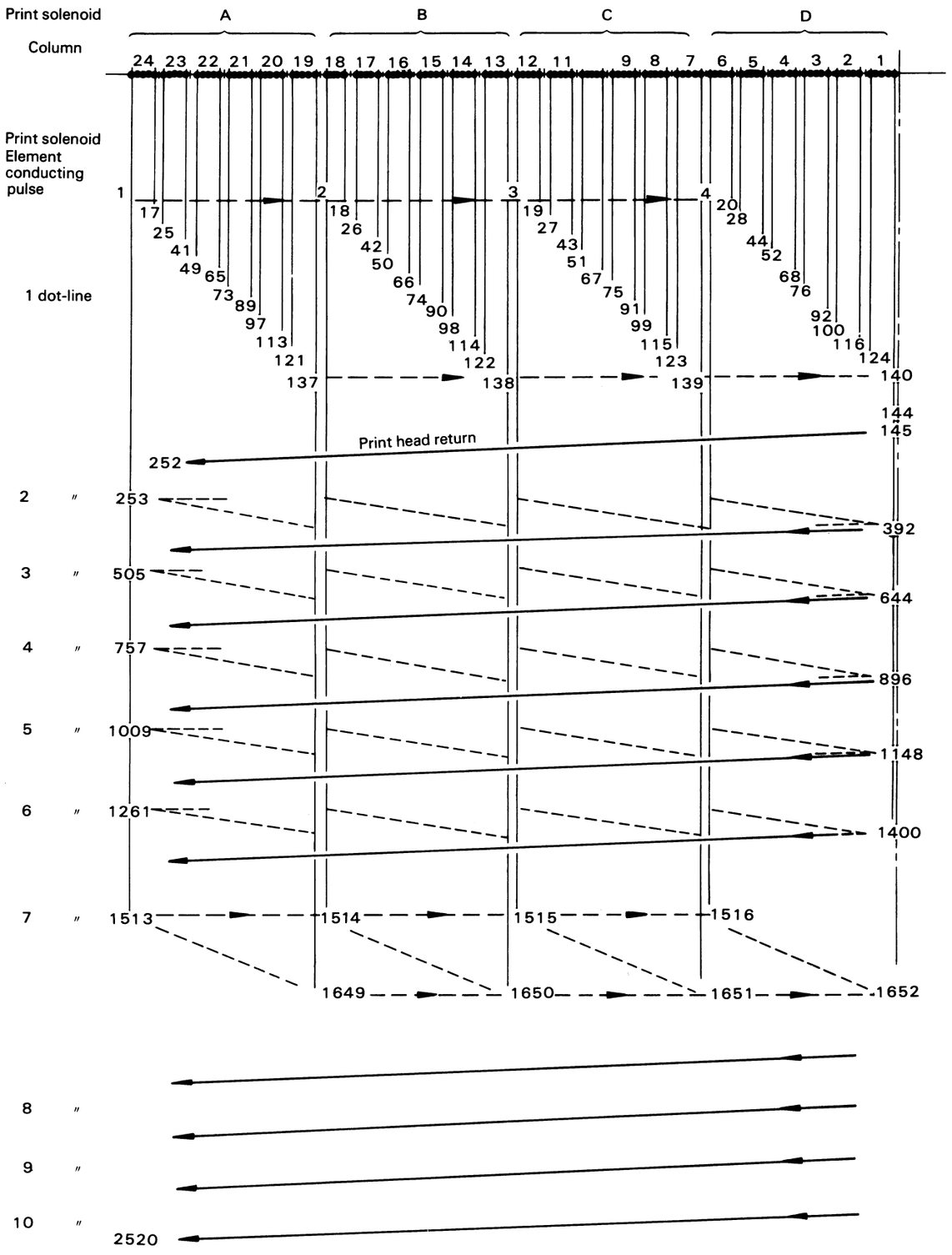
Notes:

1. 95 or more timing pulses appear during the period from the start of motor to appearance of R_1.
2. Periods when print solenoids must not be energized:
   1) From start of motor to rise of R_1 (from the moment when the motor starts to the moment when it attains normal speed).
   2) From $T_{145} + {}_{252n}$ to $T_{252} + {}_{252n}$ (during return of printing head) (n = one of the integers from 1 to 10 in case of printing with 5×7 dot-matrix and line spacing equivalent to three dot-spaces).
   3) The print solenoids must not be energized nor deenergized by noise.
   4) Ascertain the generation of R_1 for each print cycle and count timing pulses anew for each print cycle.



Timing chart for printing with 5×7 dot-matrix and line spacing equivalent to three dot spaces: The pulses enclosed in ▭ are to be provided by the customer.

Fig. 3-57



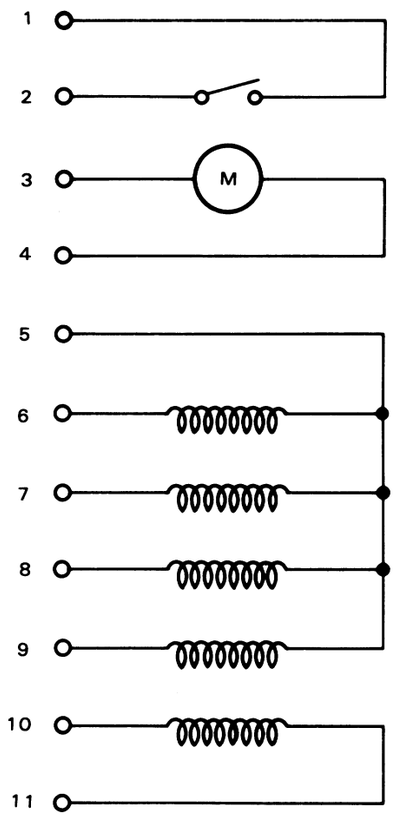
NOTE: $P_n = T_n - T_{n+1}$ (P_n: Print solenoid element conducting pulse
T_n: Timing pulse)

Timing pulse assignment (for printing with 5×7 dot-matrix and line spacing equivalent to three dot spaces)

Fig. 3-58

3.4.8 Terminal Contacts Arrangement

Connection	CN9 pin numbers on MOSU P.C. board
Resetting detector	1, 2
Resetting detector	3, 4
Motor (–)	5, 6
Motor (+)	7, 8
Common, Print solenoid	9, 10
Print solenoid (D)	11, 12
Print solenoid (C)	13, 14
Print solenoid (B)	15, 16
Print solenoid (A)	17, 18
Timing detector	19
Terminal Nos.	20



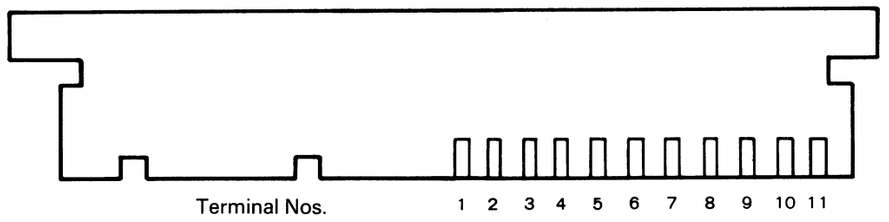


Fig. 3-59

3.4.9 Control Circuit

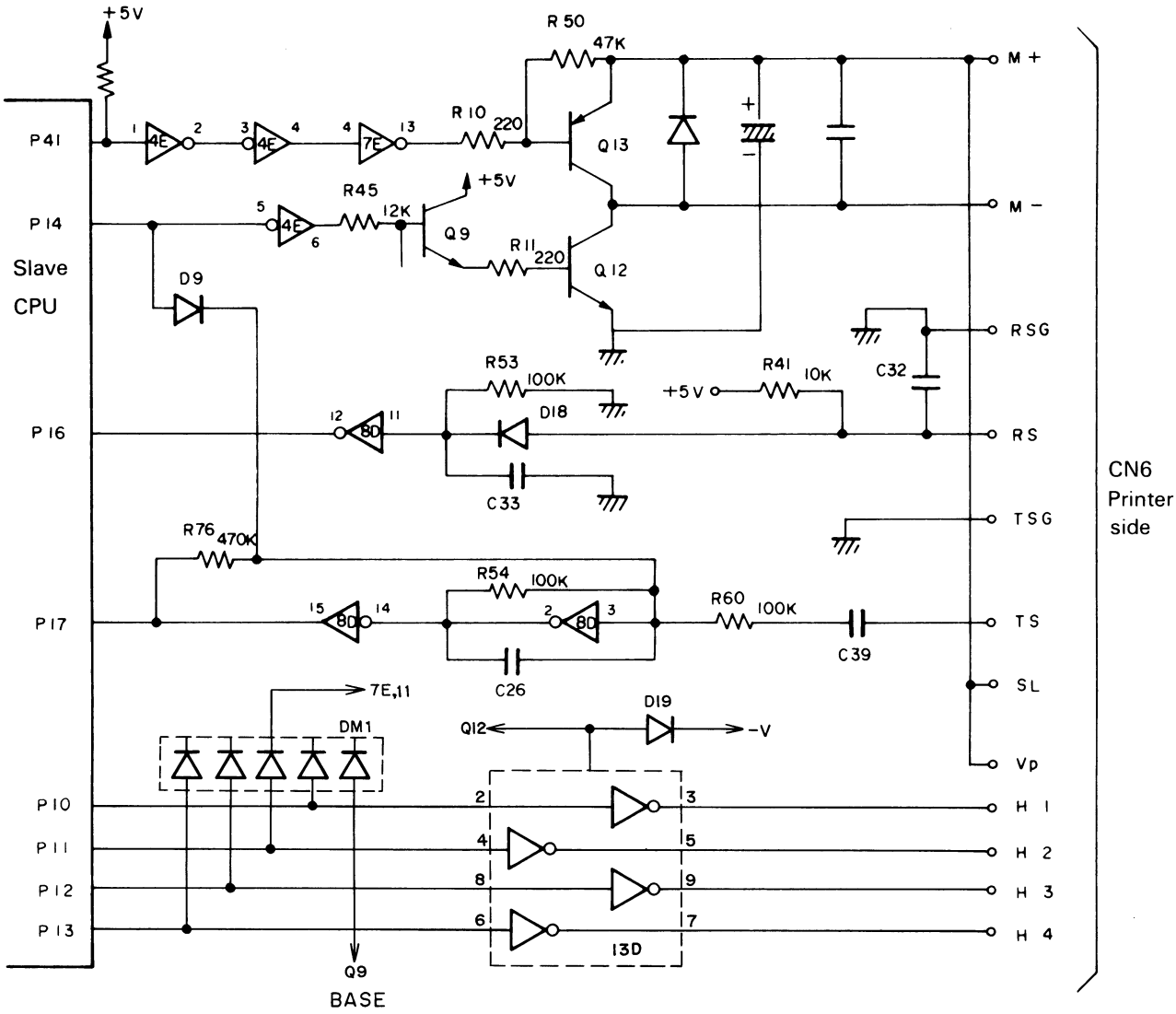


Fig. 3-60

3.4.10 Printing Start

Before operating the microprinting, make sure that P41 is at low level, and then set P14 to low level. As a result, transistors Q9 and Q12 are turned on, M- goes to ground level, and the +5V is routed from M+ to M− (GND) via the motor coils to feed a current and turn the motor.

When the printer motor runs, the tachogenerator which is directly coupled to the motor generates a TS (timing signal) about every 0.6 msec. The TS signal is received by the slave CPU 6301 at P17, which counts it and waits for a reset signal (RS) from the printer.

If an RS signal comes from the printer before the TS signal count reaches 95, the RS signal is ignored, and the printer keeps running the motor until the next RS signal comes.

When an RS signal is received after the TS signal count is 95 or more, the printer starts printing.

(This process is intended for withholding printing until the carriage can move at constant speed because, if characters are printed while the head carriage is unsteady in operating speed, printed dots come out uneven in density. The head carriage becomes steady in operating speed by the time the TS signal count is 95.)

3.4.11 Print Timing

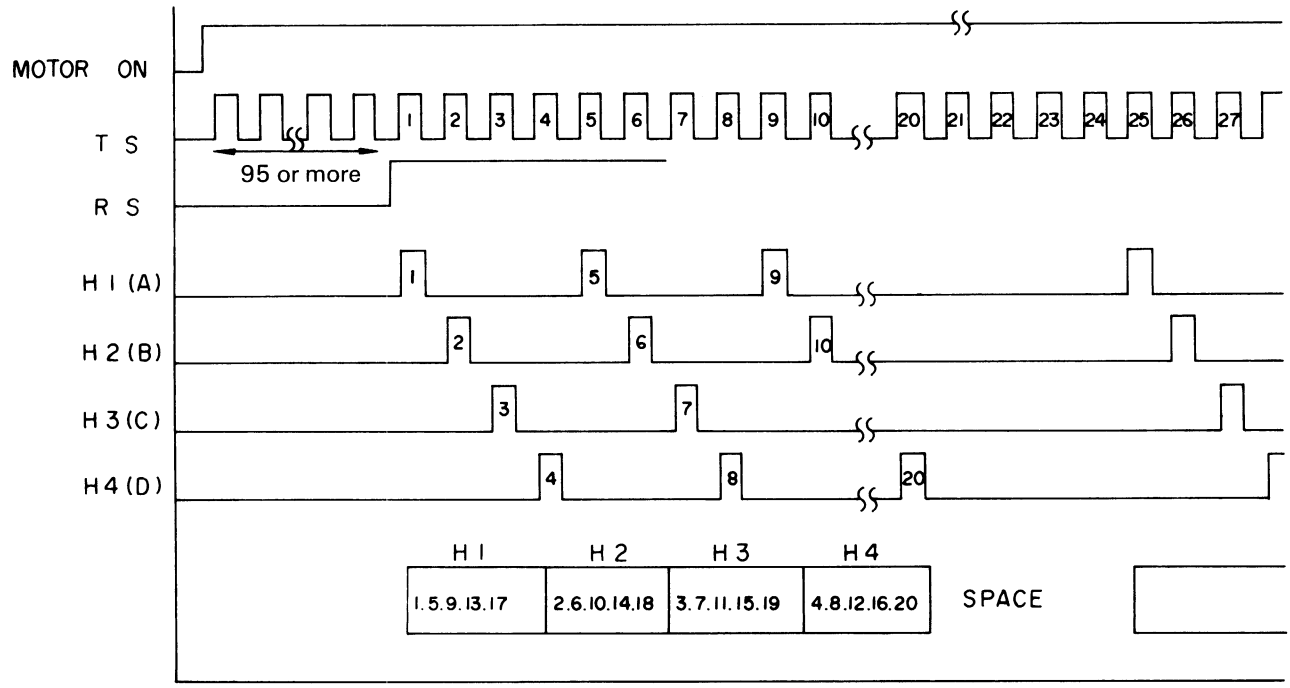


Fig. 3-61

3.4.12 Heads and Printing Positions

The dot heads are slightly out of line with printing start positions (indicated by arrows below). Two or more dot heads do not print simultaneously.

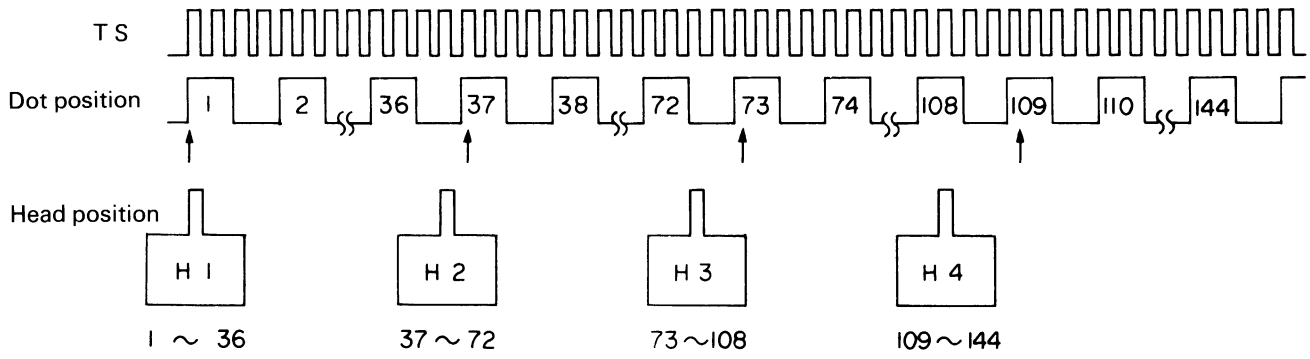


Fig. 3-62

The printer has 4 printing heads, whose physical positions are as shown in Fig. 3-73. Specifically, H2 1 TS left of the printing start position; H3, 2 TSs left of it; and H4, 3 TSs left of it. Thus, only one of the printing heads H1 to H4 can operate against one TS so a plurality of printing heads cannot simultaneously operate.

As shown in the print timing example, a reset signal (RS) represents a printing start. Thus, the TS which is output immediately after RS is on signifies the print timing of each head. TS No. 1 in the timing chart is for H1; TS No. 2 for H2; TS No. 3 for H3; and TS No. 4 for H4. One dot line (a total of 144 dot positions) is printed by repeating this operation 36 times.

A character has 7 dots in the vertical direction so, if the above operation is repeated 7 times (144 x 7 = 1008 dot positions) and the paper is line-spaced 1 dot, 24 characters are printed in a line.

3.4.13 Example of Printing

Examples of printing are shown below.

1st to 6th columns (H1): Letter A

7th to 12th columns (H2): Letter E

13th to 18th columns (H3): Numeral 8

19th to 24th columns (H4): Letter H

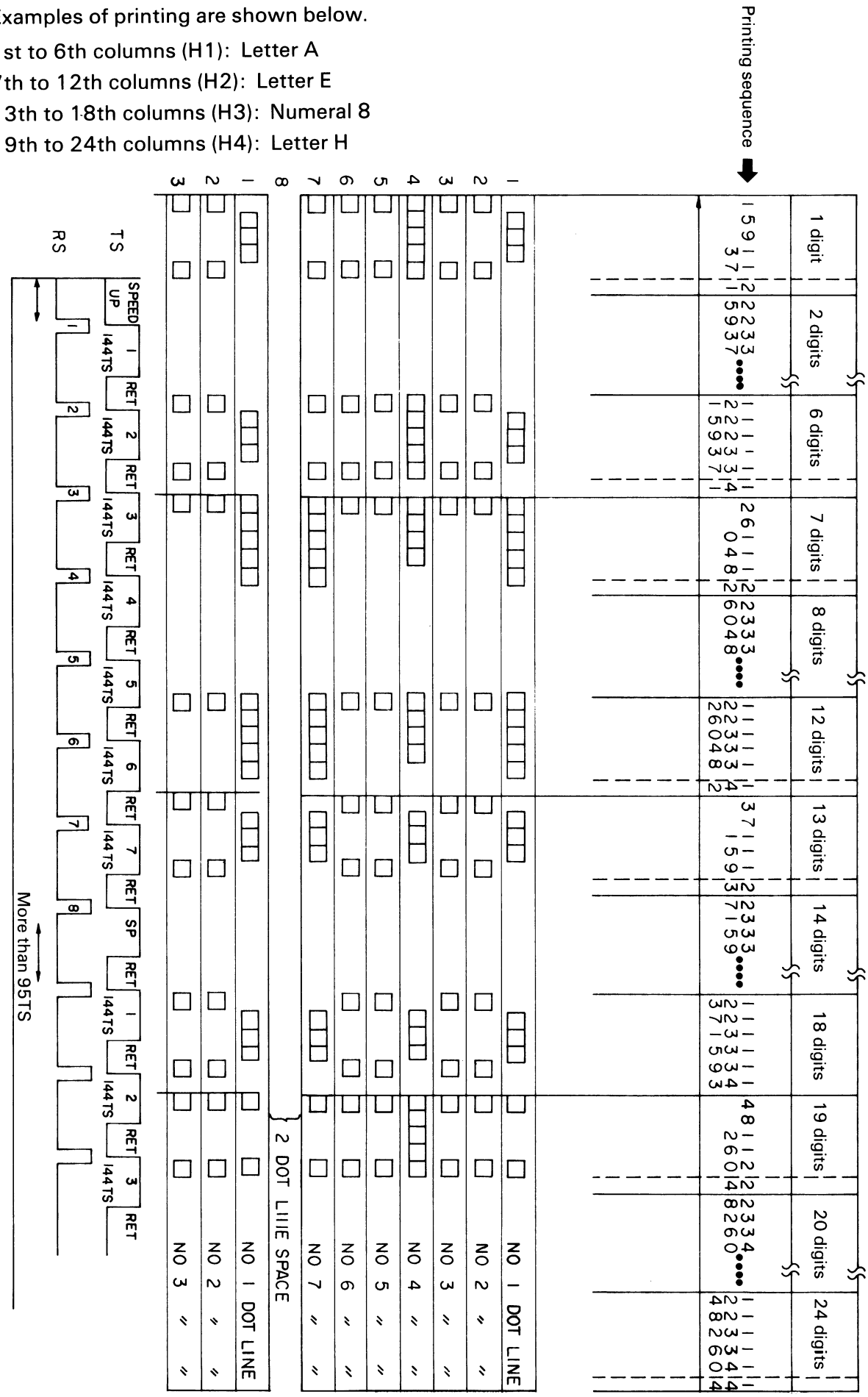


Fig. 3-63

3.4.14 Character Generators

Printed characters are composed of dot matrixes, and dot patterns are generated from character codes (ASCII codes).

For this purpose, character generators are built into external ROMS 11E and 12E.

Each text character consists of 5×7 dots, and 8 bytes (7 bytes for a character and 1 byte for a line space) are used to compose a single character font.

Example: Letter H

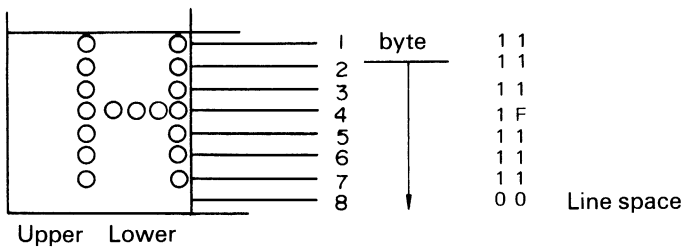


Fig. 3-64

An example of character font is shown below. It is normally composed of 5 x 7 dots.

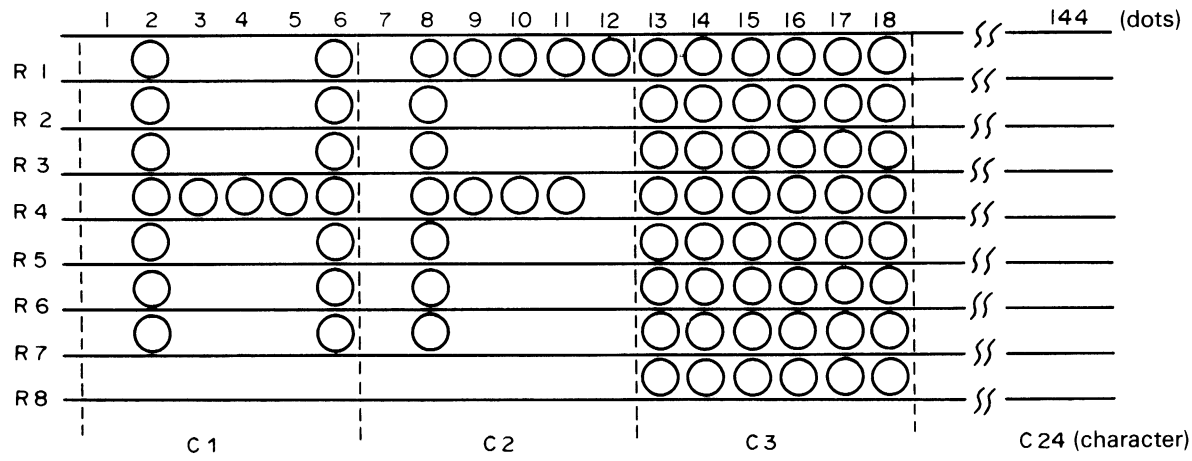


Fig. 3-65

The printer prints each dot line (low line) which has 144 dot positions. By repeating this dot printing 7 times (for text characters) or 8 times (for graphics) (R1 to R8) the printer prints a line of characters.

Printing data can be transferred or stored in units of bytes, but the upper 2 bits are ignored because the printer uses only 6 bits (for 6 columns).

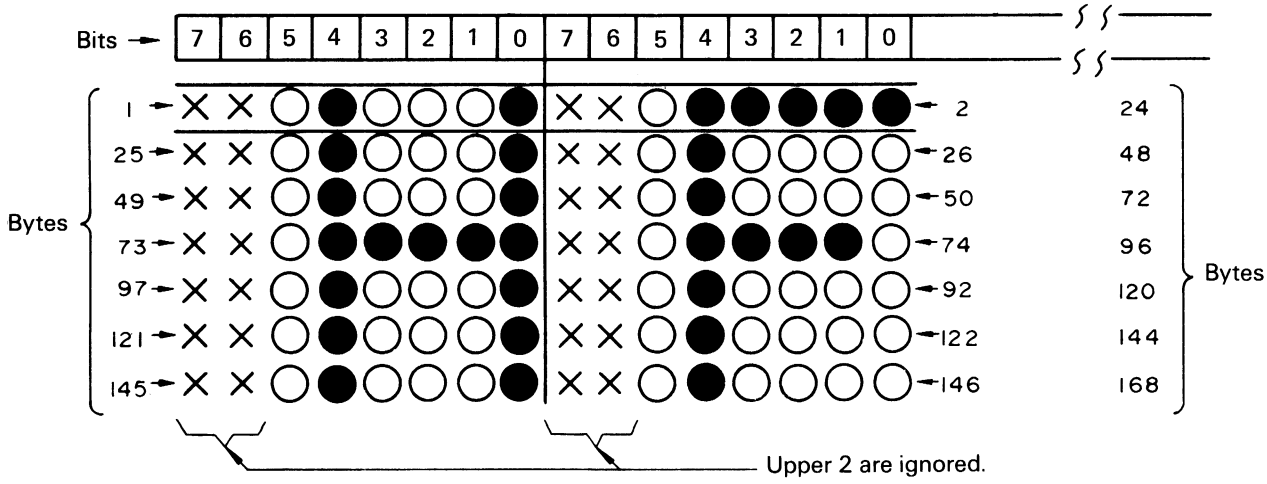


Fig. 3-66

3.4.15 Printing Process

Printing data tarnsfer to the printer is performed in the following order.

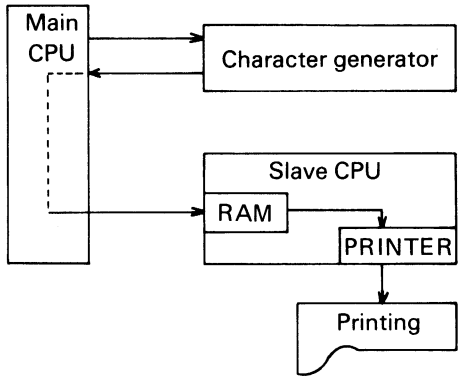


Fig. 3-67

(1) A line of printing data is read and stored. (24 characters) (Main CPU)

(2) A print command is sent to the slave CPU. (The slave mode is selected.)

- The printer motor is turned on. (Slave CPU)

(3) A font of 1 dot line is generated by the character generator, and sent to the slave CPU. (144 dots)

- The data is stored in the RAM, and waits for printing start timing. (An RS signal after TS count of 95 or more)

(Slave CPU)

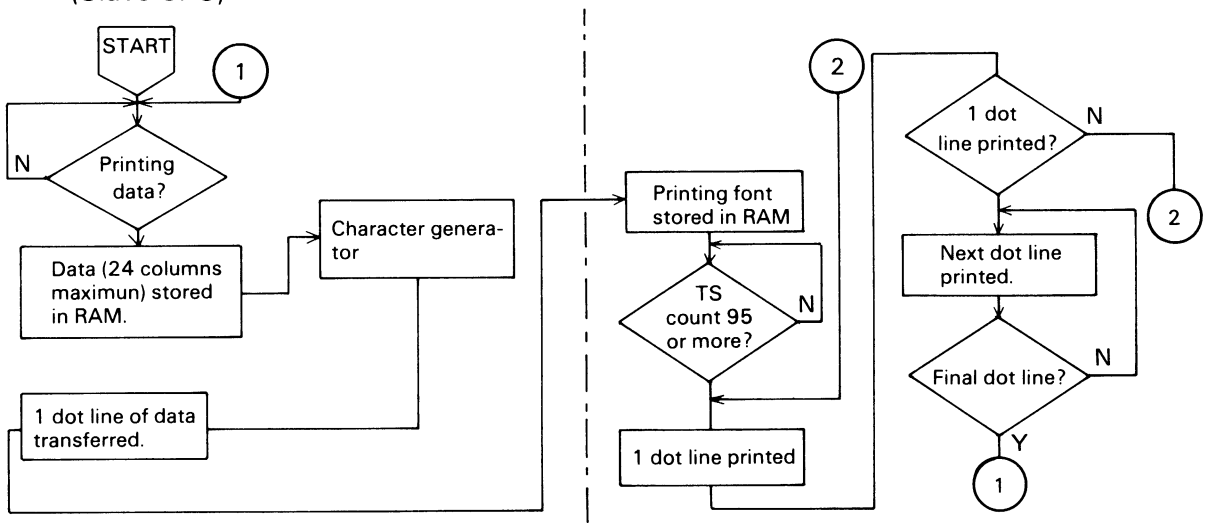


Fig. 3-68

3.4.16 Printing End

The RS signal that follows the printing of the final dot line of printing data (7 dot lines) effects a character reset, and a request is sent to the control program (stored in a 4k mask ROM) of the slave CPU 6301 for the next data transfer.

If there is no more printing data, the head carriage moves one way and back to line space the paper by 1 dot line, and the printing operation is brought to an end in the following sequence.

(1) P14 of the slave CPU 6301 goes high to turn off transistors Q9 and Q12, thus turning motor power off.

(2) P41 goes high to turn on Q13, by which the counterelectromotive force generated by the moment of inertia of the motor is utilized to brake the motor and thus stop it in the shortest distance.

3.5 Liquid Crystal Display

The liquid crystal panel (LCD) has a 20 x 32 dot matrix and each character consists of 5 x 7 dots. It can display 20 characters per line, up a maximum of 80 characters on the screen. The LCD features lightweight, thin design, and low power consumption so it is an ideal display unit for the HX-20.

3.5.1 Hardware Composition

(1) The liquid crystal display (LCD) unit consists of an LCD panel, 6 control ICs, and a voltage dividing circuit. All the component elements except the view angle control element are mounted on a single substrate. Signals are supplied from the MOSU circuit board via the keyboard.

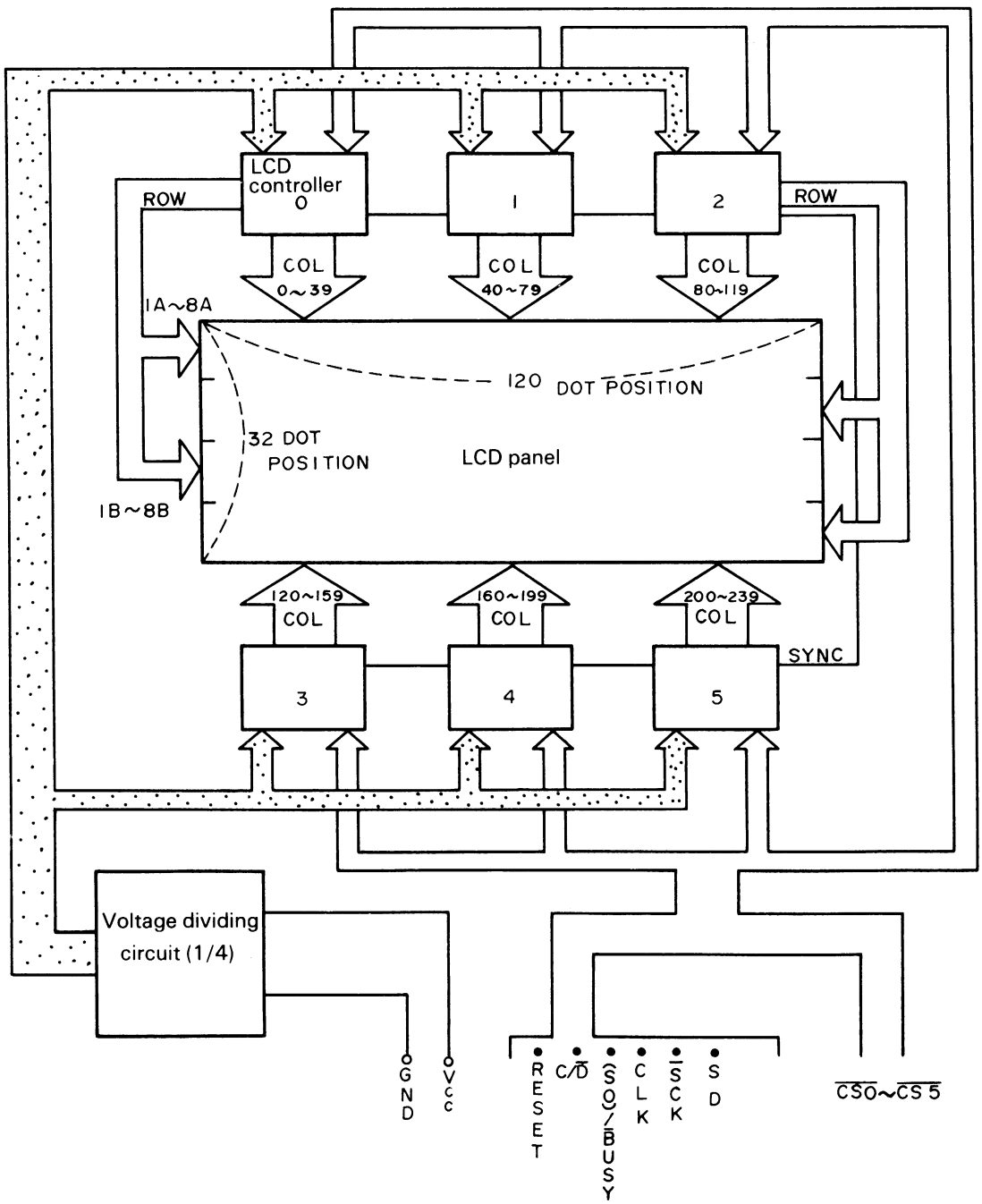


Fig. 3-69 Block Diagram

(2) The LCD unit has one panel, 6 control ICs (μPD 7227s), 7 resistors, and 5 capacitors, and their locations and the arrangement of the pins are as shown below.

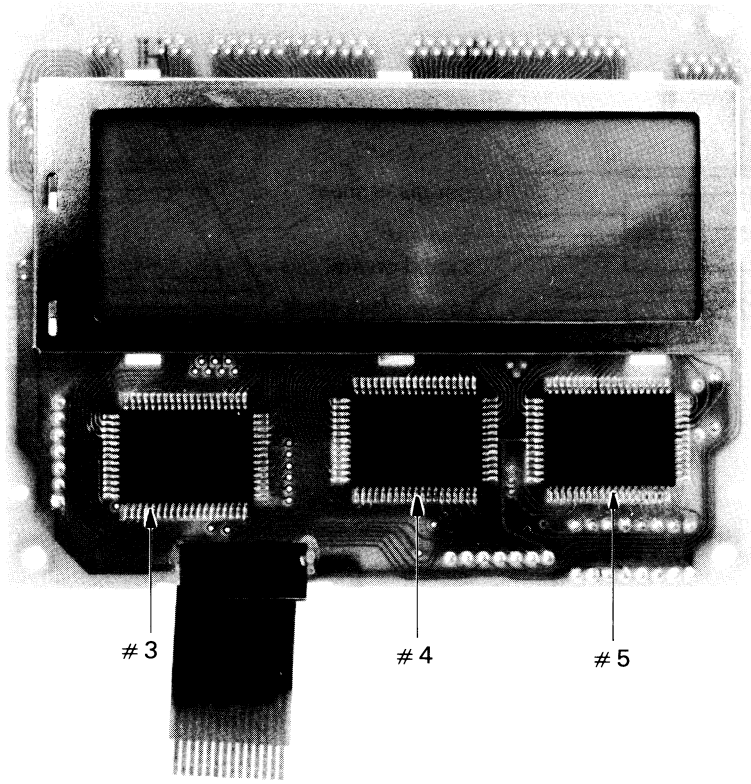


Fig. 3-70

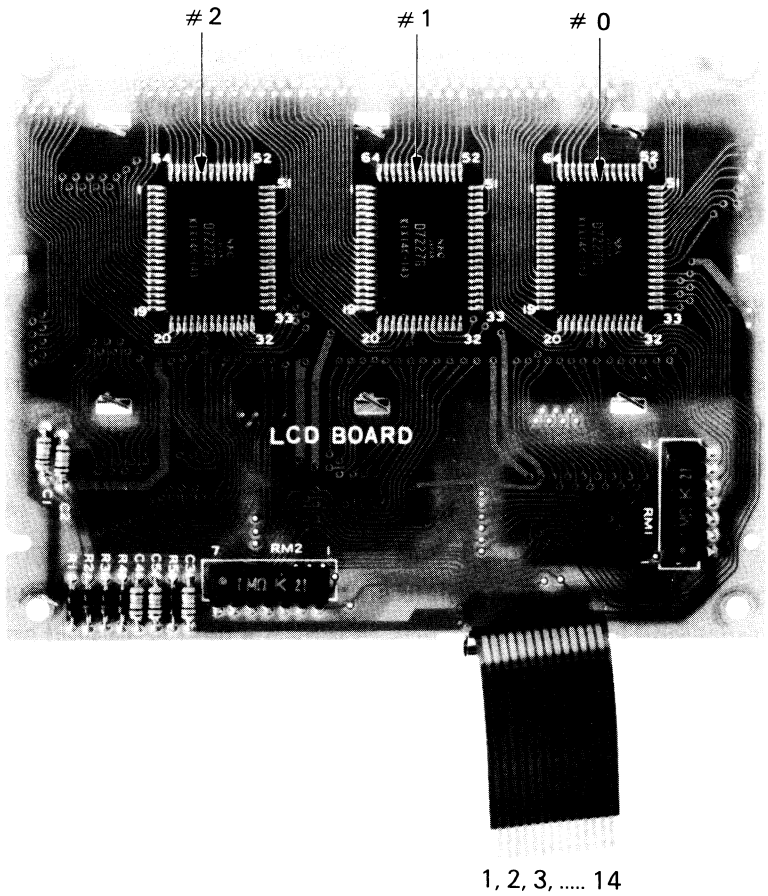


Fig. 3-71

3.5.2 LCD Panel

The HX-20 employs a liquid crystal display of the twisted nematic type (TNM), a kind of voltage effect type, whose structure is as illustrated below.

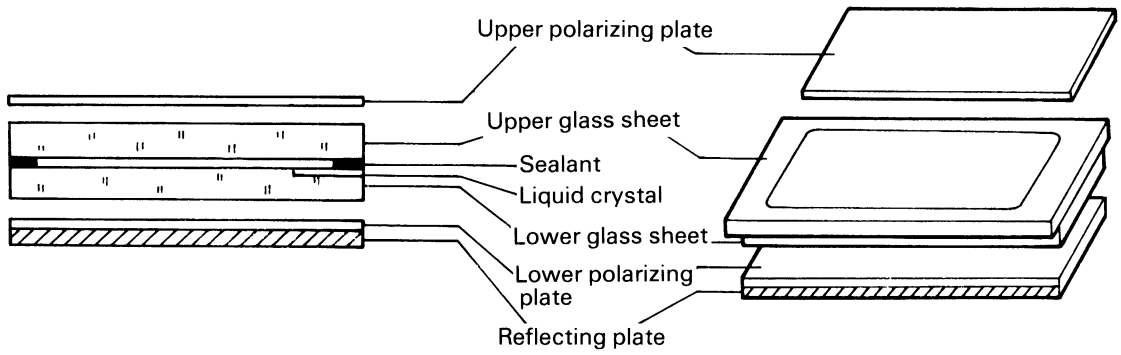


Fig. 3-72

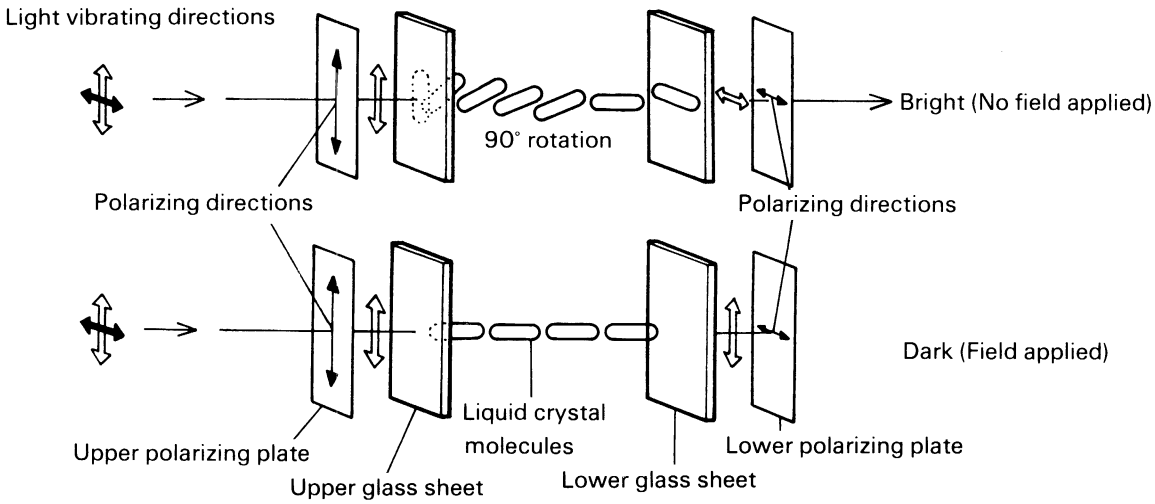


Fig. 3-73

3.5.3 Theory of Operation of LCD Panel

As light reaches the liquid crystal display, only that part of it which vibrates in a single direction passes the upper polarizing plate. If no field is applied to the liquid crystal layer, this light component rotates 90° in its vibrating direction as it passes the layer of liquid crystals arranged in a twisted way between the upper and lower glass sheets. As a result, the vibrating direction meets the polarizing direction of the lower polarizing plate to let the light pass the lower polarizing plate.

If a field is applied to the liquid crystal layer, the light does not rotate in the liquid crystal layer, and the light that has passed the liquid crystal layer vibrates at right angles to the polarizing direction of the lower polarizing plate so that the light is interrupted. It is in this way that a contrast is generated between the parts to which a field is applied and the other parts.

- Liquid crystal reacts to the difference of temperature, so, the HX-20 carries out temperature compensation with the view angle volume, but it does not work correctly under the conditions below.
  1) More than +70°C: Liquide crystal will turn fluid with the black display.
  2) Less than −40°C: Liquid crystal is solidified with no contrast generated on the display.

  However, the liquid crystal mentioned in 1) and 2) will resume its function when the temperature returns normal.

3.5.4 Display Control

Each control IC μPD 7227 has two data memories (banks O and 1), and each memory has a capacity of 40 x 8 bits. Each control IC controls 40 columns. The No. 0 μPD 7227 controls the first and second rows; the No. 2, the third and fourth rows; and the data stored in the memories are read out every row and every line to display on the panel.

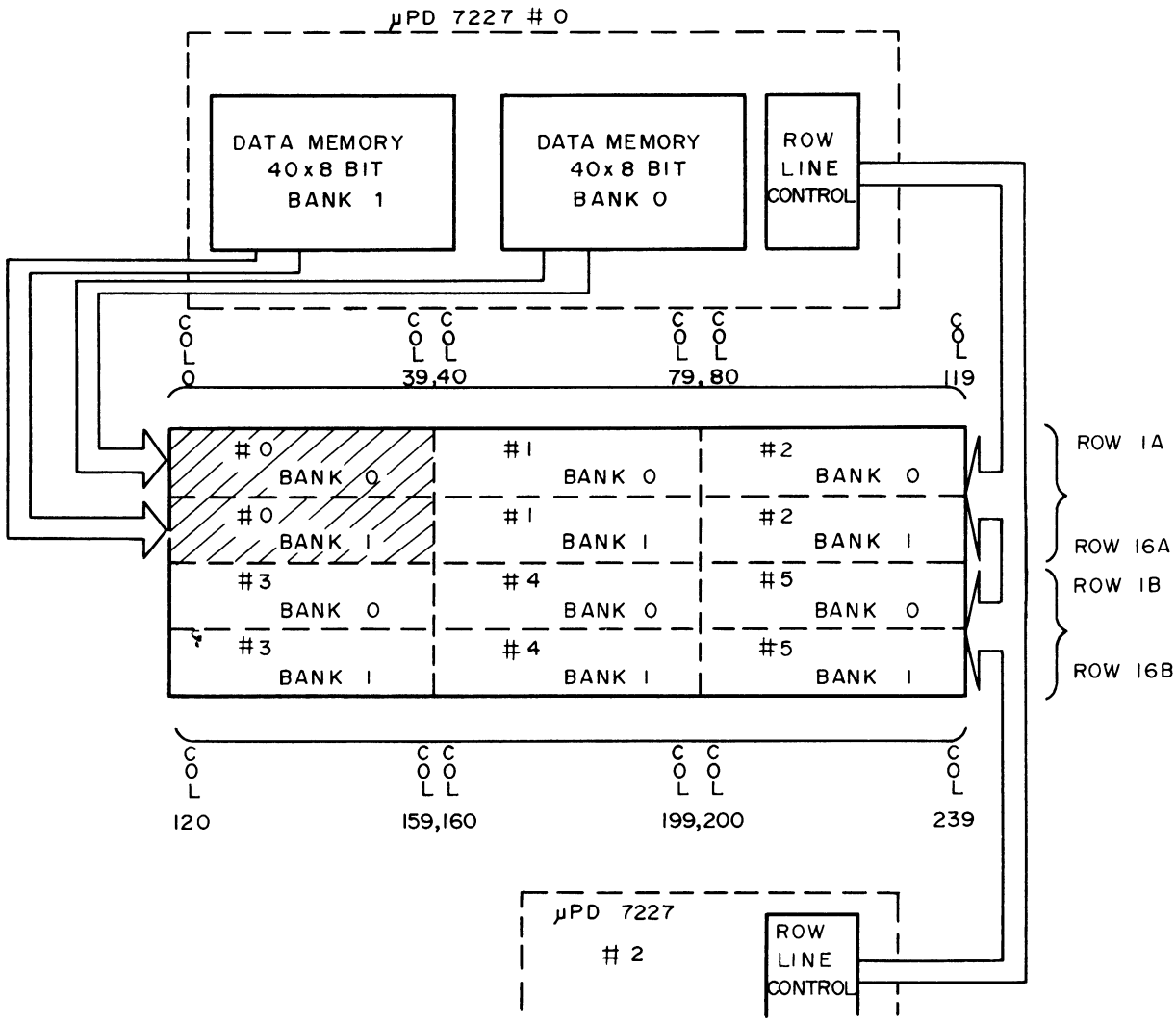


Fig. 3-74

3.5.5 Display Initializing

A reset signal is sent from the reset circuit on the MOSU circuit board after power is turnd on to initialize the LCD control ICs (μPD 7227s). Then, the program sends the following setting commands.

(1) SFF (Set Frame Frequency): The clock input to the CLOCK terminal is divided to the ratio specified by the command to determine internal control timing.

(2) SMM (Set Multiplexing Mode): This command designates a two driver function, time division number, memory banks, SYNC terminal input/output operations, and thus determines a display method.

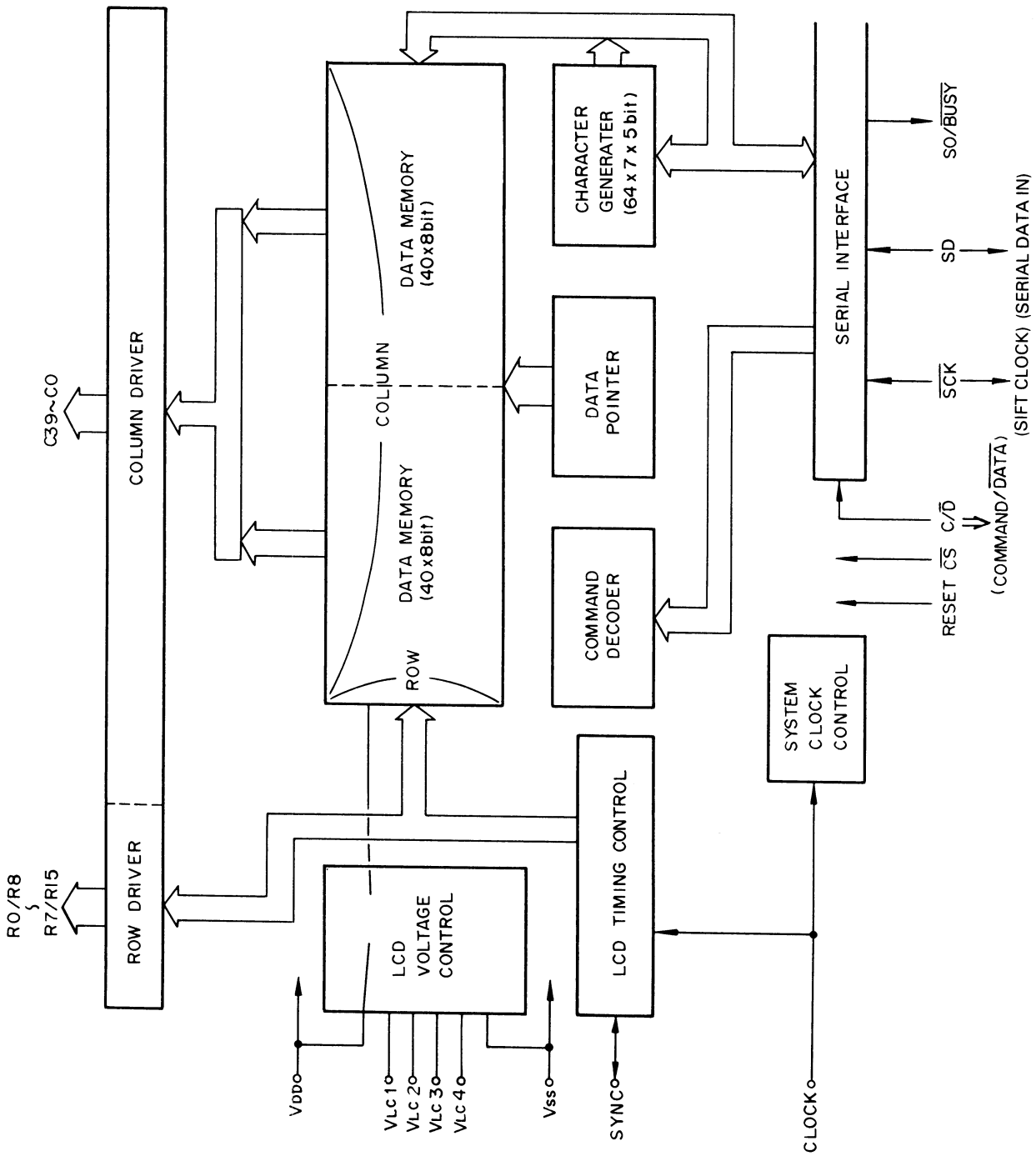


Fig. 3-75

(3) DISP ON (Display On): This command sets the LCD in a state of waiting for display data.

3.5.6 Display Data Transfer

The character generators in the ICs μPD 7227s are not used for generating display data. It is necessary, therefore, to write the dot patterns (display data) generated by the character generators in the ROMs on the MOSU circuit board into the data memories in the ICs μPD 7227s. Before each transmission of display data, the command SWM (Set Write Mode) must be prefixed to the data. Shown below is an example of display data transfer where a single character is transmitted.

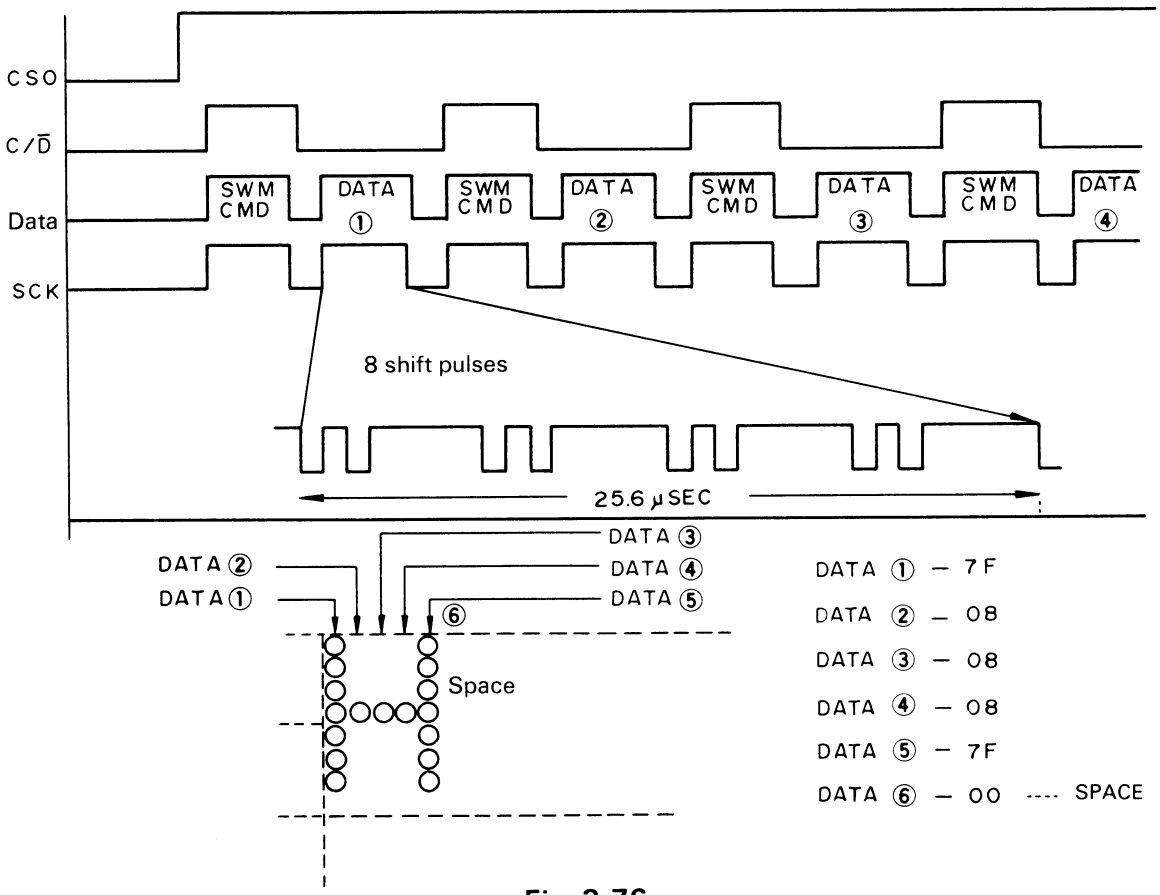


Fig. 3-76

One character is composed of a 5 x 7 dot matrix, and a space corresponding to one dot is necessary between adjacent characters. This means that 6 bytes each of data and command (a total of 12 bytes) are necessary to display a single character.
That is, a total of 960 bytes of data must be transferred to display characters on the whole screen. Simple transfer speed is about 24 msec as calculated by the following equation.

$$\underline{25.6\ \mu\text{sec} \times 2} \times 120 \times 4 = 2.4576 \times 10^4\ \mu\text{sec}$$

$$\text{Time for transferring a single command} = 24.576\ \text{msec}$$

$$\text{Time required for transferring a line of data for display on the screen.}$$

Actually, however, a longer timer than 24.576 msec is necessary for display data transfer because an additional time is required for switching the chips (of the 6 ICs μPD 7227s) and address designation by an LID (Load Immediate to Data Pointer) command.

3.5.7 Data Read

(1) This operation is performed only when making screen copies (pressing the CTRL key and COPY function key to output the displayed data to the printer to print out). In reading the displayed data out, select the read mode with an SRM command, set a read address into the data pointer with an LID command, and lower the C/$\overline{D}$ signal to low level (data mode). If an SCK signal is sent then, the data is serially read to the SO $\overline{BUSY}$ signal line.
The read data is routed via the keyboard and IC 4G (keyboard gate circuit) on the MOSU circuit board to data line 7. This serial data is converted into parallel data, which is then sent to the printer to be printed out.
The printer prints row by row so the same read operation must be repeated as many row lines as comprise a line of data. That is, data read must be repeated 960 times (120 columns × 8 rows) to print a line (20 characters).

(2) Data memories and display patterns

Data memory bit patterns correspond to display patterns as shown below.

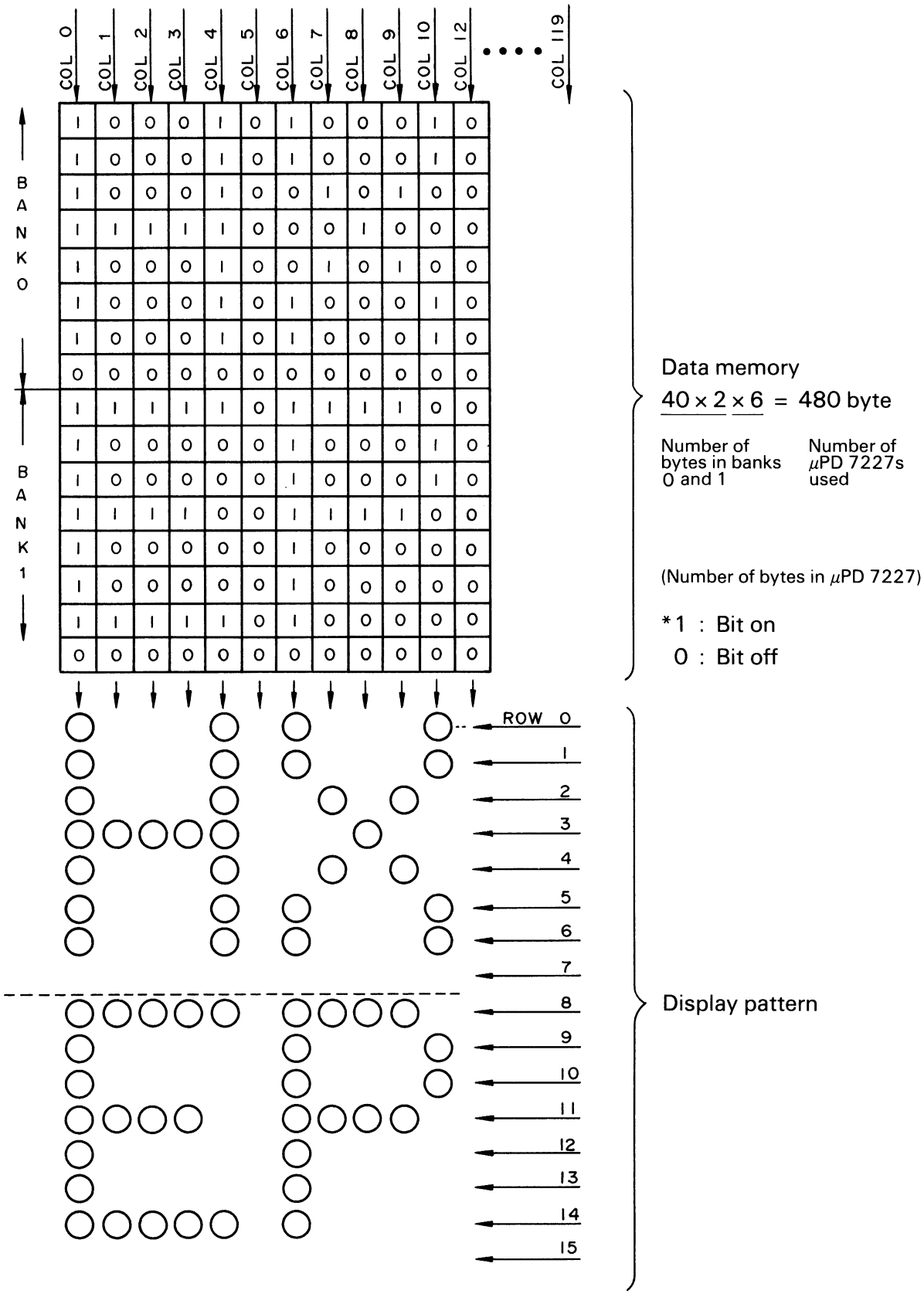


Fig. 3-77

3.5.8 Control Circuit

In transferring display data to the LCD, first address 0026 is output, and an appropriate data output is sent to DA 4 to DA 7 at this timing. Thus, the LCD's $\overline{CS}$ signal and C/$\overline{D}$ signal are input to IC 9G, where these signals are held. So an LCD $\overline{CS}$ (one of $\overline{CS0}$ to $\overline{CS5}$) signal can be input to the output end of IC 16G.

If address 002A is output and a transfer command or data to data bus lines under this condition, the command or data is input to IC 10G, which is a shift register. As an R/$\overline{W}$ signal is input to Pin 15 of IC 10G, the data is transferred from Pin 13 to IC 10H bit by bit. The bits received by IC 10H are sent to the SD line by the R/$\overline{W}$ signal timing and address 002A (IC 1F Pin 1 output).

As a chip has already been selected on the LCD side, the SD signal enters the selected chip (μpD 7227), and is shifted by an $\overline{SCK}$ signal for parallel conversion. Thus, the command or data can be received.

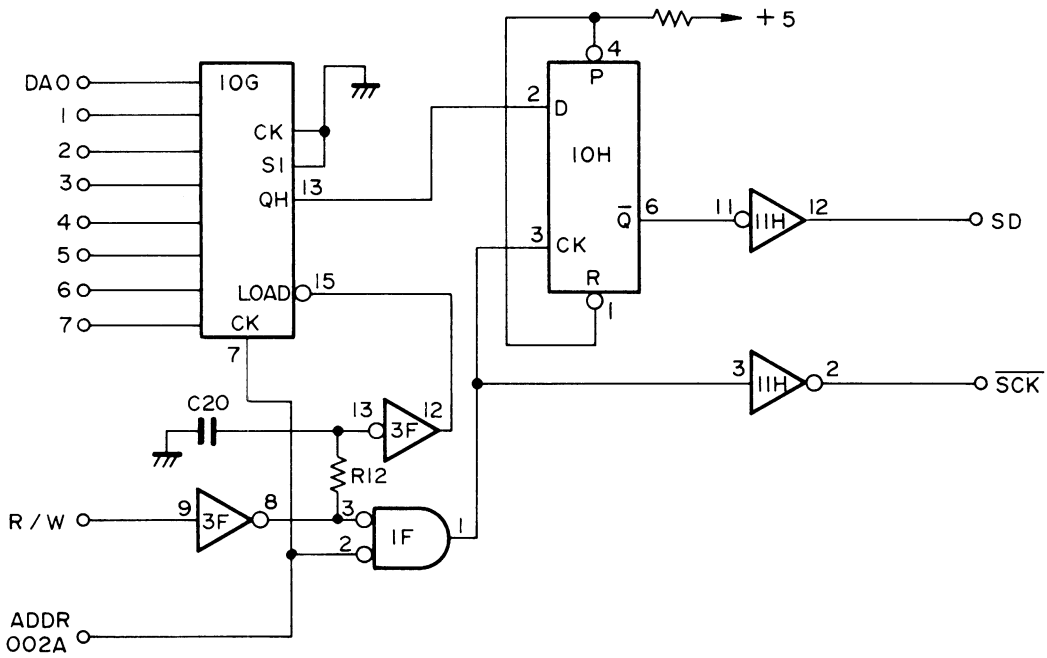


Fig. 3-78

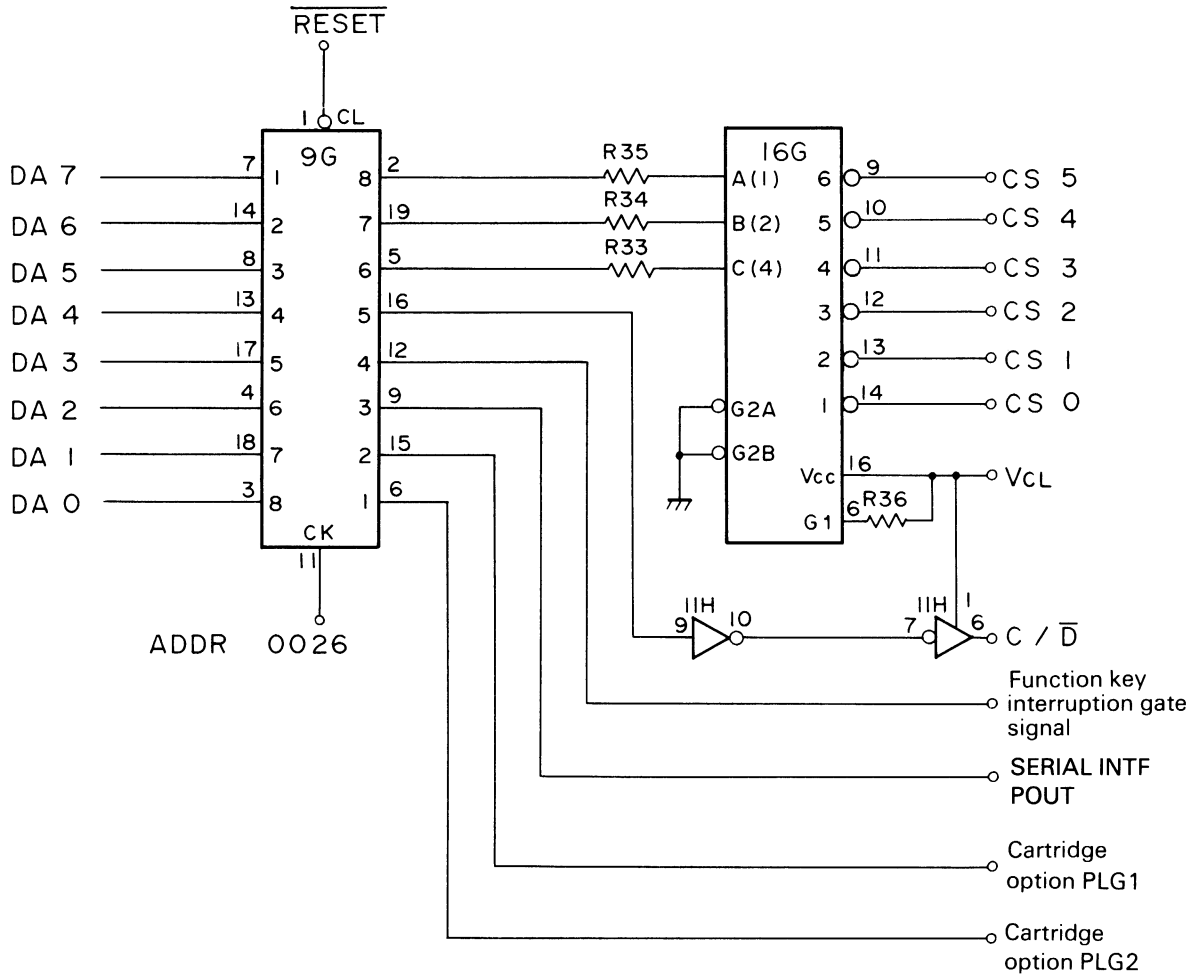


Fig. 3-79

	ADDRESS	DATA								HEX DATA
		7	6	5	4	3	2	1	0	
LCD CS 5	0026	X	X	X	X	X	○	○	X	06
LCD CS 4		X	X	X	X	X	○	X	○	05
LCD CS 3		X	X	X	X	X	○	X	X	04
LCD CS 2		X	X	X	X	X	X	○	○	03
LCD CS 1		X	X	X	X	X	X	○	X	02
LCD CS 0		X	X	X	X	X	X	X	○	01
LCD C/D		X	X	X	X	○	X	X	X	08
KEY INT MASK		X	X	X	○	X	X	X	X	10
P OUT		X	X	○	X	X	X	X	X	20
MO 1		X	○	X	X	X	X	X	X	40
MO 2		○	X	X	X	X	X	X	X	80

Fig. 3-80

3.5.9 Voltage Regulator Circuit

(1) The voltage regulator circuit located on the keyboard regulates the voltage to be applied to the LCD as the VIEW ANGLE knob is turned.

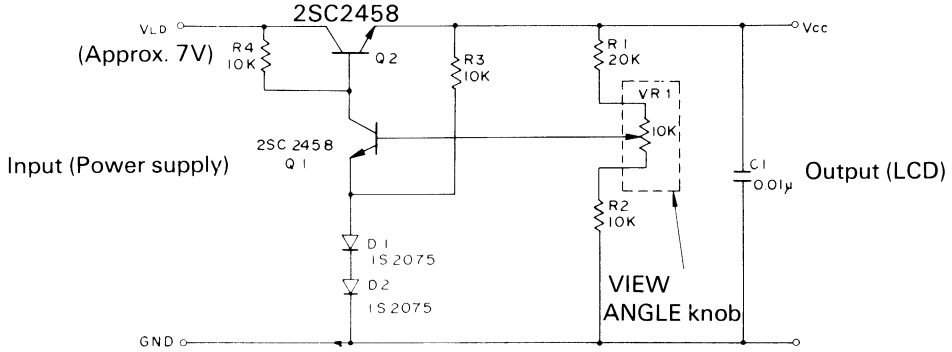


Fig. 3-81

The LCD is based on the theory of polarization for displaying characters, and the degree of polarization can be changed by varying the voltage applied to the LCD dot matrix. The voltage regulator circuit is necessary to compensate for the variation of liquid crystal reaction with temperature.

(2) Operation

The LCD voltage (VLD) generated by the MOSU circuit board is routed via transistor Q2 to its emitter, where it is output. This voltage enters the voltage dividing circuit composed of R1, R2 and VR1, from which (VR1: VIEW ANGLE knob) the voltage is applied to the base of transistor Q1. The level of this voltage can be adjusted with VR1, and the output voltage Vcc can be changed by controlling transistor Q1.

3.5.10 Voltage Dividing Circuit

Dot display on the LCD is controlled by voltage. That is, four voltages (V1, V2, V3, V4) are generated from the voltage Vcc that is supplied to the LCD unit. The LCD unit divides it by using resistors as shown below.

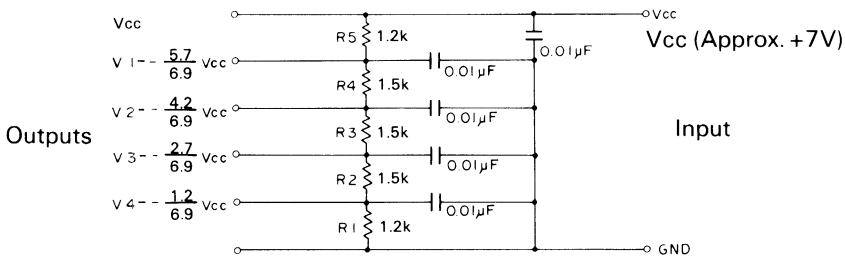


Fig. 3-82

The output voltages generated by the above circuit are as shown below.

LCD voltage

Vcc	100%	* 7V
V1	82.6%	5.78V
V2	60.8%	4.26V
V3	39.1%	2.74V
V4	17.4%	1.22V
VSG	GND	GND

* Vcc is variable.

3.5.11 Display Timing Example

The LCD outputs each column signal at the row line timing to change the reaction of the liquid crystals with its signal voltage, and displays characters in dots. An example of signal waveform and display dots is shown below.

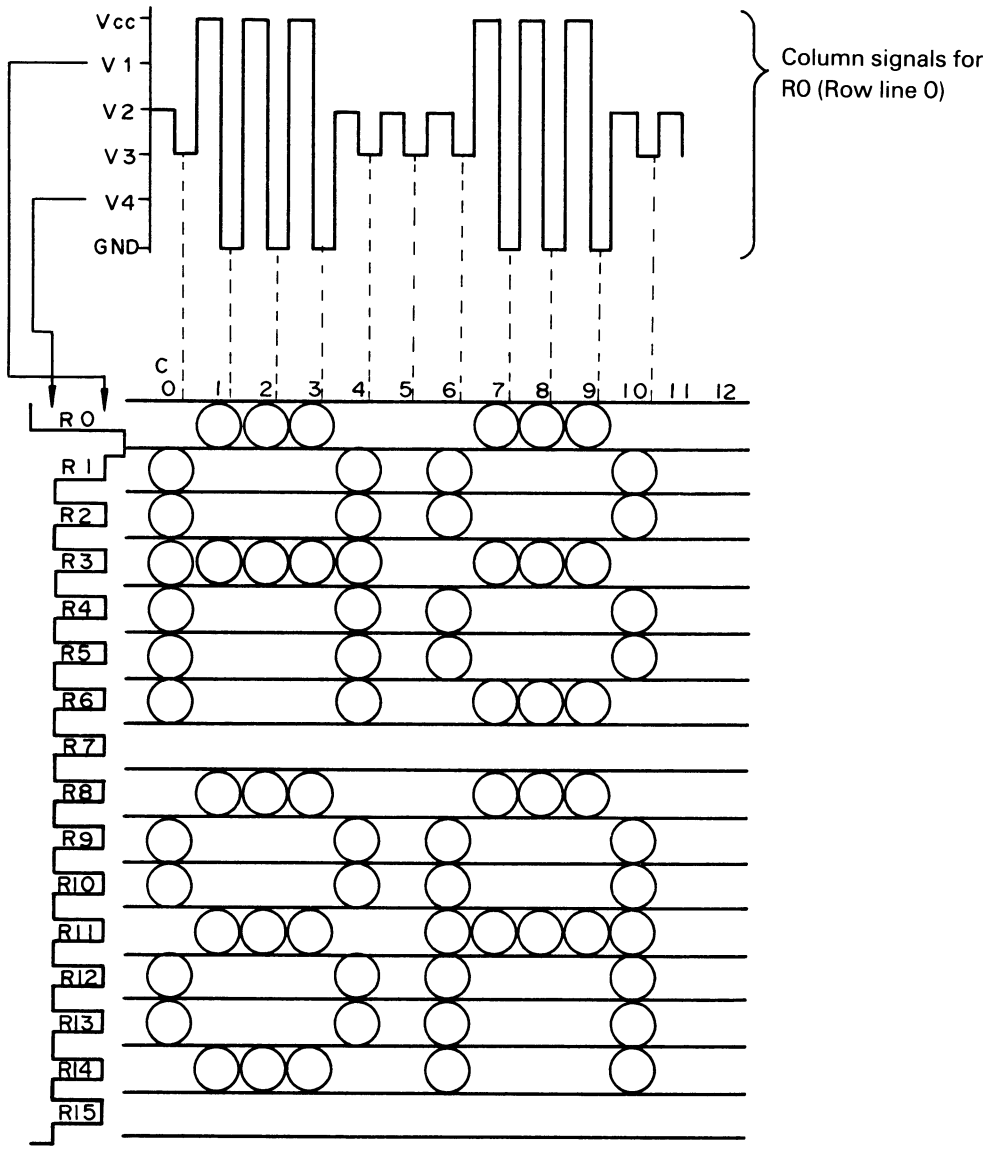


Fig. 3-83

3.6 Keyboard

The keyboard is connected to connectors 1 and 2 on the MOSU circuit board, outputs key data, and supplies signals to the piezo-electric buzzer and the LCD.

3.6.1 Hardware Composition

The keyboard unit consists of the following 5 components.

1. Key switches
   60 contact-point type key switches (data keys)
   8 rubber contact-point type key switches (function keys)
   1 slide switch (Printer switch)
   1 push switch (Paper feed switch)
2. View angle adjusting circuit: LCD view angle control knob and voltage regulator circuit
3. Power switch: To switch the HX-20 on and off, and output 2 kinds of ($\overline{\text{PW SW}}$) signal to the MOSU circuit board
4. Piezo-electric buzzer connector: To send buzzer signals from the MOSU circuit board to the buzzer via a connector
5. LDC signal circuit: To send LCD signals from connectors CN4 and CN5 to the KCN1 via the keyboard

3.6.2 Key Switches

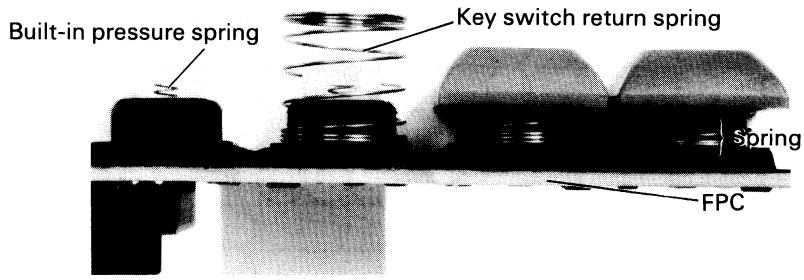


Fig. 3-84

The keyboard switches contact the wiring pattern on the keyboard circuit board with the wiring pattern on the FPC under the pressure produced by the springs installed in the switches. Normally, the built-in switch springs are in an extended state so the electroconductive pattern on the FPC is clear of the pattern on the circuit board. When a key switch is pressed, the spring is compressed to force the conductive parts of the FPC and circuit board into contact.

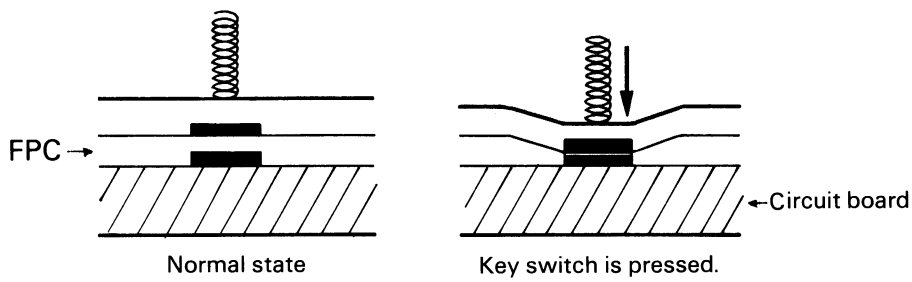


Fig. 3-85 **Fig. 3-86**

3.6.3 Key Switch Signal Input

(1) The key switches comprise a 10 x 8 matrix, and when a key switch is pressed, a KSC signal line and a KRTN signal line contact with each other. Normally, the KRTN signal lines are pulled up by a +5V, but when a KRTN signal line contacts a KSC signal, it goes low so the output of IC 1G goes high. This high-level output is sent through the circuit shown below to turn an IRQ signal on in the main CPU. The depression of a key switch shorts the KRTN signal with a KSC line (normally low) and lowers the signal, and an interrupt request signal $\overline{\text{KB REQUEST}}$ is output to the main CPU via the OR circuit of IC 1G. Then, addresses 0022 and 0028 are output, and the keyboard data is read via IC 3G and IC 4G to the data bus lines.

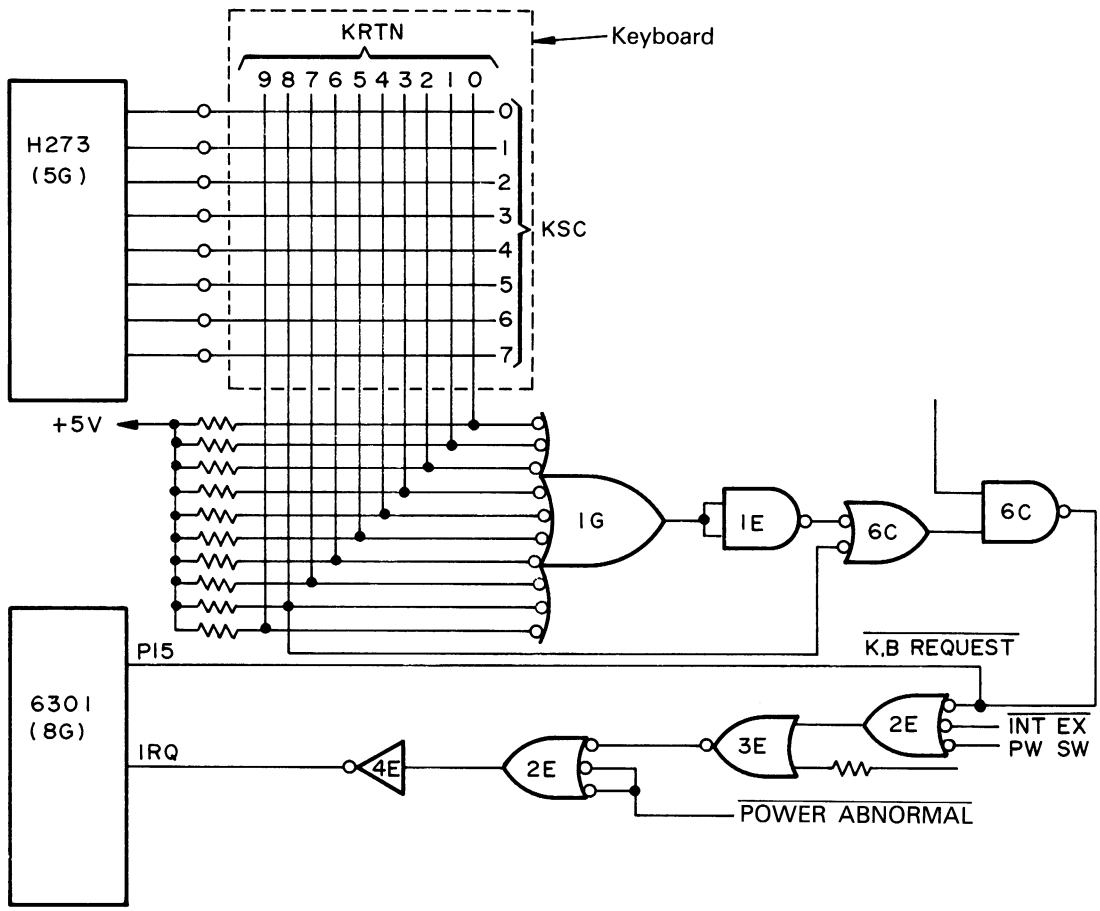


Fig. 3-87

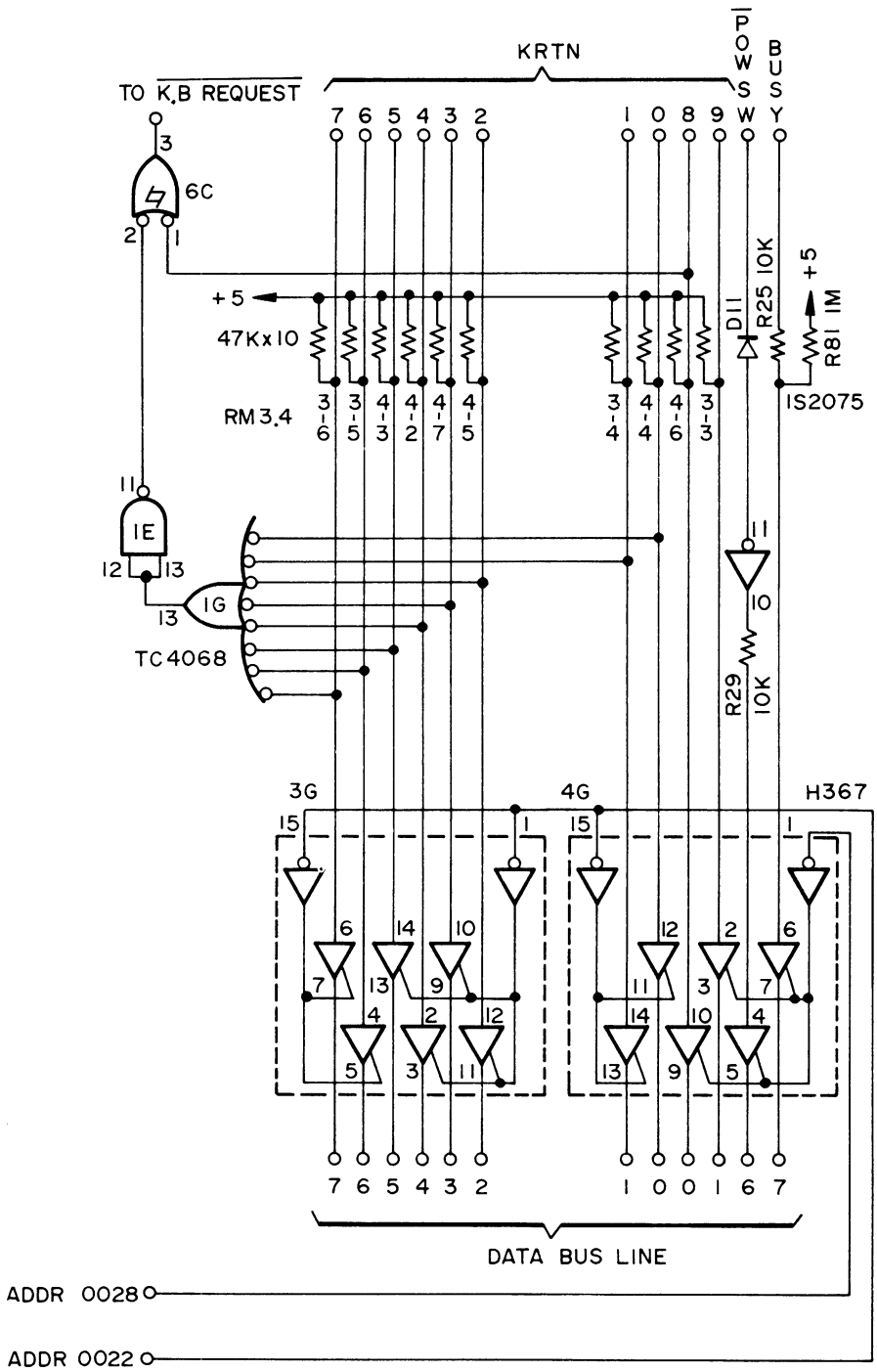

KRTN
POWSW BUSY
TO K.B REQUEST
7 6 5 4 3 2
1 0 8 9
3
6C
2
1
+5
47Kx10
RM3.4
3-6
3-5
4-3
4-2
4-7
4-5
3-4
4-4
4-6
3-3
D11
R25 10K
+5
R81 1M
IS2075
11
1E
12
13
1G
13
TC4068
11
10
R29
10K
3G
4G
H367
15
1
6
14
10
7
13
9
4
2
12
5
3
11
12
2
6
11
3
7
14
10
4
13
9
5
7 6 5 4 3 2
1 0 0 1 6 7
DATA BUS LINE
ADDR 0028
ADDR 0022

Fig. 3-88

(2) When the main CPU receives the IRQ signal, it checks the ports and identifies it as $\overline{\text{KB REQUEST}}$. Then, it outputs a keyboard address, and KSC signal data to the data bus lines. IC 5G outputs one KSC signal after another. If a key is depressed, a KSC signal is output to the corresponding KRTN signal line so this signal is read to the data lines via IC 3G or IC 4G to identify the key switch depressed.

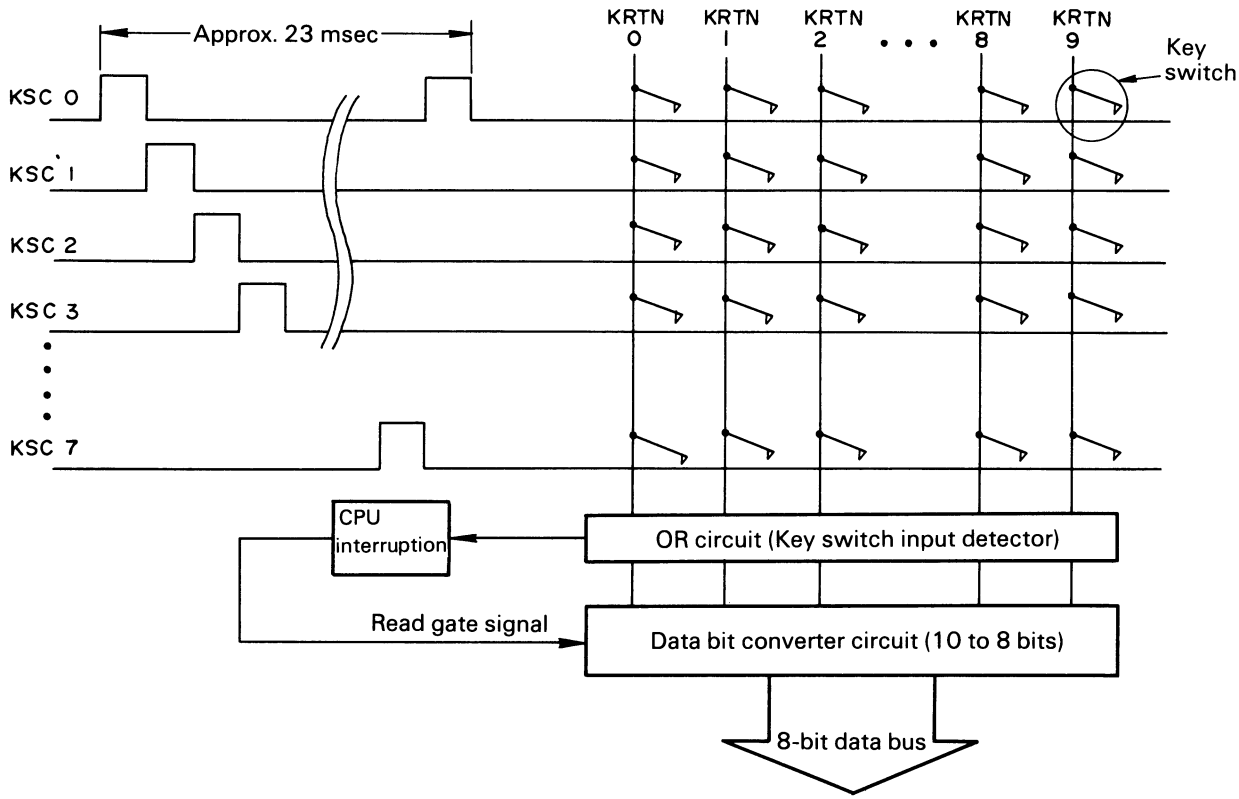


Fig. 3-89

(3) The function keys use rubber contact points instead of the FPC pattern. As the rubber contact point of a function key contacts the pattern on the circuit board, interruption processing takes place as when a data key is pressed, and the function key depressed is identified.

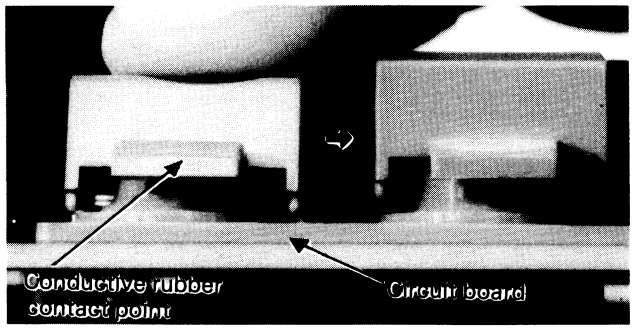


Fig. 3-90

3.6.4 Power Switch

The power switch is at floating level when it is off, and at low level when it is on. The power switch sends $\overline{\text{PW SW}}$ signals to connectors CN4 and CN5 on the MOSU circuit board; and a power on signal (V_L ON) and a battery voltage detector circuit signal ($\overline{\text{PW SW}}$).

3.6.5 Piezo-electric Buzzer Connector

An SP signal output from the MOSU circuit board is received via connector CN5, and sent to the piezo-electric buzzer via connector KCN2 on the back of the keyboard.

3.6.6 LCD Signal Circuit

Signal outputs from the MOSU circuit board are supplied to connector KCN2 in the keyboard pattern, from which LCD control signal and display data are output.

* View angle adjusting circuit
  Refer to the section on the LCD unit for details.

3.6.7 Keyboard Switch Structure

The keyboard FPC (flexible printed circuit) uses carbon-coated contact points to improve their durability. The same is true of the parts connected to connectors CN4 and CN5 on the MOSU circuit board. Therefore, the connectors and contact points have high resistance. A continuity test conducted on the connector signal lines and the same signal lines on the keyboard normally shows a resistance of about 15 to 20 ohms*.

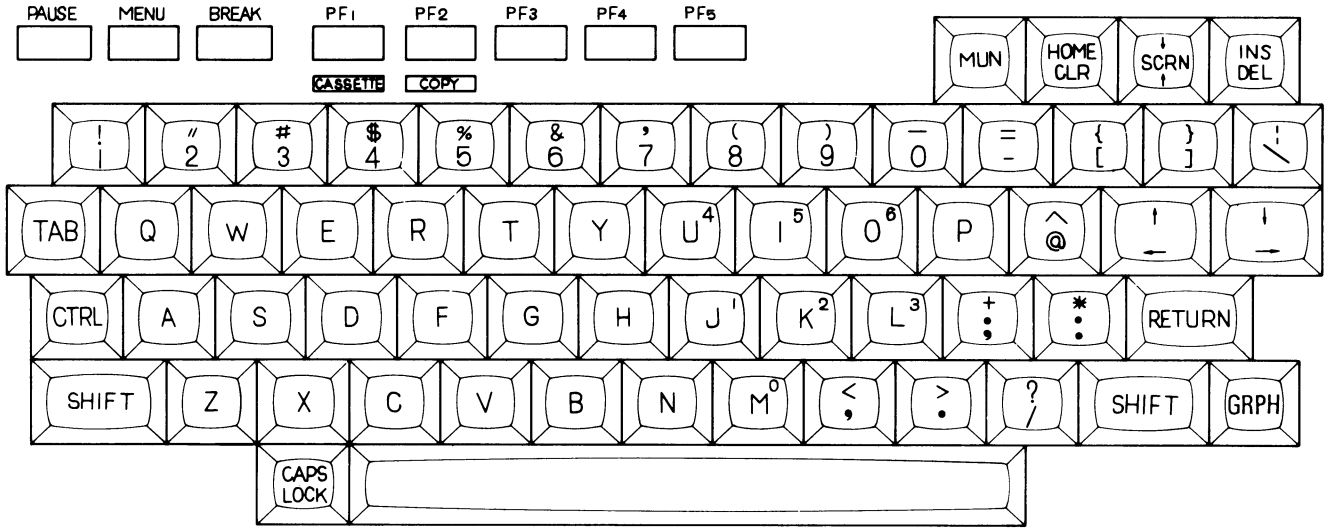
A continuity test on a KSC line and a KRTN signal line also gives a resistance of about 15 kilohms when the corresponding switch is depressed. Although the connector resistance is considerably high, the signals (LCD, SP, KSC, KRTN) that are routed through the keyboard require little current so signal voltage drop is too small to present any operational problems.

* The resistance of the KRTN and KSC lines were measured by connecting a tester as follows:

Tester { Black lead to KSC
Red lead to KRTN

3.6.8 Key Switch Code

Each switch on the keyboard is read by KSC and KRTN signals, and has a code as shown below.



ASCII KEY BOARD

Fig. 3-91

* The data key switches are not independent of one another, but the right and left key switches are integrally built with the frame.

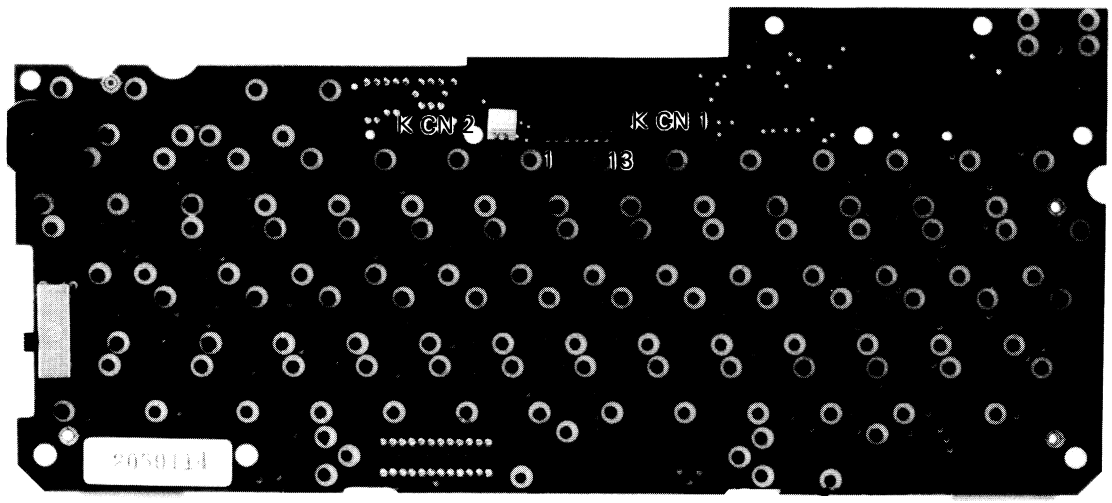
KSC \ KRTN	0	1	2	3	4	5	6	7	8	9
0	0	1	2	3	4	5	6	7	PF 1	SW6 1
1	8	9	:	;	,	—	.	/	PF 2	SW6 2
2	@	A	B	C	D	E	F	G	PF 3	SW6 3
3	H	I	J	K	L	M	N	O	PF 4	SW6 4
4	P	Q	R	S	T	U	V	W	PF 5	
5	X	Y	Z	[	]	\	←	→	PAPER FEED	SHIFT
6	RET	SP	TAB			NUM	GRPH	CAPS LOCK *		CTRL
7	CLR HOME	SCRN	SRAKE	PAUSE	INS DEL	MENU				PRTR ON/OFF

* CAPS LOCK = SHEET CLOCK

Fig. 3-92

3.6.9 Keyboard Connector Signals

The keyboard has FPC cables to connect to CN4 and CN5 on the MOSU circuit board and connectors to connect to the LCD and piezo-electric buzzer. See the table below for the connectors and signals.



TO CN4
20 1

Rear View

Fig. 3-93

TO CN5
20 1

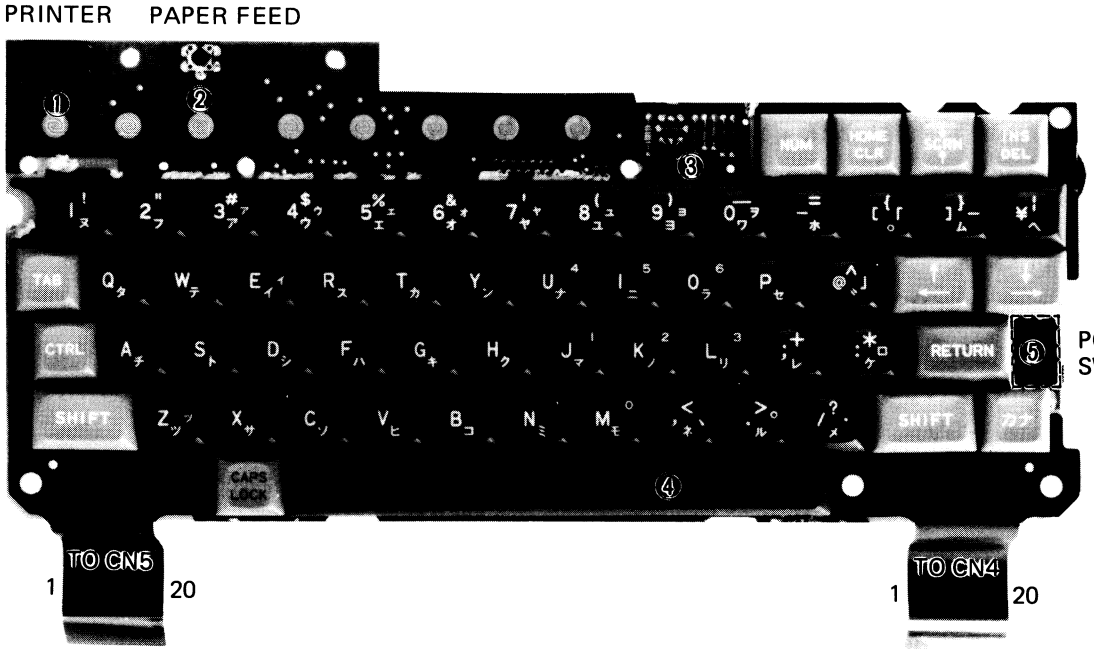
CN4

Pin No.	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Signal	$\overline{BUSY}$ SO	$\overline{PWSW}$	KRTN0	KRTN1	KRTN2	KRTN3	KRTN4	KRTN5	KRTN6	KRTN7	KRTN8	KRTN9	KSC7	KSC6	KSC5	KSC4	KSC3	KSC2	KSC1	KSC0
KCN1	12																			

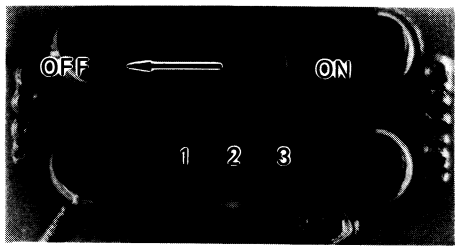
CN5

Pin No.	20	19	18	17	16 15 14	13	12	11	10	9	8	7	6	5	4	3	2 1
Signal	SPG	SP	$\overline{PWSW}$	VLD	GND	$\overline{CS0}$	$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	$\overline{CS5}$	SCK	SD	CLK	C/$\overline{D}$	RESET	VCL
KCN1				13	0	1	4	3	5	2	6	11	10	8	9	7	

3.6.10 Keyboard Layout

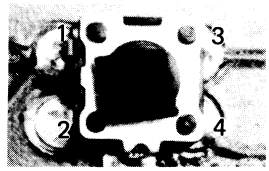


①



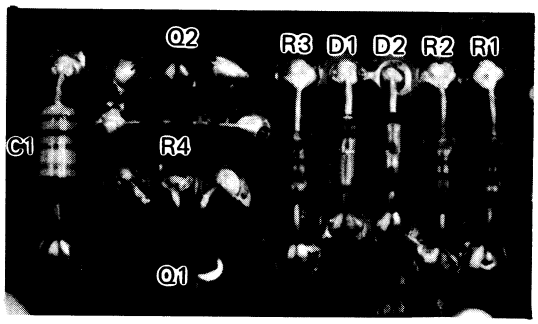
Pints 1 and 2 are electrically connected when the key is pushed in the arrow direction.
3: Unused

②

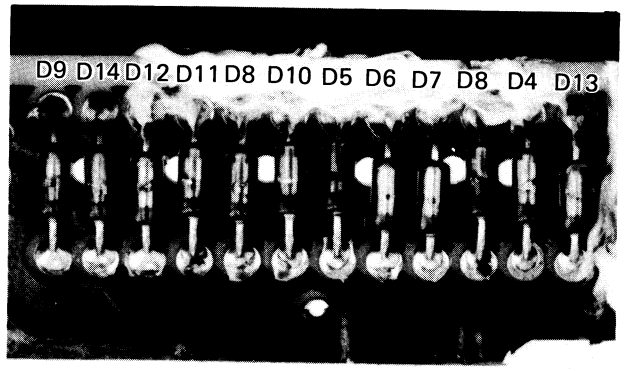


1 ↔ 3 : Shorted
2 : Unused
4 : If the N/O switch is pushed to Pin 1 or 3, Pins 1 or 3 and Pin 4 are electrically connected.

③

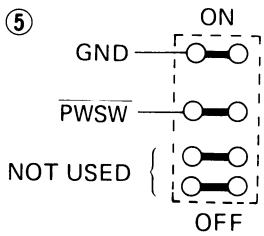


④



Resistance from CN4 to each KSC is 15 to 20 ohms.

⑤



Resistance from CN4 to each power switch lead is approximately 15 ohms.

Fig. 3-94

3.7 RS-232C Interface

The HX-20 uses the RS-232C to send and receive data with a terminal printer and personal computer, or via the acoustic coupler CX-20, with other terminal equipment.

The RS-232C requires specific voltages (+25V to +3V for space, ie., logic 0, and −25V to −3V for mark, i.e., logic 1, which must be generated from the battery voltage of +5V. The HX-20 has a built-in regulator to generate +8V and −8V for the RS-232C. This regulator is controlled by software so it is operated only when the RS-232C is used.

3.7.1 Power On

When using the RS-232C, first Pin 36 of the slave CPU 6301 to high level. As a result, Pin 12 of IC 7E goes low, and an $\overline{SWL}$ signal turns transistor Q2 on. Thus, the voltage V_B is applied to Pin 14 (Vcc) of TL 497 to make it ready for operation. TL 497 starts switching Q11 to generate ± 8V.

The +8V is routed via R22 (5.1K) as a DTR signal, which is sent to the MODEM for simultaneously confirming connection of the HX-20 to the MODEM interface.

The HX-20 uses a USART IC (6B: HD75188 quad line driver; 7B: HD75189 quad line receiver), which conforms to the USART standard, for the RS-232C interface so when the voltage ± 8V are supplied, the system operates to the RS-232C standard.

* USART stands for Universal synchronous Asynchronous Receiver Transmitter.

3.7.2 Interface Circuit

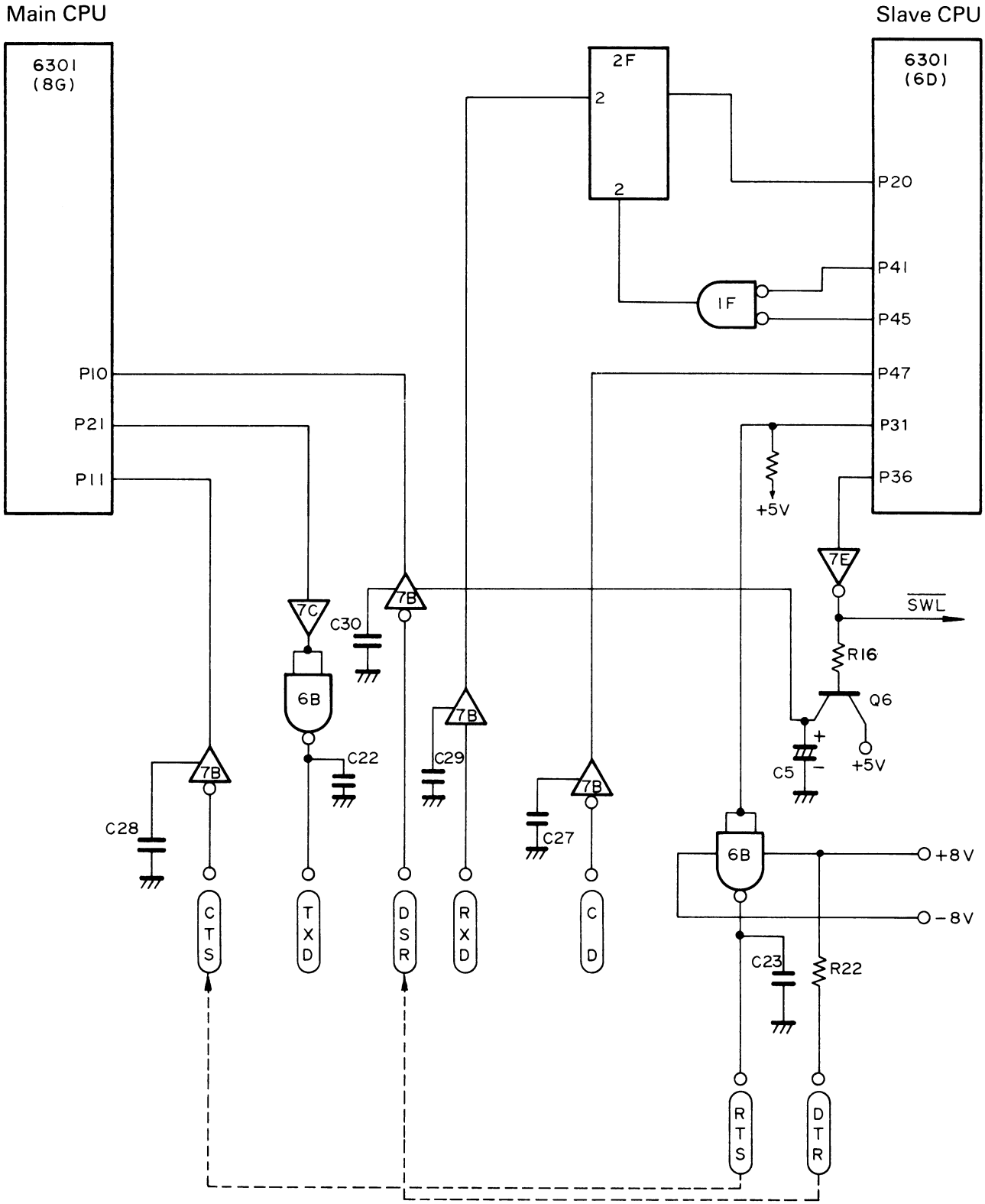


Fig. 3-95

3.7.3 Operation Sequence

The HX-20 controls the operation of the RS-232C with the main CPU 6301 (8G) and slave CPU 6301 (6D). Data transmission is controlled by the main CPU, and data receiving by the slave CPU.

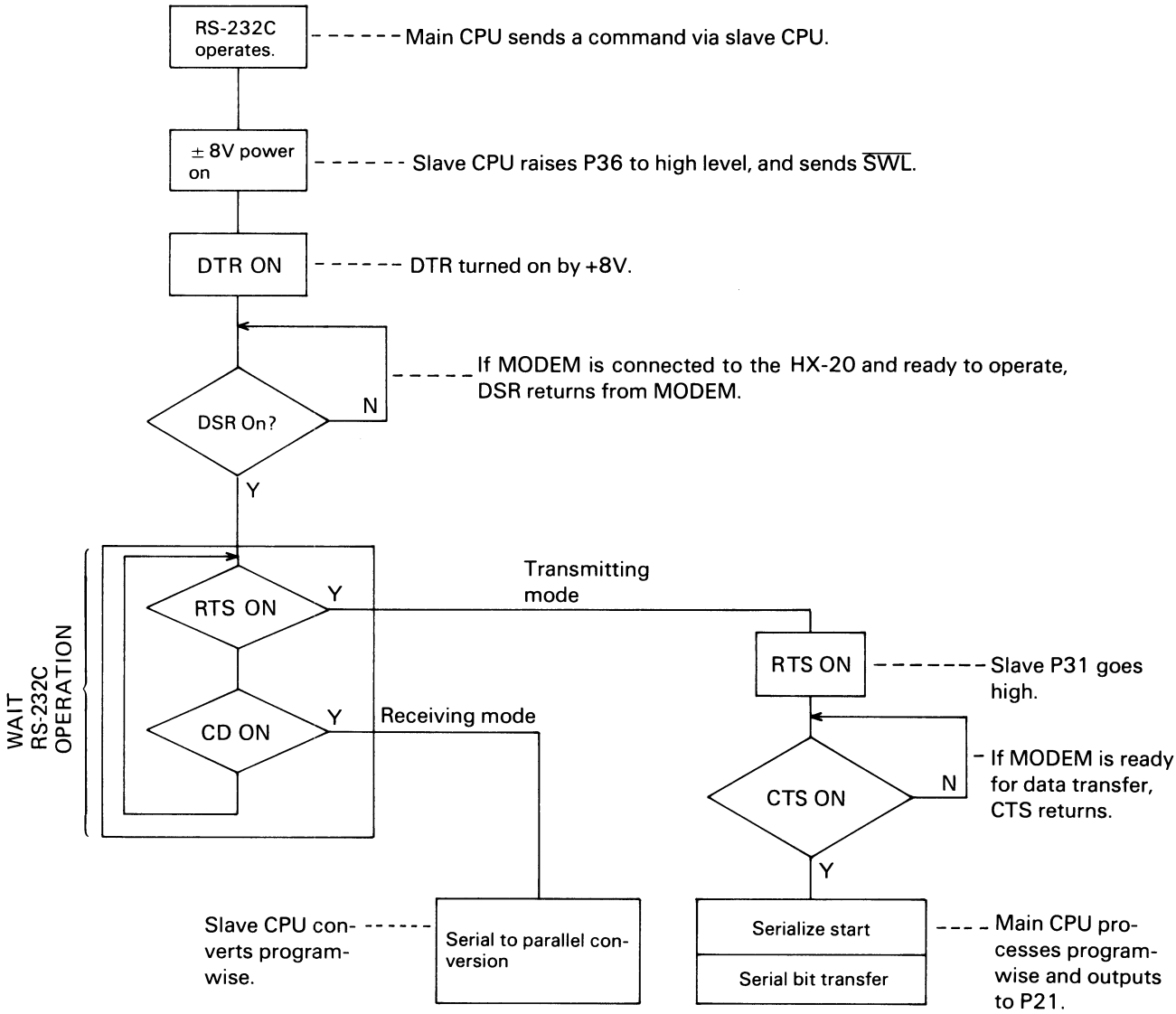
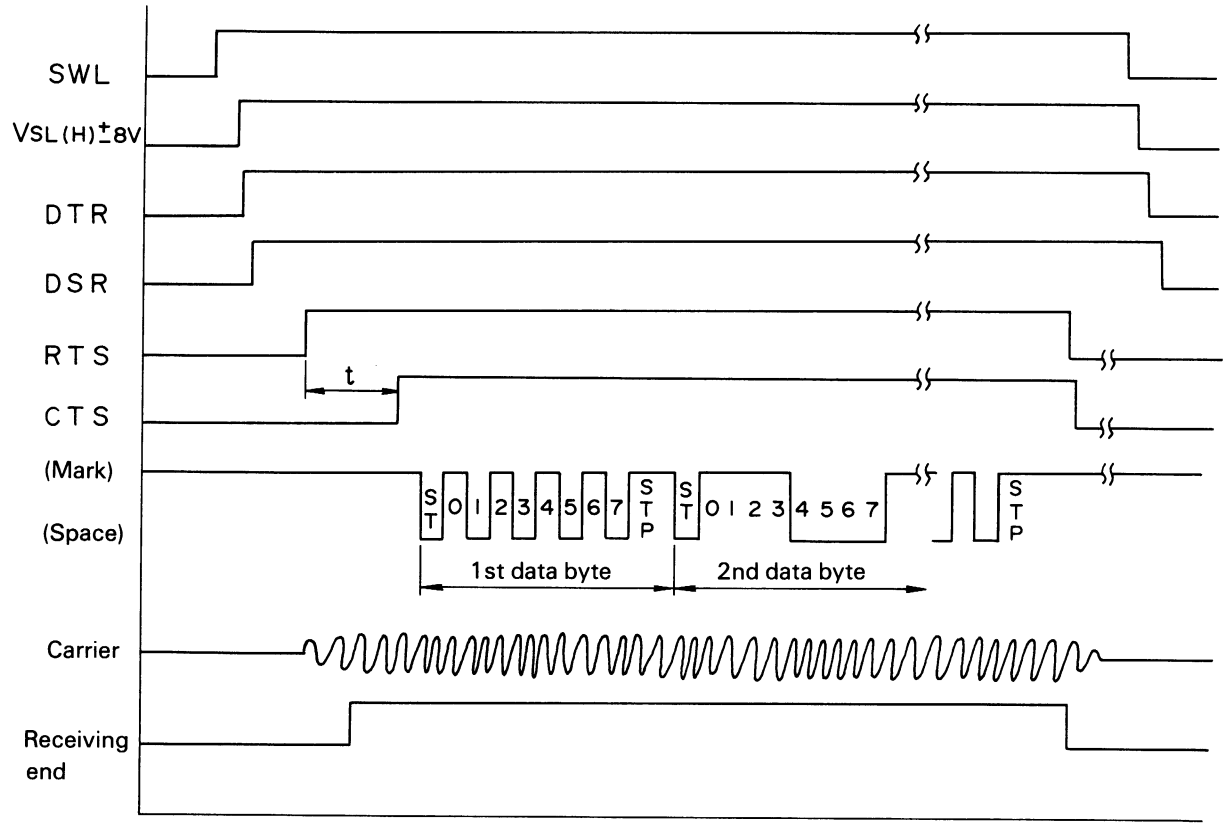


Fig. 3-96

3.7.4 RS-232C Operation Timing



*t: Delayed time until MODEM is ready for data transfer.

Fig. 3-97

(1) Signal polarities

- Mark = Logic 1 (−3V to −25V): Stop bit
- Space = Logic 0 (+3V to +25V): Start bit

(2) Word length

- Start bit: 1 bit
- Data bit 7 or 8 bits
- Stop bit: 1 bit or longer

(3) Bit rate: 110 bps to 4800 bps

3.7.5 Operation Where MODEM (Coupler) Is Used

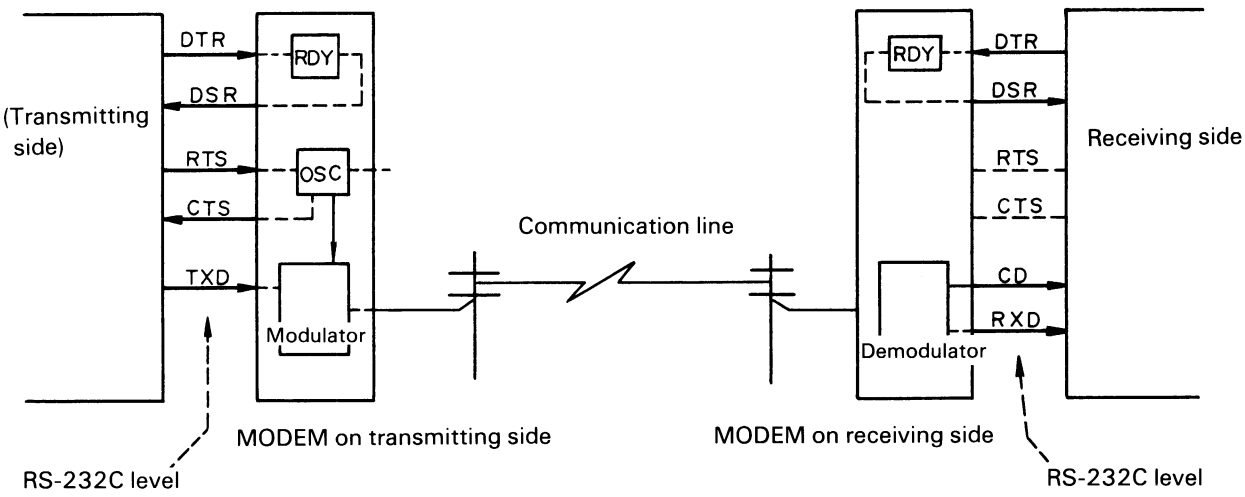


Fig. 3-98

MODEM: MODEM stands for modulation and demodulation, and modulation comes in different kinds, including FSK (Frequency Shift Key), PSK (Phase Shift Key), and AM (Amplitude Modulation).

Operation

A DTR is sent to check if the MODEM is ready to operate.
If it is, the MODEM outputs a DSR signal. If there is data to send after receiving the DSR, an RTS signal is sent to request the MODEM to send. When the MODEM receives the RTS signal, the carrier oscillator operates to output its output carrier to the transmitting data line.
A CTS signal is sent to the transmitting terminal after the oscillator output stabilizes. (The time required for the oscillator to stabilize in output level varies with the characteristics.)
When the MODEM on the receiving side detects the carrier from the receiving data line, it outputs a CD (Carrier Detect) signal, and makes the receiving terminal ready for receiving.
When the transmitting terminal receives the CTS signal, it converts the data to be transmitted from parallel to serial, and starts sending the data to the MODEM bit by bit. The MODEM modulates the data bits, and sends them to the transmitting data line.
The receiving terminal, which is made ready for receiving by the CD signal, demodulates the transmitted modulated data by the MODEM, and sends the digital data to the receiving terminal.

The timing chart shown below illustrates the above operation.

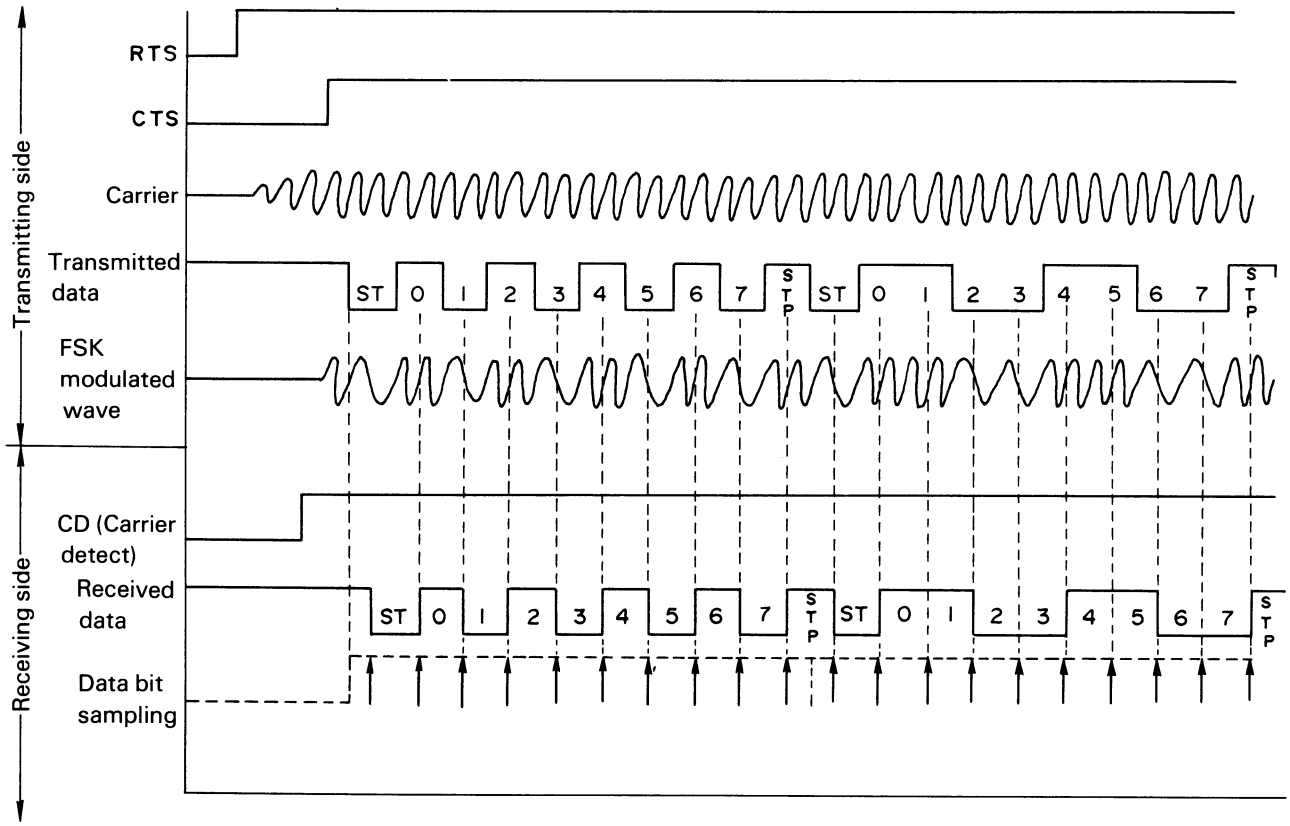


Fig. 3-99

3.7.6 Data Transfer Between HX-20s

In this case, HX-20s are directly connected to each other without MODEMs so, different from normal RS-232C operation, the signals generated by MODEMs are generated by cable connections.

(1) DSR and DTR lines are crossed to turn on the DSR of the opposite terminal with its own DTR signal.

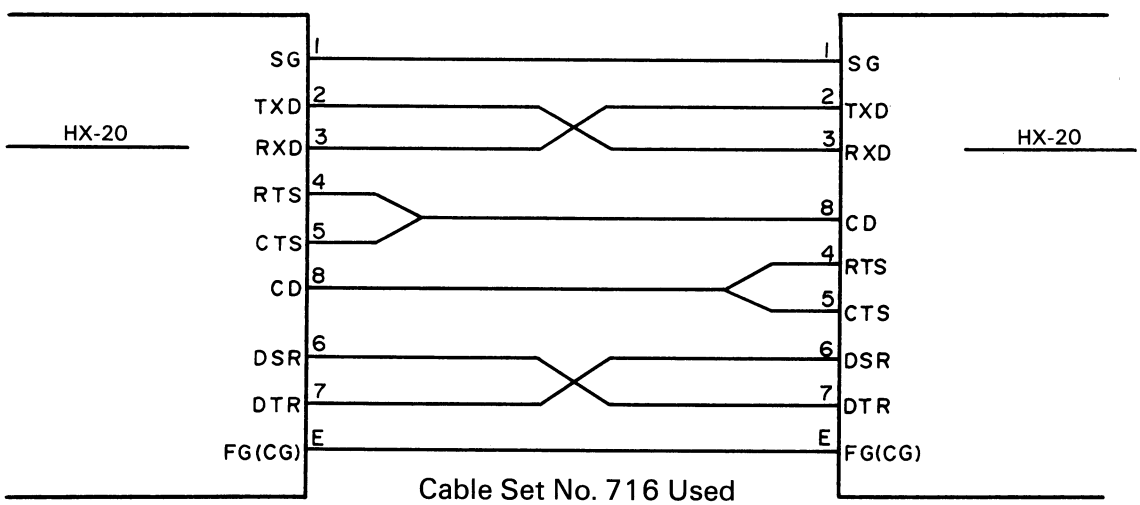


Fig. 3-100

(2) Pins RTS and CTS are connected to each other so that, if an RTS is output, a CTS will be automatically detected.

This signal is sent to the opposite HX-20 through its CD line to make it ready for receiving.

3.7.7 Connecting Printer (EPSON Printer for HX-20)

A serial interface (No. 8145 serial interface with a 2K buffer) is necessary on the printer side when connecting the HX-20 to a printer.

If this interface is used, the printer only receives data from the HX-20, but does not send data to the HX-20.

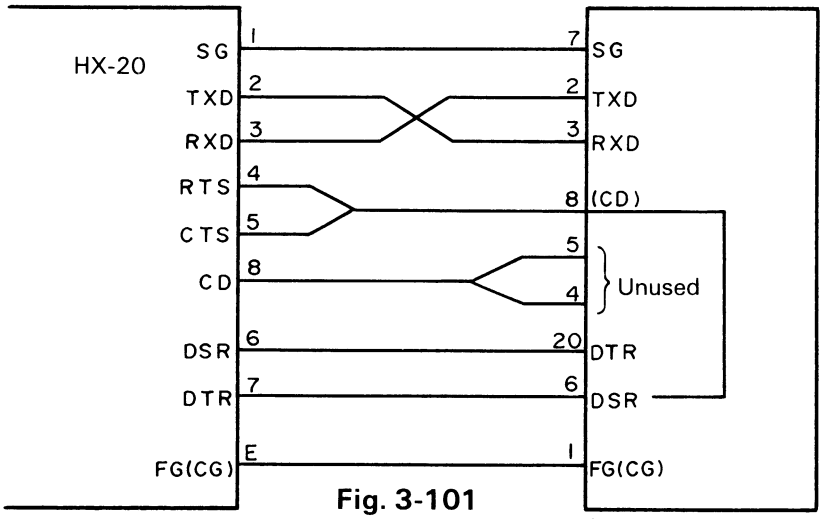


Fig. 3-101

Serial interface (No. 8145)

(1) RTS and CTS on the HX-20 are connected to each other in its cable, and its signal is connected to Pin 8 (CD) on the printer side. Pins 8 (CD) and 6 (DSR) on the serial interface circuit board on the printer side are connected to each other, and Pin 6 is connected to Pin DTR on the HX-20.

Therefore, if the HX-20 outputs a DTR or RTS, the HX-20's RTS, CTS and DTR are turns on, and the printer's Cd and DSR are turned on.

(2) The DTR signal on the printer side indicates whether data can be transferred. (If it is at high level, data can be transferred.) This signal is connected to DSR on the HX-20. Therefore, the HX-20 transfers data to the printer while checking this DSR signal.

3.8 Serial Interface

The serial interface uses high-speed data transfer lines between the main and slave CPUs, and releases these lines to the outside as high-speed serial interface.

As this serial interface can transfer data at high speed (38,400 bps maximum), a TV monitor floppy drive can be connected via display adaptors.

3.8.1 Operation Control

IC 4D (4016) is provided between the main CPU and slave CPU, and its gate signal is controlled at Port 22 by the main CPU to switch serial lines and transfer data by full duplex.

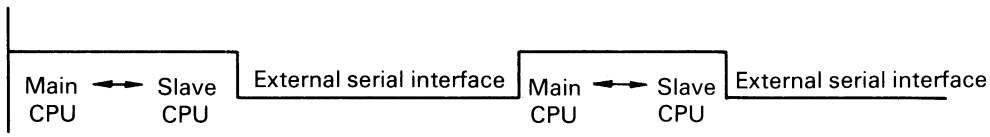


Fig. 3-102

3.8.2 Interface Operation

Where a serial interface is used, data is transferred without MODEMs, and MODEM control signals are necessary so that it is simpler than the RS-232C interface. When sending data, a P OUT signal is sent and then serial data is sent to the $\overline{\text{PTX}}$ signal line. When receiving data, a PIN signal is sent from the display adaptor prior to data transfer. After receiving the PIN signal, the $\overline{\text{PRX}}$ line data is received by the main CPU at Port 23. Simultaneous data transmission and reception can be made by full duplex operation through 4 signal lines.

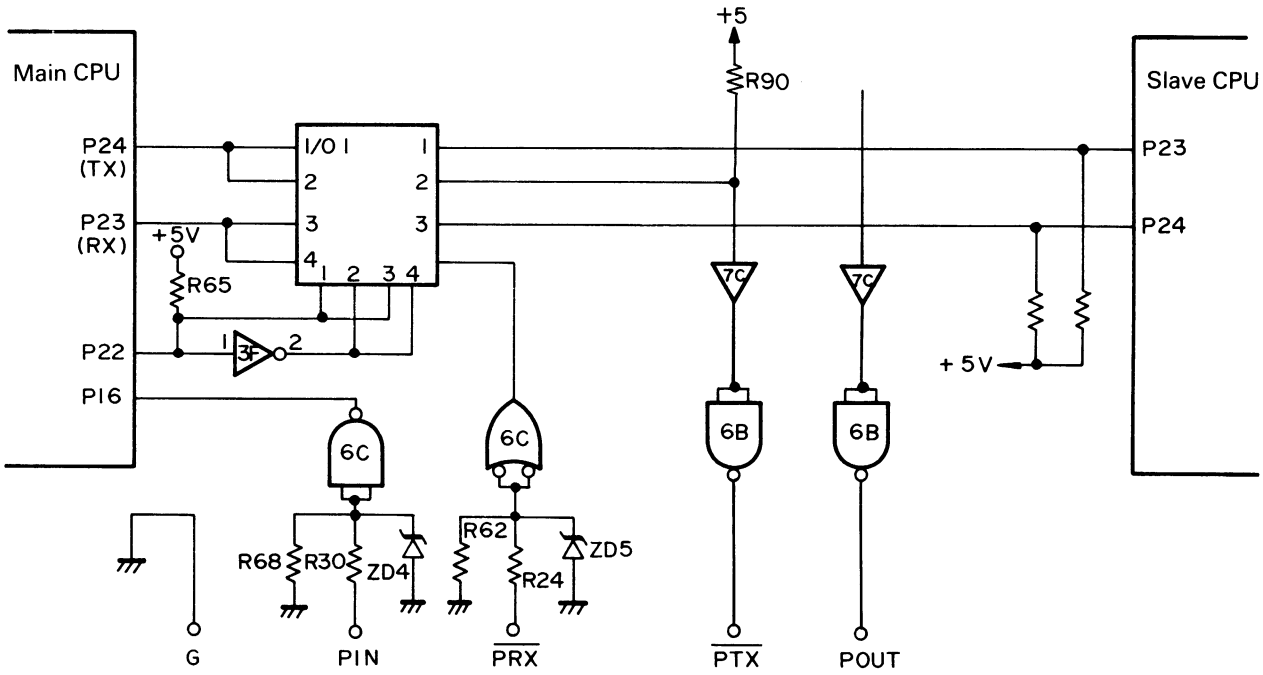


Fig. 3-103

Signal Level

In sending data to or receiving data from the outside, a signal level conforming to the RS-232C standard is used. In this case, voltage of ± 8V must be generated by the power supply before starting operation as in the case of the RS-232C.

3.8.3 Data Transfer Between HX-20s

Data can be transferred from one HX-20 to another or vice by using the cable set No. 717. Pins $\overline{\text{PTX}}$ and Pins $\overline{\text{PRX}}$s are connected to each other across; and so are Pins PINs and Pins P OUTs within the cables.

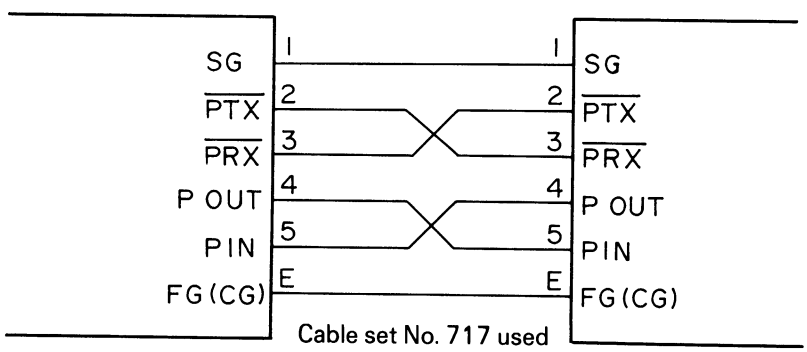


Fig. 3-104

3.8.4 Connecting Display Controller or Terminal Floppy

The cable set NO. 707 is used for daisy-chain connection.

This cable set uses 5-pin and 6-pin DIN connectors for preventing wrong engagement with the display controller. Pin 6 is unused.

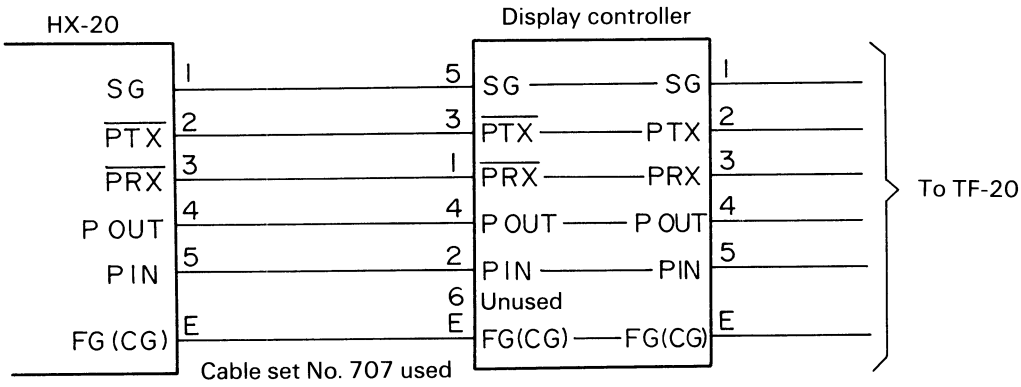


Fig. 3-105

3.9 External Cassette Interface

The external cassette interface is used for reading or writing data (programs by using a normal cassette tape recorder.)

Because cassette tape recorders vary in frequency response, tape speed, read/write head position (azimuth) adjustment from one type to another, the same recorder must be used in read and write operations. If cassette tapes written by use of different cassette tape recorders are read by another one, the possibility of occurrence of read errors is high.

3.9.1 Operation Control

All control operations are performed by the slave CPU, which is connected to a cassette tape recorder with cable set No. 702.

3.9.2 Motor Control Circuit

If the RMT cable is plugged into a cassette tape recorder and set into the play mode, the tape recorder motor can be controlled from the HX-20. When a LOAD or SAVE command is received, the slave CPU sets P30 to low level. As a result, the anode of diode D8 goes low, and relay LAD1 closes its contact points so that the motor circuit shown in the diagram below closes to start winding the cassette tape.

In an unused state, the IN signal line is pulled up by diode D10 to reject data. As P30 of the slave CPU goes low when the motor is turned on, the IN signal line becomes ready for operation.

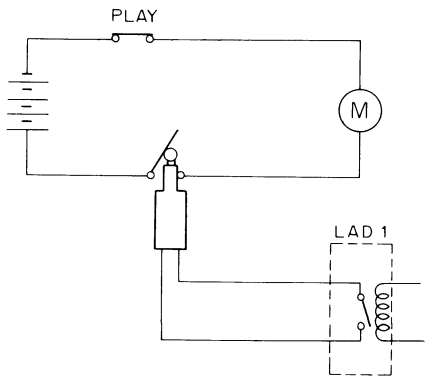


Fig. 3-106

3.9.3 External Cassette Connection

Use the special cable set No. 702 to connect the HX-20 to an external cassette tape recorder as shown below.

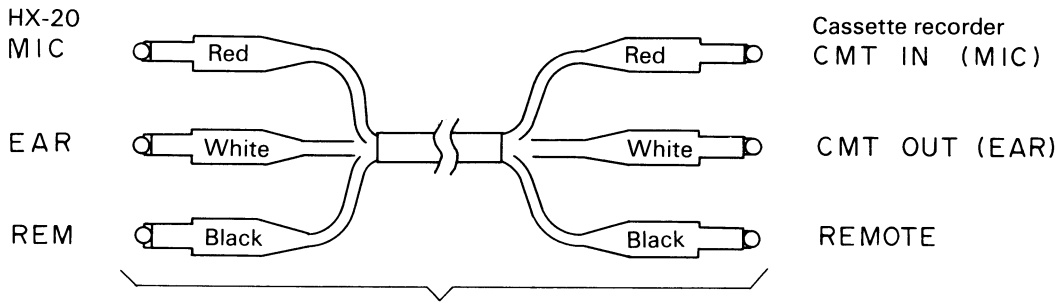


Fig. 3-107

Remote signals are for controlling the cassette tape recorder motor. When using the remote signal line for switching on and off the recorder motor from the HX-20, the play switch on the cassette tape recorder must be in the on position.

Note:

Do not plug the remote cable into the connector when manually controlling the cassette tape recorder without using remote signals.

3.9.4 Read/Write Signals

The read/write waveform has a period of 1 kHz when on and a period of 2 kHz when off.

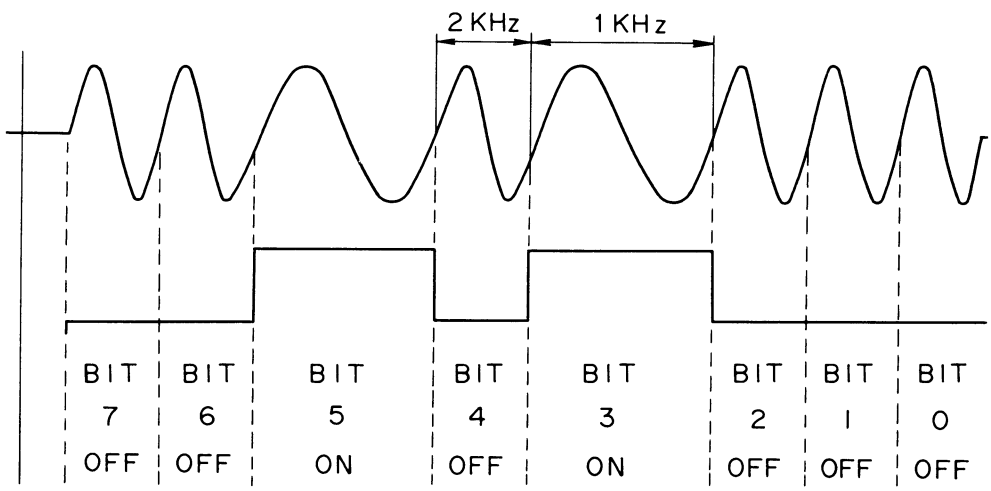


Fig. 3-108

3.9.5 Data Read

Output signals from the cassette tape recorder are routed through capacitor C1 to remove their DC components and take out only the AC components. Simultaneously, the high-voltage components generated by noise are eliminated by zener diode ZD6.

The resultant AC components are supplied to IC 8D, where they are subject to a threshold process by capacitor C25 and resistor R55 to be as shown at 3 in the diagram at right. The signals applied to Pin 9 of IC 8D are amplified and supplied to the slave CPU as pulse signals.

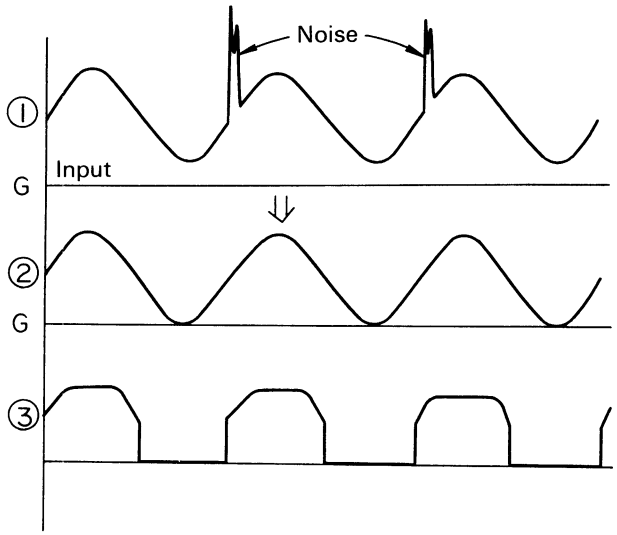


Fig. 3-109

3.9.6 Data Write

When a pulse signal is sent from Pin 33 of the slave CPU, it is routed through the R/W circuit of the cassette tape recorder to write data on the tape.

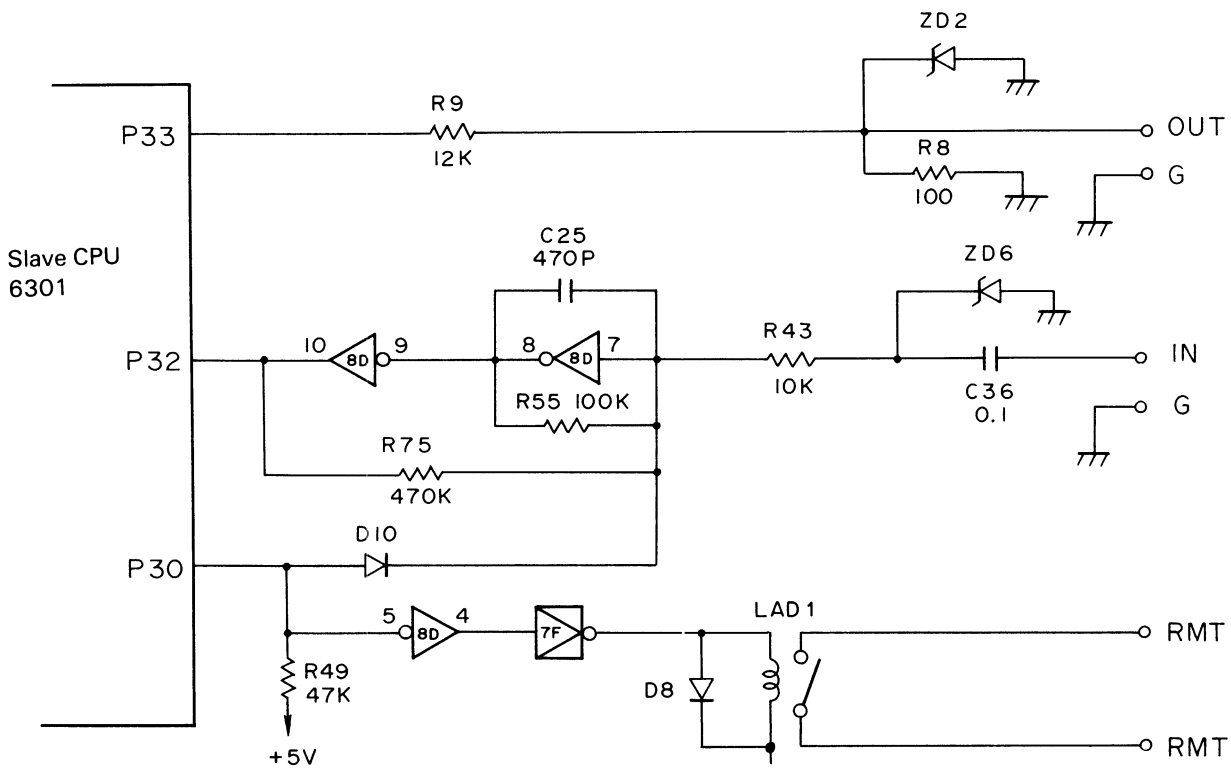


Fig. 3-110