HX-20

Technical Reference Manual

EPSON

H8294018-0
Y202990006

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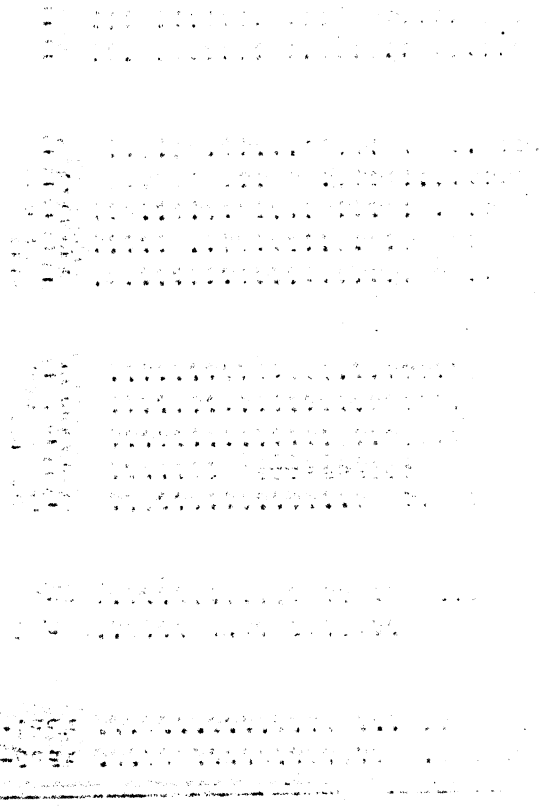
FOREWORD

This manual provides an outline of the HX-20 hardware configuration and explains the MONITOR program and its use. The information, drawings, diagrams and data contained in this manual are both accurate and reliable. However, the circuits related to the products not manufactured by EPSON, sample programs, etc. have been inserted merely to facilitate the understanding of the general applications of the HX-20, and thus they are not complete for practical use.

EPSON assumes no responsibility for the infringement of third party's patents resulting from the incorporation of or use of the EPSON HX-20, nor for the infringement of any other rights related thereto.



SECTION 1 HARDWARE

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CHAPTER 1 GENERAL

1.1 System Overview

The HX-20 is an all-in type computer which incorporates a liquid crystal display (LCD) and a microprinter in addition to other essential components. It was designed as a portable computer which operates on a built-in battery. As the HX-20 has a great choice of options, the HX-20 system can be configured or expanded with ease according to your specific application.

1.1.1 System configuration

The HX-20 incorporates the following standard equipment:

1 24-column microprinter
2 Liquid crystal display [20 characters x 4 lines (80 characters)]
3 Typewriter type keyboard (68 keys)
4 RS-232C interface
5 Serial interface
6 Cartridge (ROM or microcassette drive) interface
7 External audio cassette interface
8 Barcode reader interface
9 ROM (32K bytes)
10 RAM (16K bytes)

The HX-20 is thus capable of system configuration with expansibility as shown below.

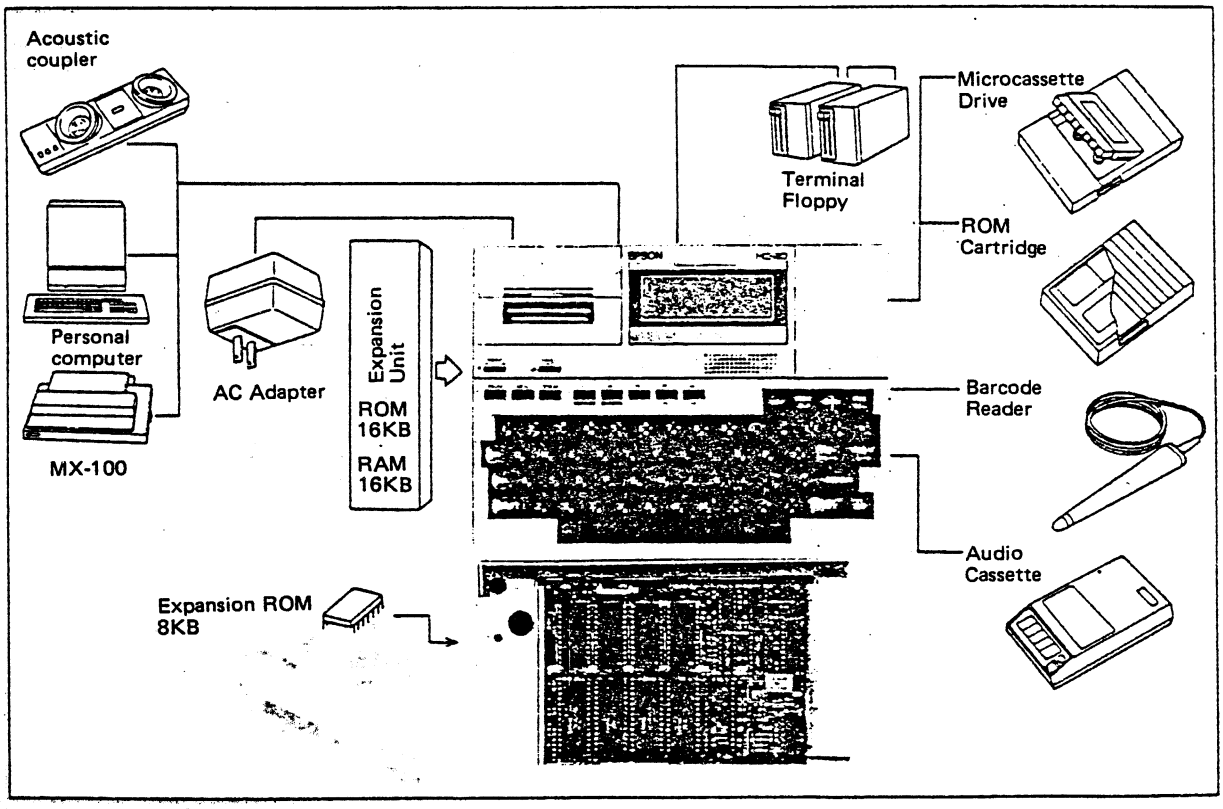


Fig. 1-1 System Configuration

Fig. 1-1 System Configuration

1.1.2 System block diagram

An (8K) ROM can be added to the internal 32K ROM of the HX-20. Other options, however, are connected to the HX-20 via the appropriate interface connectors located inside the portable computer as shown in Figs. 1-3 and 1-4 below.

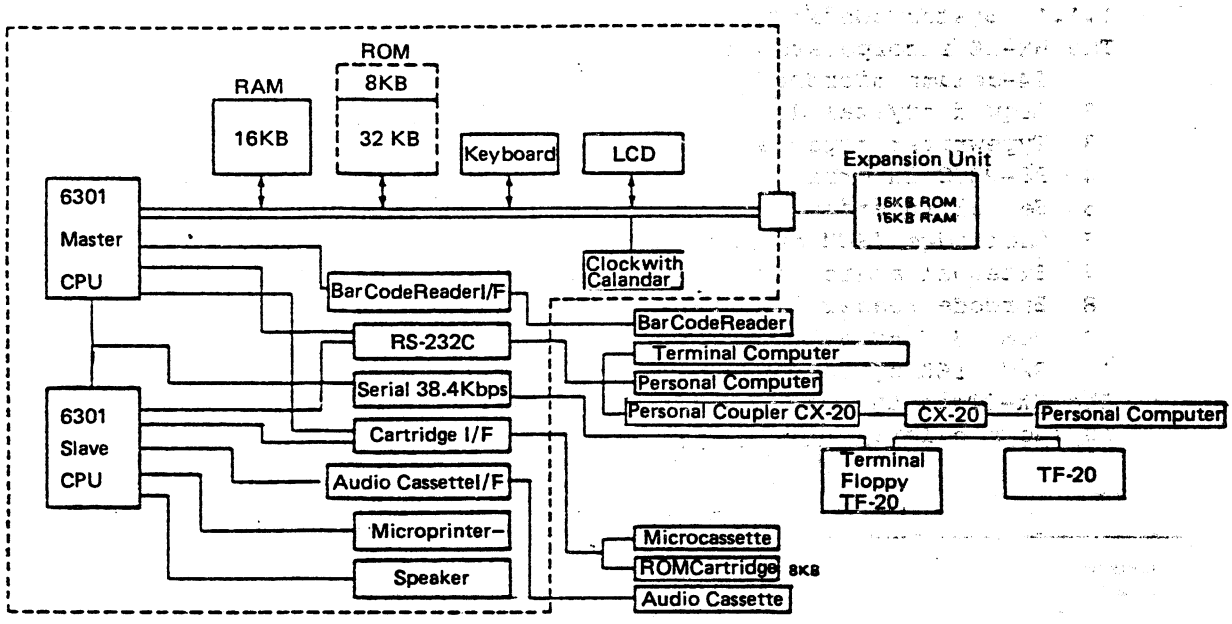


Fig. 1-2 System Block Diagram

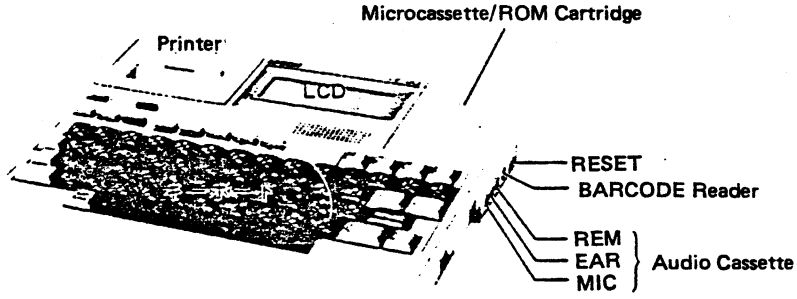


Fig. 1-3 Interface Connectors

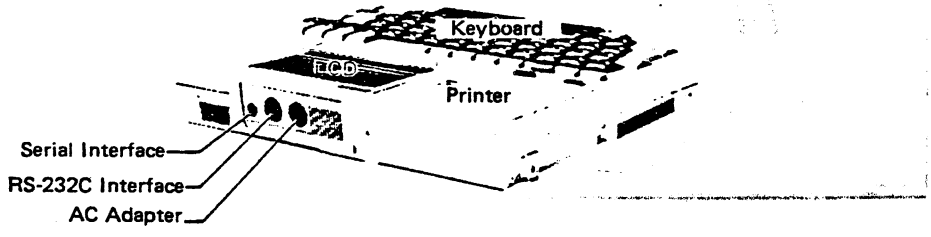


Fig. 1-4 Interface Connectors

1.1.3 Major components

The HX-20 consists of the following 7 major components:

1 MOSU control circuit board (MOSU board)
2 Keyboard unit
3 Liquid crystal display (LCD) panel
4 Microprinter
5 Ni-Cd battery
6 Speaker
7 Case

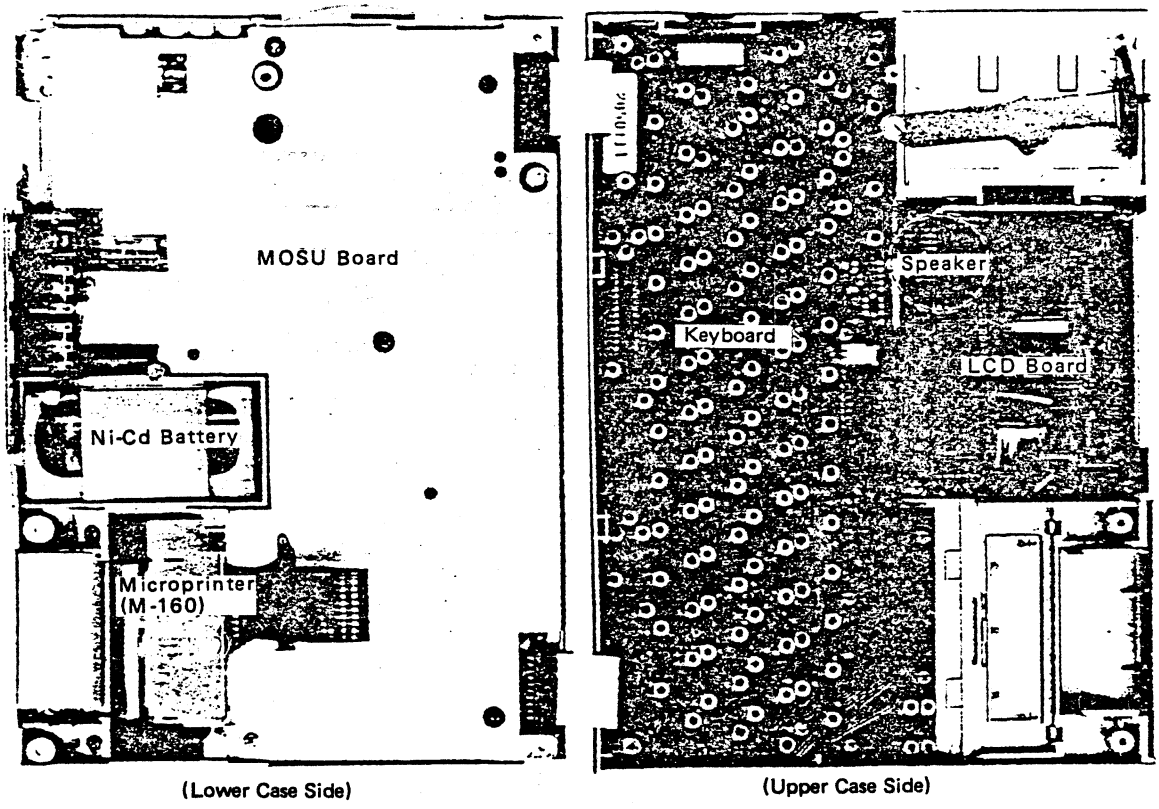


Fig. 1-5 Major Components

(1) On the MOSU board are mounted the connectors for various interfaces such as the RS-232C interface, the serial interface, the external audio cassette interface, the barcode reader interface, the expansion unit interface, and the optional cartridge interface and the AC adapter inlet. The HX-20 controls its components by a dual CPU system which employs two CMOS 6301 CPUs. This enables distributed processing of inputs and outputs and provides upgraded system performance.

(2) On the keyboard unit are mounted the power switch and the view angle control knob for the LCD. The LCD control circuit is located inside the keyboard unit.

1.1.4 Hardware configuration of HX-20

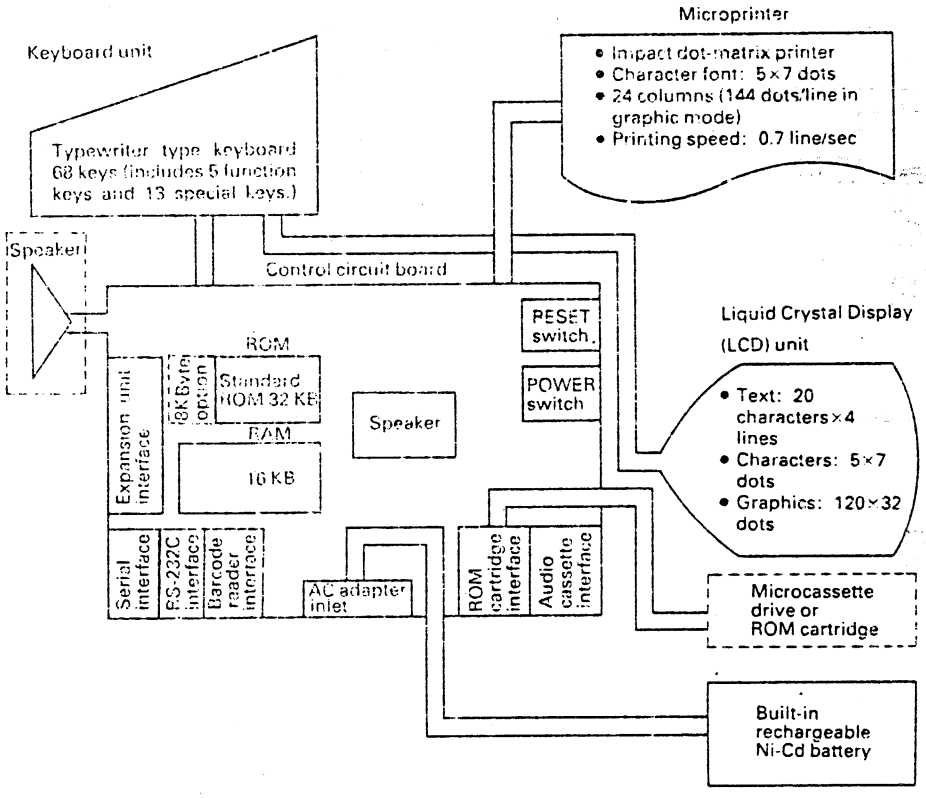


Fig. 1-6 Block Diagram of HX-20

The HX-20 comprises 6 major blocks as shown in the block diagram above; namely, an MOSU control circuit board, a keyboard unit, a microprinter, an LCD unit, a speaker, and a battery power supply. Each block is connected to the control circuit board and housed in the HX-20. A block diagram of the MOSU control circuit board is shown in Fig. 1-7 on the next page.

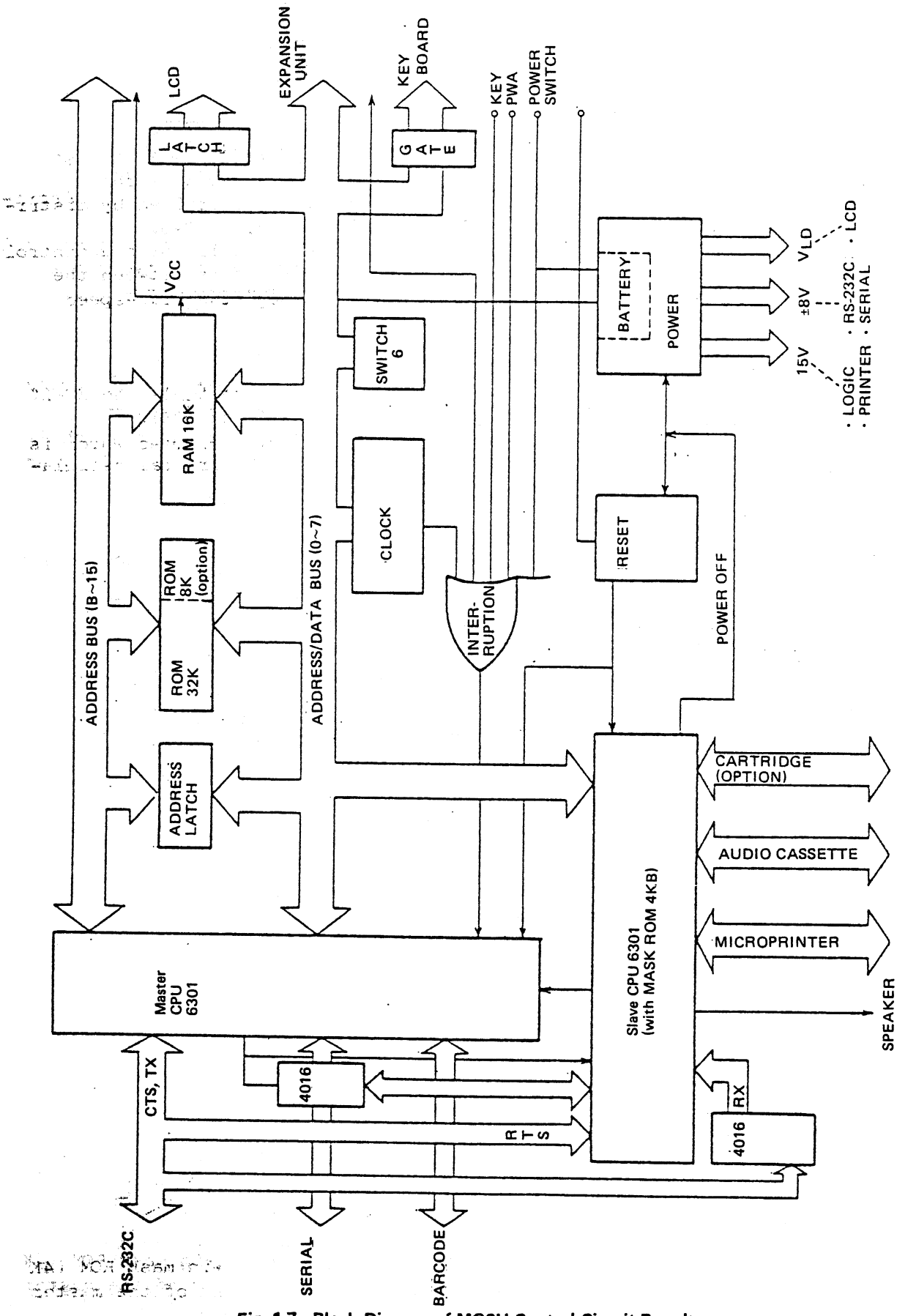


Fig. 1-7 Block Diagram of MOSU Control Circuit Board

1.1.5 MOSU board

The HX-20 adopts a dual CPU system which consists of two CMOS 6301 CPUs located on the MOSU board. Input/output units such as the microprinter, keyboard unit, LCD, etc., are thus controlled by distributed processing between the master CPU and the slave CPU.
Each CPU, the master and the slave, has its own oscillator and control program to control inputs and outputs. Data transfers between the master CPU and the slave CPU are performed through the high-speed serial interface (38,400 BPS).

(1) Master CPU 6301
The master CPU 6301 is a main processor which controls the HX-20 by the program stored in the external ROM (15E to 12E).
The system clock of the master CPU is approx. 1.63 μsec which is generated by an externally connected 2.4576 MHz crystal oscillator.
The master CPU mainly controls the following:
(a) Keyboard
(b) Liquid crystal display (the buffer for display is incorporated in the LCD control circuit board)
(c) Addressing of the built-in ROM and RAM
(d) Barcode reader
(e) Clock function
(f) Serial interface
Note: The master CPU does not use the built-in mask ROM.
The master CPU operates in Expanded Multiplex mode.

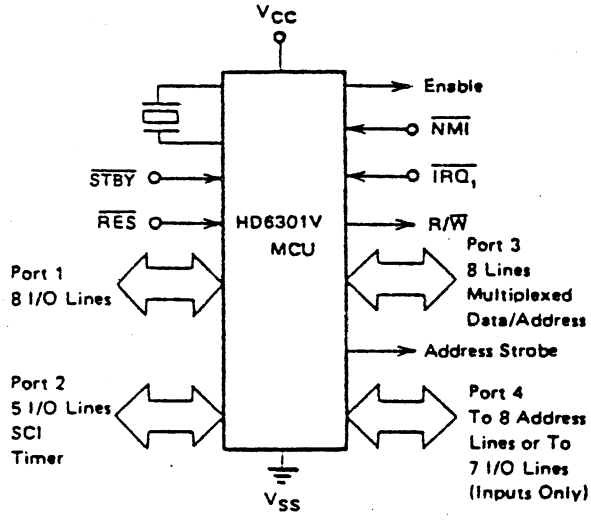


Fig. 1-8 Expanded Multiplex Mode of HD6301V MCU

(2) Slave CPU
The slave CPU has a control program in the built-in mask ROM (4K bytes) and controls input/output units independent of the master CPU.
The slave CPU mainly controls the following:
(a) External audio cassette
(b) Microprinter (M-160)

(c) Barcode reader
(d) RS-232C interface
(e) Optional cartridge (ROM or microcassette drive)
(f) Power ON/OFF

The system clock of the slave CPU is approx. 1.63 μsec. The slave CPU operates in Single Chip Mode:

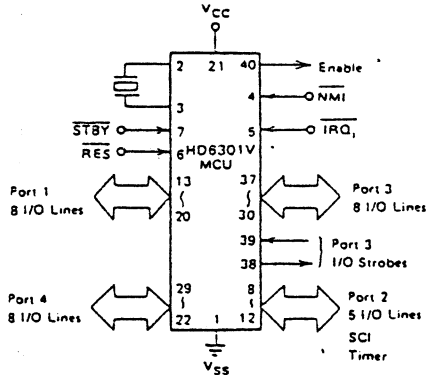


Fig. 1-9 Single Chip Mode of HD6301V MCU

(3) Power Supply Unit

The power supply unit consists of a charging circuit with built-in battery and the AC adapter, a voltage detection circuit, an LCD voltage circuit, an RS-232C voltage circuit, and a backup circuit, all designed to minimize power consumption.

(a) Fuse: 5A fuse for protection against faults by overcurrent.
(b) Charging circuit: This circuit consists of a noise filter, a diode for reverse current protection and a resistor. A zener diode is also connected to the output side of the fuse circuit for overvoltage protection.
(c) Voltage detection circuit: Normally, this circuit monitors the battery voltage after the power has been turned on. When the battery voltage falls below 4.5 volts the circuit outputs a POWER ABNORMAL signal to notify the master CPU of the low voltage condition.
(d) LCD voltage circuit: This circuit generates approx. +7V by DC-DC conversion of the battery voltage to drive the liquid crystal display.
(e) RS-232C voltage circuit: This circuit generates approx. $\pm$8V from the battery voltage which meet the voltage requirements of the EIA Interface Standard RS-232C. This circuit is designed so that $\pm$8V is output only when the RS-232C interface is used. Power on/off control of the circuit is performed by the slave CPU.
(f) Backup circuit: This circuit supplies from the built-in battery, the minimum current required to operate the clock and the components to be used when power is turned on, and also protects the data stored in the RAM while the power switch is being turned off.

(4) Clock

The HX-20 employs a real-time clock (146818RTC) which has clock and calendar functions and is connected directly to the master CPU through the data bus. It uses a 32.768 KHz oscillator as the basic clock.

(5) RAMs

The HX-20 incorporates a total of 8 CMOS RAM chips each with a capacity of 16,384 bits. (2K bytes). The total RAM capacity is thus 16K bytes. The RAMs are backed up by the built-in battery for data retention even when the power is turned OFF.

(6) ROMs

The HX-20 incorporates 4 8K-byte mask ROM chips. The ROM chips contain the BASIC interpreter, OS (Operating System) and machine language monitor.

(7) Switch (SW6)

A 4-pin DIP switch is mounted on the control circuit board. Pin Nos. 1 to 3 are used for selecting character sets. Pin No. 4 is used to specify whether or not the terminal floppy unit is connected (ON: connected, OFF: not connected).

(8) Interrupts

There are two types of interrupts: NMI (non-maskable interrupts) and IRQ (Interrupt request). The NMI interrupts are not used. An IRQ is generated under one of the following conditions.

(a) Keyboard input
(b) Low voltage detection (PWA)
(c) Power switch (PWSW)
(d) External interrupt (INT EXT)
(e) Clock interrupt

(9) System Bus

The system bus consists of an address bus and a data bus. The address bus consists of 16 address lines (0 ~ 15) and a maximum of 64K bytes of addresses are thus accessible directly. Since the 8 low-order address lines (0 ~ 7) are also used as data lines, an address latch is provided to switch between the address and data buses by the appropriate timing.

(10) RS-232C Interface

The USART (Universal Synchronous/Asynchronous Receiver/Transmitter) IC's (75188 and 75189) are used for the RS-232C interface. +8V and -8V are used as the signal levels of the RS-232C interface. The operation of the interface is controlled by both the master CPU and the slave CPU. Through this interface, data can be transferred at bit rates ranging from 110 BPS to 4,800 BPS.

(11) Serial Interface

The Serial Communication Interface (SCI) is used to connect the master CPU with the slave CPU. Interfacing between the master CPU and the slave CPU or between the master CPU and an external unit is switched under software control.
Through the serial interface, data can be transferred at bit rates ranging from 38,400 BPS to 150 BPS.
The operation of this interface is controlled by the master CPU.
The serial interface is not supported by BASIC.

(12) Connector Locations

There are 12 connectors in the HX-20: 9 on the MOSU board 2 on the keyboard, and 1 at the optional cartridge section. The location and description of each connector is given in the figure and table below.

Table 1-1 Connectors on the MOSU Board

Connector	No. of pins	Connection
CN1	5	Serial interface
CN2	8	RS-232C
CN3	2	AC adapter
CN4	20	Keyboard
CN5	20	Keyboard
CN6	20	Microprinter
CN7	40	Expansion unit
CN8	14	Optional cartridge
CN9	2	Built-in battery

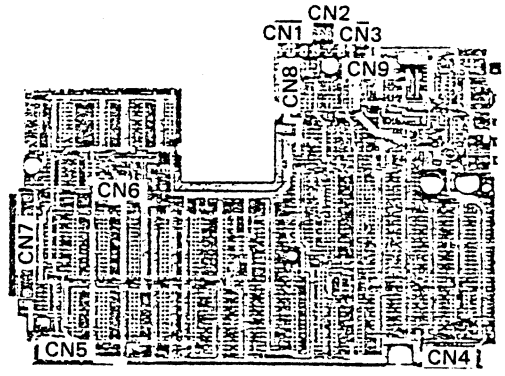


Fig. 1-10 Rear View of MOSU Board

1.2 Input/Output Interfaces

1.2.1 Interface control

The input/output interfaces are controlled by the master CPU and the slave CPU as shown in Fig. 1-11.

(1) Control by the master CPU: LCD and keyboard

(2) Control by the slave CPU: Speaker, external audio cassette and M-160 microprinter

(3) Control by both CPUs: High-speed serial interface, RS-232C interface, cartridge interface (option) and barcode reader interface

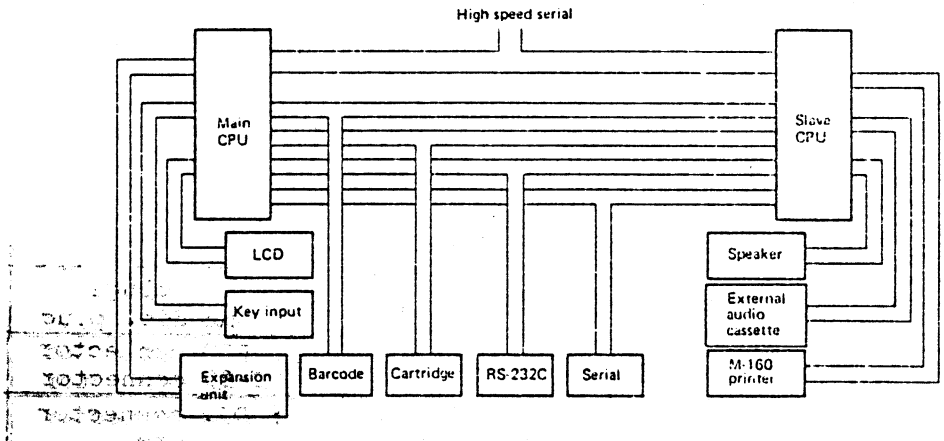


Fig. 1-11 Relationship between CPUs and I/O Operations

The following 6 interfaces are open to external units.

Table 1-2 External Interfaces

Interface	Connector Type	Specification of Connector	No. of Signal Lines (including Voltage and GND Lines
Barcode Reader	Jack 3.50 (x1) 3-position		3
Optional cartridge	Plug-in connector		14
RS-232C	8-pin DIN	TCS4480	8
Serial	5-pin DIN	TCS4450	5
External Audio Cassette	Jack 3.50 (x2) 2.50 (x1)		6
Expansion Unit	F/C		40

1.2.2 Interface cables

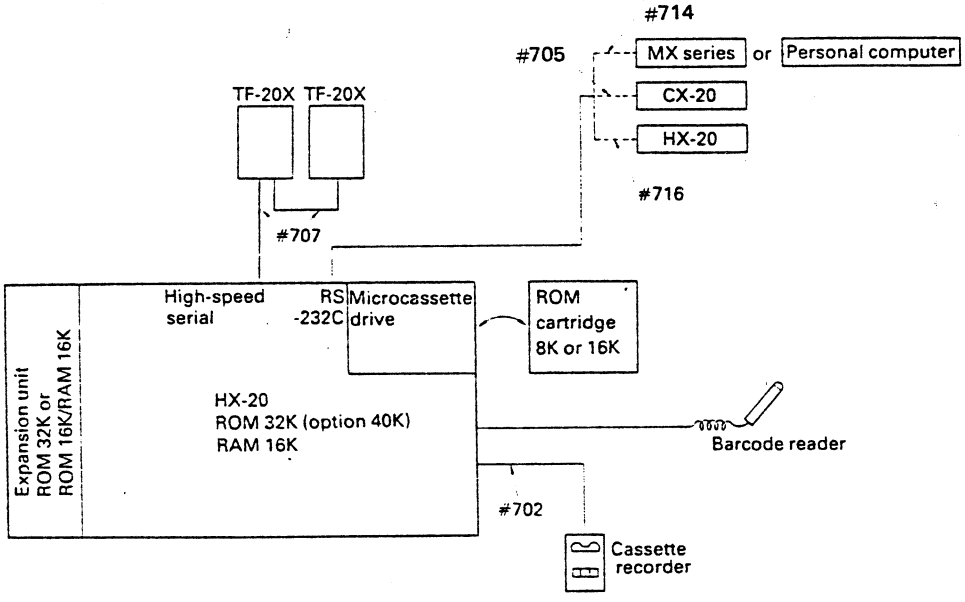


Fig. 1-12 Cable Connection Diagram

Table 1-3 Interface Cables

Cable Set Number	Connection between	Part Number	Connector
#702	HX-20 and External audio cassette	Y201302000	Two 3.5mm dia. plugs and one 2.5mm dia. plug
#705	HX-20 and acoustic coupler	Y201305000	One 8-pin DIN connector and one DB-25 connector
#707	HX-20 and TF-20	Y201307000	One 5-pin DIN connector and one 6-pin DIN connector
#714	HX-20 and Terminal printer (MX series)	Y201309000	One 8-pin DIN connector and one DB-25 connector
#716	HX-20 and HX-20	Y201311000	Two 8-pin DIN connectors

(1) Cable Set #702 (with two 2.5mm dia. jack adapters)

(a) Use: To connect the HX-20 to an external cassette tape recorder

(b) Plugs: 3.5mm dia. (white and red), and 2.5mm dia. (black)

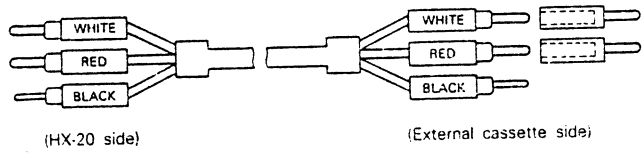


Fig. 1-13

(c) Connection

Connect the HX-20 to the external cassette tape recorder as shown below.

If the diameter of the input jack of the external audio cassette is 2.5mm, connect the plugs using the supplied jack adapter.

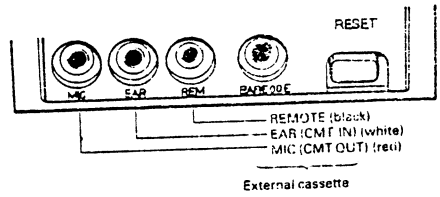


Fig. 1-14

(d) Signal names

Color	Pin No.	Signal Name
Black	1	Shield
	2	Input
Red	1	Shield
	2	Output
Black	1	Remote
	2	Remote

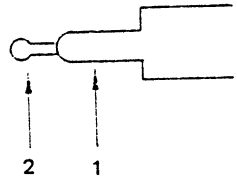


Fig. 1-15

(2) Cable Set #705

(a) Use: To connect the HX-20 to the acoustic coupler.

(b) Connectors:
HX-20 side: 8-pin DIN connector
Coupler side: DB-25 connector (male)

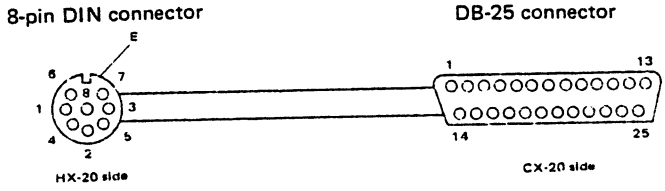


Fig. 1-16

(c) Connection

Plug the DIN connector into the RS-232C interface connector on the rear panel of the HX-20 and the DB-25 connector into the CX-20 interface connector. Then, tighten the two mounting screws with a screwdriver to secure the DB-25 connector to the CX-20.

Fig. 1-17

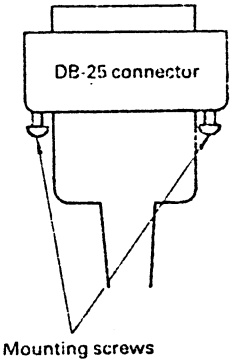


Fig. 1-18

(d) Signal names

8-Pin DIN Connector

Pin No.	Signal Name	Color
1	GND	Black
2	TX	Red
3	RX	Gray
4	RTS	Yellow
5	CTS	Green
6	DSR	Brown
7	DTR	Blue
8	CD	White
E	FG (CG)	(Shield)

DB-25 Connector

Pin No.	Signal Name	Color
1	CG	(Shield)
2	TX	Red
3	RX	Gray
4	RTS	Yellow
5	CTS	Green
6	DSR	Brown
7	GND	Black
8	CD	White
9-19	Unused	-
20	DTR	Blue
21-25	Unused	-

(3) Cable Set #707

(a) Use: To connect the HX-20 to the floppy disk unit.

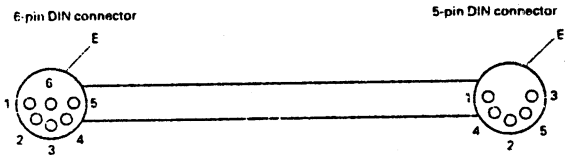
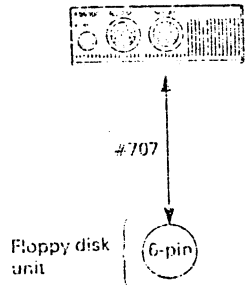


Fig. 1-19

(b) Connectors:

HX-20	Floppy disk unit
(5-pin DIN)	(6-pin DIN)



(c) Connection

Plug the DIN connectors on both sides into the corresponding interface connectors.

Fig. 1-20

(d) Signal names

6-Pin DIN connector

Pin No.	Signal Name	Color
1	PRX	White
2	PIN	Green
3	PTX	Red
4	POUT	Yellow
5	SG (Signal Ground)	Black
6	Unused	-
E	FG (CG)	(Shield)

5-Pin DIN connector

Pin No.	Signal Name	Color
1	SG (Signal Ground)	Black
2	PTX	Red
3	PRX	White
4	POUT	Yellow
5	PIN	Green
E	FG (CG)	(Shield)

(4) Cable Set #714

(a) Use: To connect the HX-20 to the MX-series terminal printer.

(b) Connectors
HX-20 side: 8-pin DIN connector
Printer side: DB-25 connector (male)

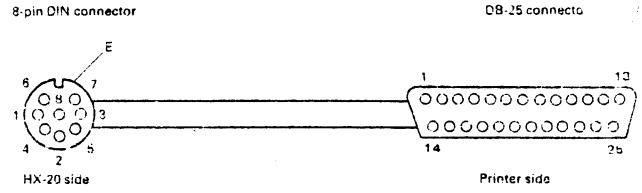


Fig. 1-21

(c) Connection
Plug the DIN connector into the RS-232C interface connector and the DB-25 connector into the interface connector of the terminal printer.

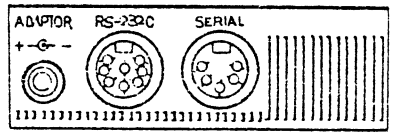


Fig. 1-22

(d) Signal names

8-Pin DIN

Pin No.	Signal Name	Color
1	SG (Signal Ground)	Black
2	$\overline{TX}$	Red
3	$\overline{RX}$	White
4	RTS	Brown
5	CTS	Brown
6	DSR	Yellow
7	DTR	Green
8	CD	Blue
E	CG	(Shield)

DB-25 Connector

Pin No.	Signal Name	Color
1	CG	(Shield)
2	$\overline{TX}$	White
3	$\overline{RX}$	Red
4	Not used	Blue
5	Not used	Blue
6	DSR	Green
7	SG (Signal Ground)	Black
8	Unused	Brown
9-19	Unused	-
20	DTR	Yellow
21-25	Unused	-

NOTE: Pin Nos. 4 and 5 are connected within each connector and then connected to the pin No. 8 of the mating connectors.

(5) Cable Set #716

(a) Use: To connect two HX-20 units through the RS-232C interface.

(b) Connectors: Two 8-pin DIN connectors

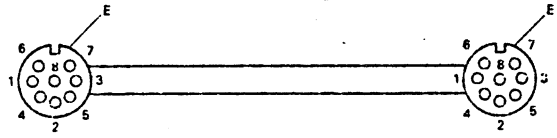


Fig. 1-23

(c) Connection

Plug the DIN connector into the RS-232C interface connector on the rear panel of each HX-20 unit.

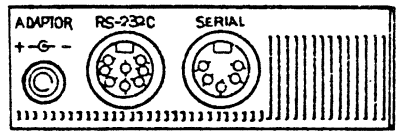


Fig. 1-24

(d) Signal Names

Pin No.	Signal Name	Color
1	SG (Signal Ground)	Black
2	TXD	Red
3	RXD	White
4	RTS	Brown
5	CTS	Brown
6	DSR	Yellow
7	DTR	Green
8	CD	Blue
E	FG (CG)	(Shield)

Pin No.	Signal Name	Color
1	SG (Signal Ground)	Black
2	TXD	White
3	RXD	Red
4	RTS	Blue
5	CTS	Blue
6	DSR	Green
7	DTR	Yellow
8	CD	Brown
E	FG (CG)	(Shield)

Note: Pin Nos. 4 and 5 are connected within each connector and then connected to the pin No. 8 of the mating connectors.

CHAPTER 2 PRINCIPLE OF OPERATION

2.1 Power Supplies

The power supply circuit of the HX-20 is located in the MOSU board. From the battery voltage this circuit generates all the voltages required for various operations in the HX-20.

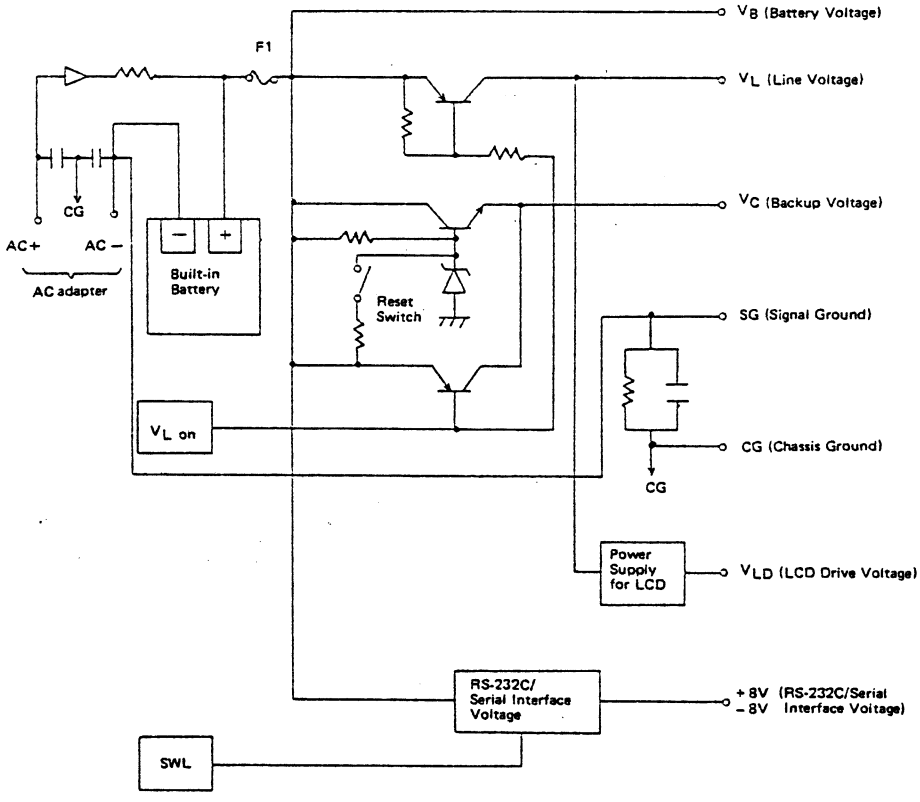


Fig. 2-1 Power Supply Circuit

Table 2-1 Output Voltages

Name	Description	Use
V_B	Output voltage of built-in battery (positive terminal of the built-in battery).	Power supply for built-in printer, expansion unit, V_L, V_C, or ±8V.
V_L	Line voltage. This voltage is generated from V_B when the power switch is turned on.	Voltage for circuit elements or barcode reader.
V_C	Backup voltage. Approx. 3V when the power is turned off and approx. 4.5V when the power is turned on.	Power supply for CMOS RAM, power ON/OFF circuit or reset circuit.
V_{LD}	LCD drive voltage. Approx. 7V is generated from VL when the power switch is turned on.	Power supply for LCD panel
+8V -8V	RS-232C level voltage (-3 to -27V, +3 to +27V). Voltage output starts upon input of an SWL signal.	Power supply for RS-232C or high-speed serial interface.
SG	Signal ground (negative terminal of the built-in battery).	
CG	Protective ground.	

2.1.1 Output voltages

(1) Built-In Battery (SUB C Type)
This battery is a rechargable type battery which is used within a range of 6.0V to 4.0V. The effective output capacity is approximately 1,100 mAH.

(2) V_B (Battery Voltage)
Voltage V_B is a battery voltage which is supplied from the built-in battery via fuse F1 and serves as the power supply for the various voltages to be used within the HX-20. When using the HX-20 with an external interface, this voltage can be output at up to 1.0A.

(3) V_L (Line Voltage)
Voltage V_L is supplied from V_B through the internal transistor Q8 (2SB808G) which is turned on when the power is turned on.
This voltage is used by all the circuit elements except the backed-up elements listed in Table 2-2 below.
When using the HX-20 with an external interface, this voltage can be output at up to 50mA.

(4) V_C (Backup Voltage)
Voltage V_C is used to protect the data stored in the RAM when the power is turned off and to keep the reset circuit in the operating state when the power is turned on.
Approx. 3V is supplied as V_C from V_B through transistor Q7 (2SA1048), when the power is turned off, and approx. 4.5V when the power is turned on.
When using the HX-20 with an external interface, this voltage can be output at up to 40mA.

Table 2-2 Elements Backed Up by V_C

Location	In type	Use
4F	TC40H002	Reset and Enable
5D	TC40H000	RAM R/W and CE
5E	TC40H004	Interrupt circuit
5F	TC4011UBP	Clock and reset circuits
13C~16C	HM6117	2K RAM x 4
12G~15G	HM6117	2K RAM x 4
16D	TC40H138	CE2 output for RAM
6G	HD146818	Real-time clock

(5) V_{LD} (LCD Drive Voltage)
Voltage V_{LD} is generated from line voltage V_L when the power is turned on.

(6) +8V, -8V (RS-232C/Serial Interface Voltage)
This voltage is activated by the slave CPU only when the RS-232C or serial interface (external interface) is to be operated.

2.1.2 Low voltage detection circuit

After the power switch has been turned on, the voltage detecting comparator operates to constantly check the built-in battery for proper voltage while the power switch is in the ON state.

This circuit prevents the HX-20 from operating abnormaly due to a decrease in the battery voltage. When the battery voltage drops below 4.5V, the low voltage detection circuit is activated and an interrupt is applied to the master CPU by an IRQ.

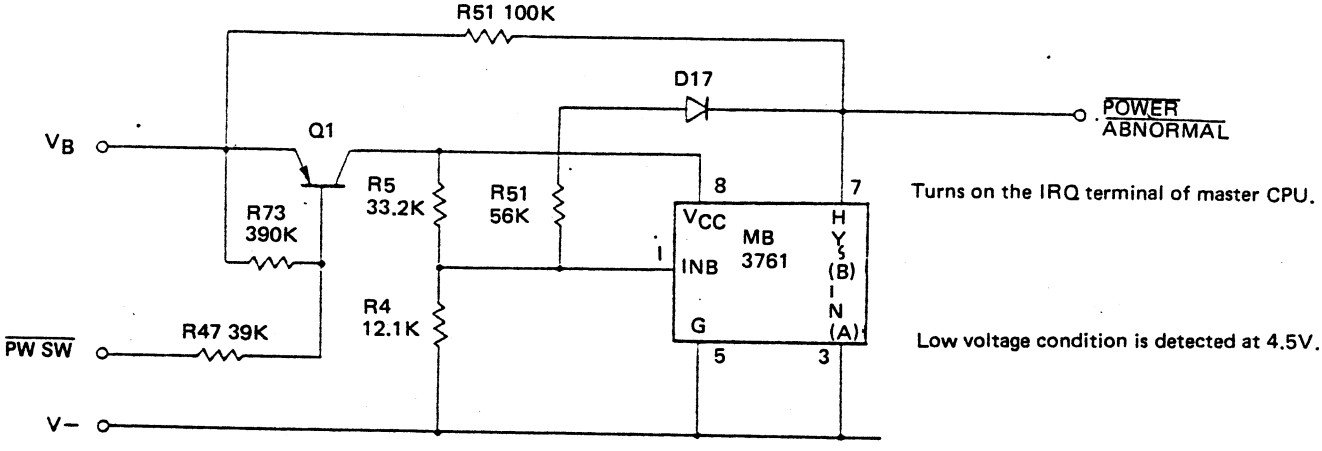


Fig. 2-2 Low Voltage Detection Circuit

2.1.3 Reset circuit

The reset circuit functions to prevent the respective circuit elements (master CPU, etc.) from overruning when power is applied to the HX-20, as well as to initialize the respective circuit elements while the reset circuit is operating.

The reset circuit operates only under the following conditions.

(1) When power is applied.
A $\overline{\text{RESET}}$ signal is output for approx. 30msec after the power switch has been turned on.

(2) When the Reset Switch is pressed.
A $\overline{\text{RESET}}$ signal is output for approx. 30msec while the Reset switch is being pressed and after it has been released.

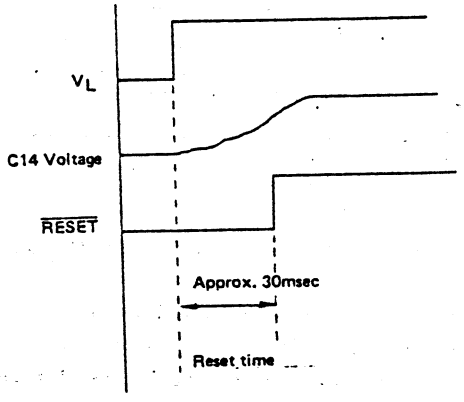


Fig. 2-3 Reset Timing

2.2 CPU Operation

2.2.1 Master CPU and slave CPU

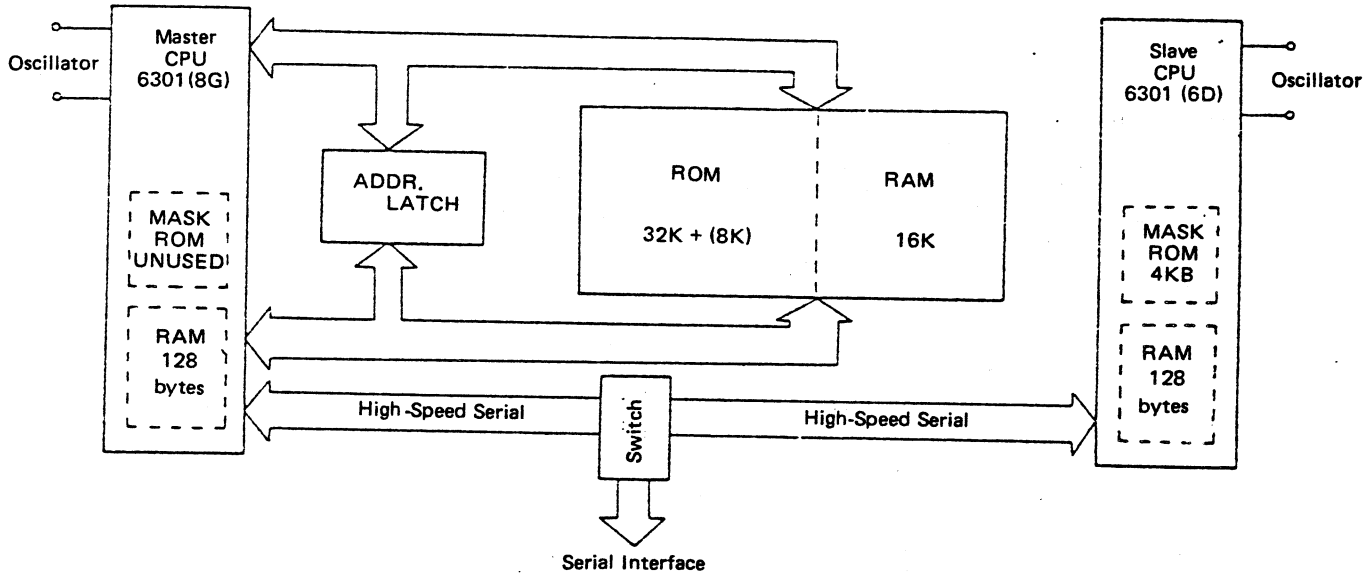


Fig. 2-4 CPU Operation

The HX-20 adopts a dual CPU system in which two 6301 CPUs are used to permit the distributed processing of inputs/outputs.

The master CPU is operated by a control program which is stored in an external ROM. The master CPU controls: (1) keyboard, (2) LCD, (3) ROM/RAM addressing, (4) barcode reader, (5) clock function, etc. The master CPU does not use the built-in mask ROM, but it only uses the program contained in the external ROM to perform the various controls described above.

The slave CPU has a control program in the built-in mask ROM (4KB). The slave CPU operates independently of the master CPU to control: (1) external audio cassette, (2) microprinter, (3) barcode reader, (4) RS-232C interface, (5) high-speed serial interface, (6) optional cartridge, (7) power off, etc. Connected to the master CPU via the high-speed 38,400 BPS serial interface, the slave CPU transmits and receives commands and data which are necessary in performing its control functions.

2.2.2 Operation modes (Memory Allocation)

The operation mode of each CPU must be set by hardware. For this reason, the operation mode of the CPU cannot be changed by software. The operation mode of each CPU is determined by the logic level (high or low) of each signal input to the pin Nos. 8, 9 and 10 of the CPU. The addresses of these pin numbers correspond to the bits 5, 6 and 7 of internal register 0003.

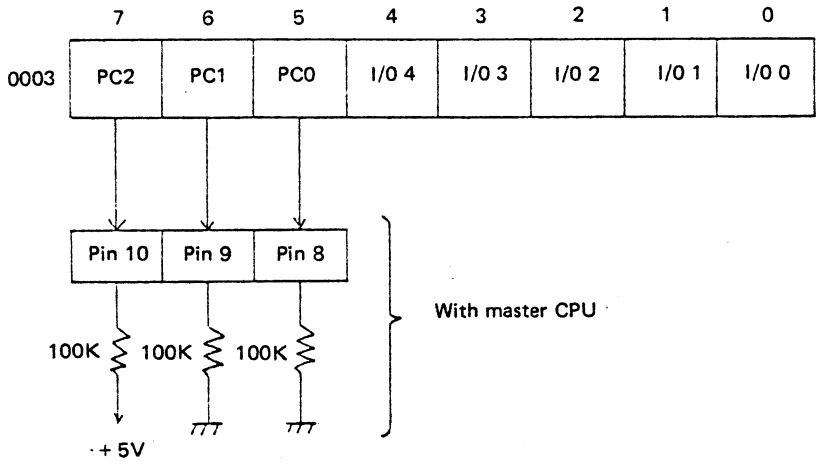


Fig. 2-5 Operation Mode

Notes:

1. Since the master CPU is connected so that pin Nos. 8 and 9 become low and pin No. 10 becomes high, it operates in Mode 4, i.e., Multiplexed/RAM mode.
2. With the slave CPU, pin Nos. 8, 9 and 10 are all connected to +5V through a 100 KΩ resistor. The slave CPU thus operates in Mode 7, i.e., Single Chip mode.

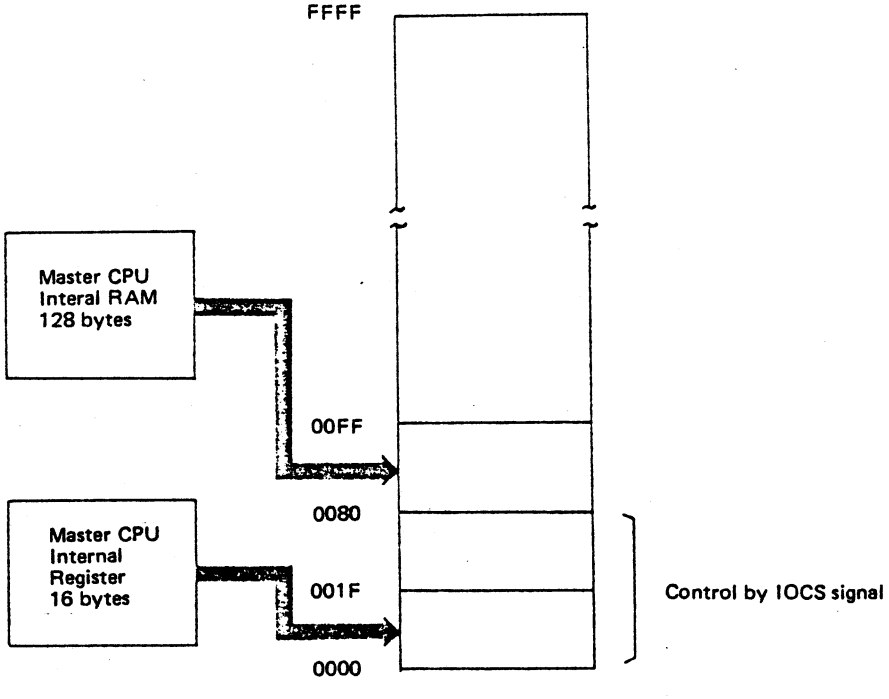
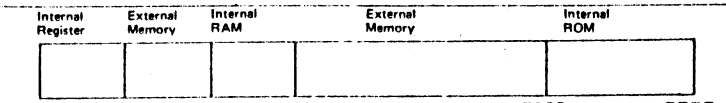
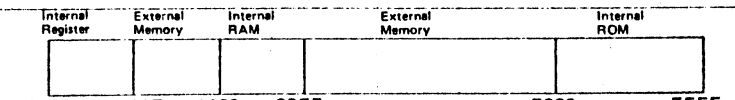
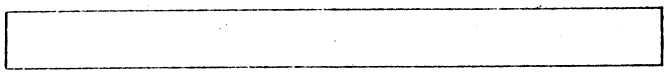
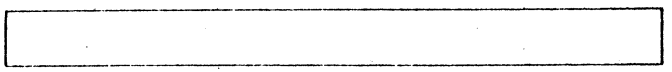
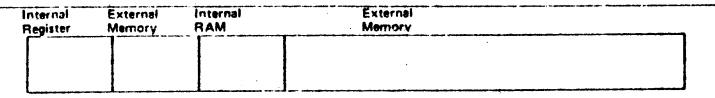
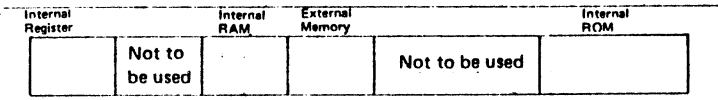
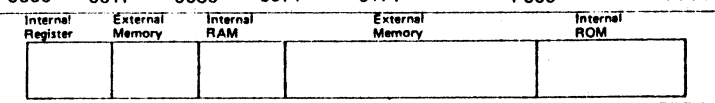
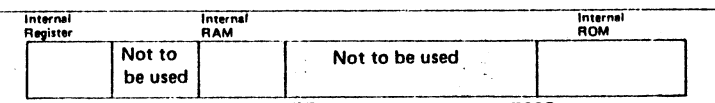


Fig. 2-6 Memory Map of Master CPU (Multiplexed/RAM Mode 4)

Table 2-3 Operation Modes

Mode	Port			ROM	RAM	Interrupt Vector	Operation Mode	Memory Map	
0	L	L	L	Internal	Internal	Internal (external for 3 cycles after RES goes high)	MULTIPLEXED TEST		This mode is used for testing only. • Does not include addresses 04, 05, 06, 07, and 0F which can be used externally. • Must be free of any overlapped area in internal and external memory spaces.
1	H	L	L	Internal	Internal	Internal	NON-MULTIPLEXED/PARTIAL DECODE		Does not include addresses 00, 02, 04, 06, and 0F which can be used externally.
2	L	H	L	–	–	–	UNUSED		
3	H	H	L	–	–	–	UNUSED		
4	L	L	H	External	Internal	External	MULTIPLEXED/RAM		Does not include addresses 04, 05, 06, 07, and 0F which can be used externally.
5	H	L	H	Internal	Internal	Internal	NON-MULTIPLEXED/PARTIAL DECODE		Does not include addresses 04, 06, and 0F (cannot be used externally).
6	L	H	H	Internal	Internal	Internal	MULTIPLEXED/PARTIAL DECODE		Does not include addresses 04, 05, and 0F which can be used externally.
7	H	H	H	Internal	Internal	Internal	SINGLE CHIP		

2.2.3 Operation timing
The operation timing of the CPU is outlined in Fig. 2-7. For details, see Appendix on "6301V".

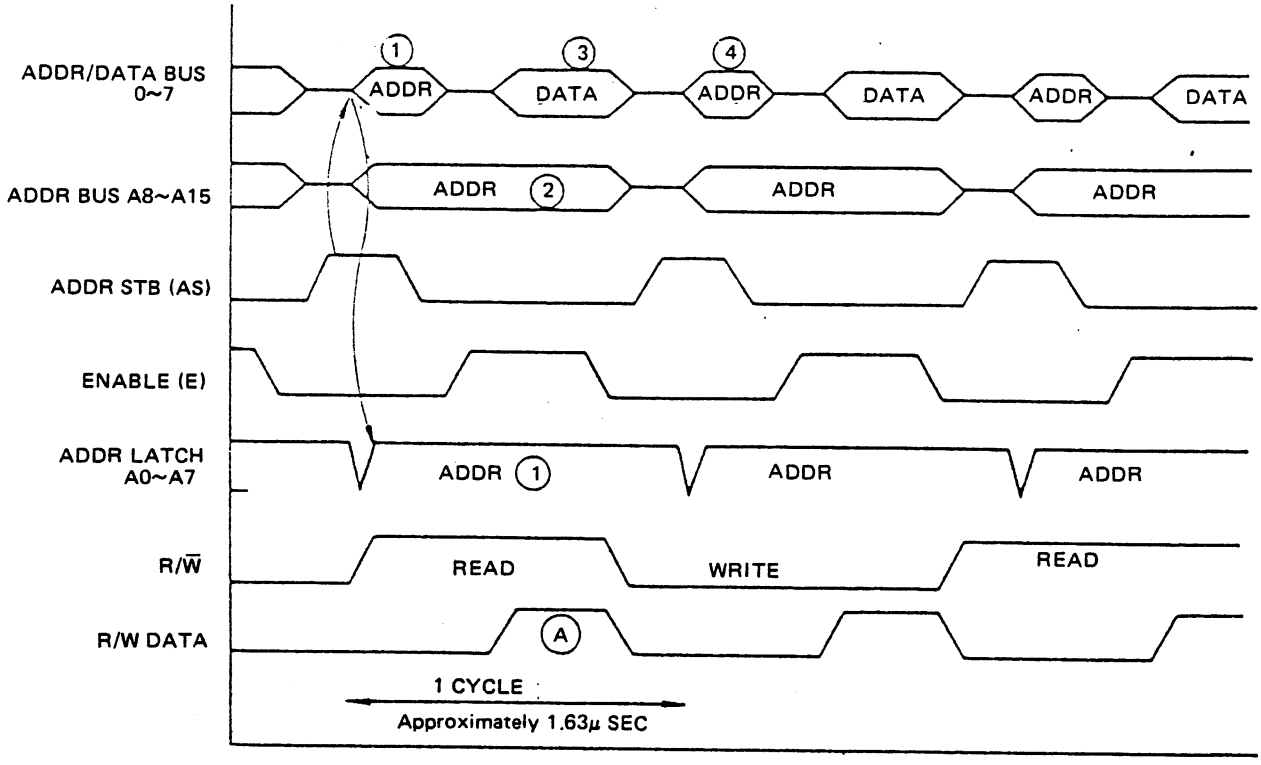


Fig. 2-7 Operation Timing

As an external oscillator is connected to the pin Nos. 2 and 3 of each CPU, the clock frequency (2.4576MHz) obtained from this external oscillator is divided by 4 in the CPU to generate a system clock of approx 1.63μsec. During a read cycle, when address 1 is output to the address/data bus following the output of ADDRESS STROBE signal (AS), the contents of that address are held in the address latch until address 4 is output. When the next address 2 is output, the address of a required data in the ROM will be specified. By outputting ENABLE signal (E) at this point, one byte of data (program) A in the ROM is output on the data bus, which can then be fetched into the 6301 CPU.

To write data, the RAM address must at first be specified in the same way as a data read. Then, if data is output with R/W signal held at Low level, the data can be written into the specified I/O or RAM.

The master CPU has 16 address lines (DA0~A15) and 8 data lines (DA0~DA7). It can thus directly address up to 64K bytes of memory locations. The bus lines are connected to the CPUs and ROM as described in the following section.

2.3 Address Control

2.3.1 Memory addressing

The internal RAM can be addressed by the CE2 (Chip Enable) signal which is output from IC "16D", the address lines (A0~A10: max. 2K bytes can be used) supplied to each RAM chip and CE1 signal. The external RAM can also be addressed by using address lines A0~15 (a maximum of 64K bytes can be used). However, the HX-20 has another RAM or buffer (for master CPU, real-time clock IC146818, LCD μPD7227), which uses the same addresses as the external RAM. For this reason, control signals are required to indicate which RAM is to be used, external or internal.

2.3.2 Address control signals

(1) The basic control signal is an IOCS signal, which must be output to the pin No. 8 of IC "2E". The $\overline{\text{IOCS}}$ signal is output when the address lines used are $\overline{\text{A7}}$ to $\overline{\text{A15}}$. When the signal is output, it indicates that addresses 0000 to 007F are specified.

(2) Auxiliary control signals include IC "9E" and associated I/O address control signals.

(3) Address control CPU

(a) With master CPU

The internal RAM or external RAM of the CPU is controlled by the bit 6 (address 0014) of the RAM control register located in the master CPU. When bit 6 is on, the internal RAM is selected. In this case, the master CPU performs neither data write nor read to or from the external RAM.

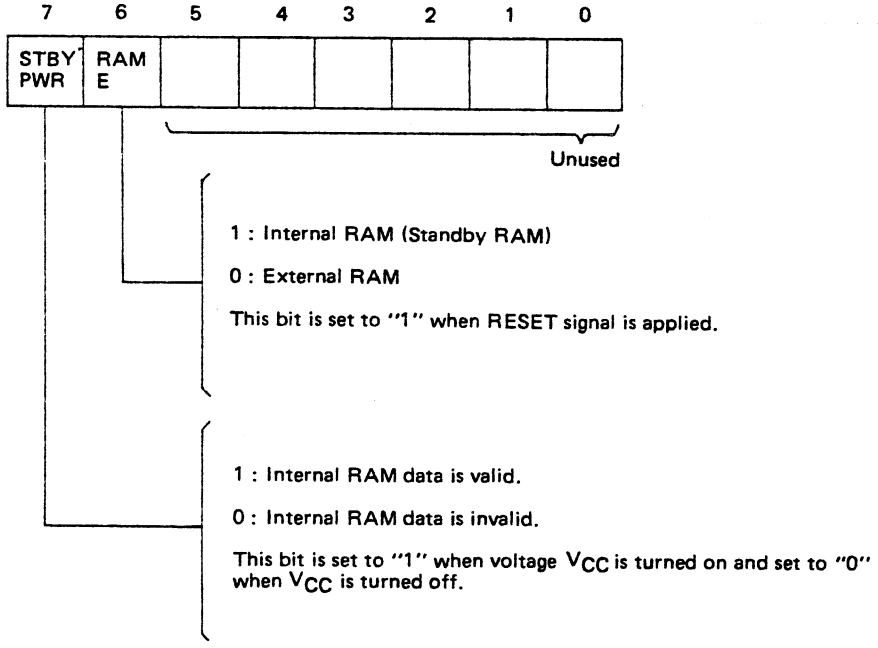


Fig. 2-8 RAM Control Register

(b) With internal RAM or expansion RAM

When IOCS ($\overline{\text{A7}}$~$\overline{\text{A15}}$) is output, it is supplied to the pin No. 9 of IC "4E" and then its inverted signal is output to the pin

No. 8. At this point, under the condition $\overline{A11}$~$\overline{A15}$, the pin No. 15 of IC "16D" for RAM Chip Select is set at Low level, but the pin No. 11 of IC "4F" is set at High level (i.e., the ON state of $\overline{IOCS}$). Therefore, the pin No. 13 goes low and the pin No. 4 of IC "5E" goes high. As a result, the CE2 terminal of RAM "13C" will not be activated and the RAM cannot be specified.

Since the IOCS signal is also supplied from connector CN7 to the expansion unit, the built-in RAM is protected from being specified erroneously.

For the above reasons, addresses 0000 to 007F indicate the RAM in the CPU, LCD buffers, or the built-in RAM for the real-time clock.

(c) With LCD buffers

The LCD has a total of 6 buffers (for 480 bytes), each of which is specified by addresses 0000 to 00F4 (80 bytes). However, these addresses are designated by setting the data pointer (of 7-bit configuration) within the LCD using the CID (LOAD IMMEDIATE TO DATA POINTER) command. Since each of the six 80-byte buffers is specified by the CS (Ship Select) signal, the master CPU does not address the LCD buffers directly. For this reason, addressing of the LCD buffers is done by the master CPU using only two addresses "0026" and "002A" as the LCD addresses, as shown in Fig. 2-9.

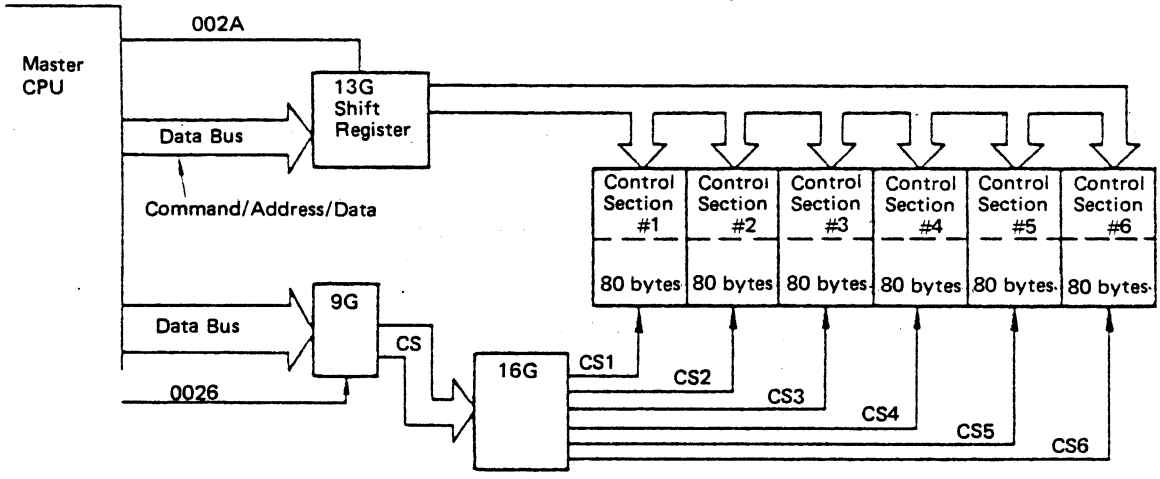


Fig. 2-9 Addressing of LCD Buffers

(d) With Clock RAM

Accessing the clock RAM is controlled by the pin No. 13 (E) of IC "6G", to which a control signal is supplied via the pin No. 8 of IC "1E", pin No. 1 of IC "4F", and pin No. 8 of IC "5E" only when both $\overline{IOCS}$ ($\overline{A7}$~$\overline{15}$) signal and DA6 signal (address 0040 or greater) are ON. Here, the addresses of the clock RAM are 0040 to 007F. Therefore, while this address space is being selected, the pin No. 13 of IC "6G" is at Low level, thus enabling the read/write of the clock RAM.

Bit / Address	7	6	5	4	3	2	1	0
XX40	0	1	0	0	0	0	0	0
XX7F	0	1	1	1	1	1	1	1

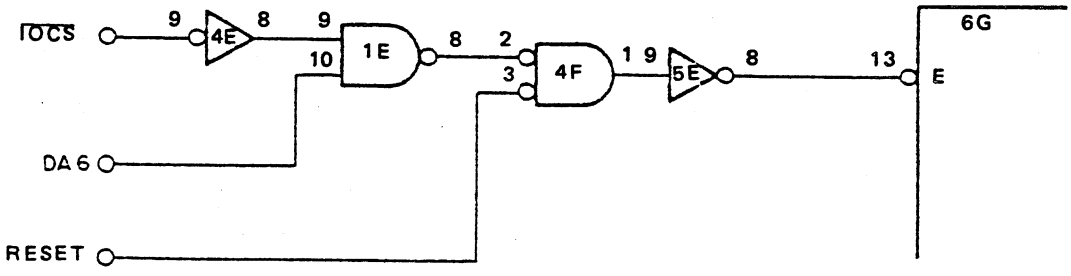


Fig. 2-10 Addressing of Clock RAM

2.3.3 $\overline{\text{IOCS}}$ signal

The $\overline{\text{IOCS}}$ signal is output under the condition of $\overline{\text{A7}}$~$\overline{\text{15}}$ (i.e., address lines $\overline{\text{A7}}$~$\overline{\text{A15}}$ all are at Low level). This signal is used for switching addresses in the low-order area of a memory.

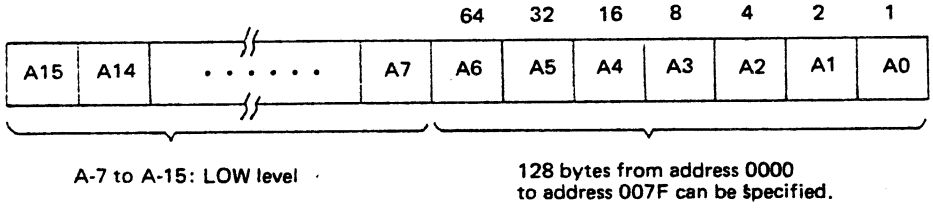


Fig. 2-11 $\overline{\text{IOCS}}$ Signal

Function	Operation
External RAM Control ($\overline{\text{IOCS}}$)	Chip Enable output to the external RAM corresponding to addresses 0000 to 07FF (2KB) is disabled.
Real-time Clock IC accessing ($\overline{\text{IOCS}}$)	According to the AND condition with address bit 6 (addresses 0040 to 007F), ENABLE signal (E) is output to the real-time clock IC so that accessing the real-time clock is enabled.
I/0 Select Control ($\overline{\text{IOCS}}$)	According to the AND condition with address bits 5 and $\overline{4}$ (addresses 0020 to 002F), GATE signal is output to the I/O select IC to enable I/O address selection. (By this signal, I/O addresses 0020, 0022, 0026, 0028, 002A, and 002C can be output.)
Bank Switching ($\overline{\text{IOCS}}$)	Using address bits $\overline{2}$, $\overline{3}$, $\overline{6}$, 4 and 5 and with address bits 1 and 0 in the ON or OFF state, the memory banks in the expansion unit are selectable. Note: Bit 0 is insignificant, and may be either ON or OFF.

2.3.4 RAM select circuit

Fig. 2-12 shows a schematic of the RAM select circuit.

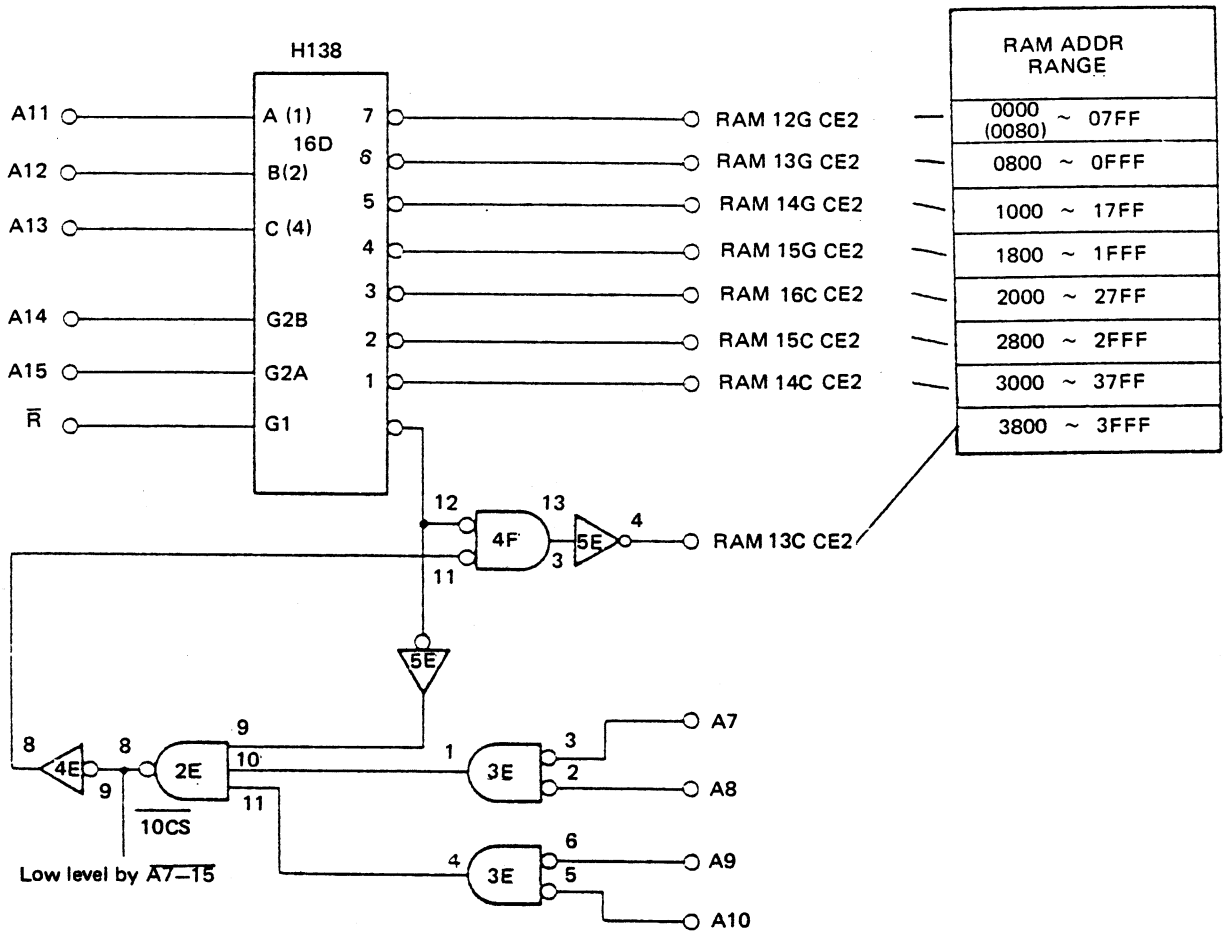


Fig. 2-12 RAM Select Circuit

2.3.5 I/O select circuit

When using any of the I/O addresses (I/O units) specified by the memory map, the I/O select circuit functions to output the gate signals corresponding to the respective I/O interfaces from IC "9E" as shown in Fig. 2-13.

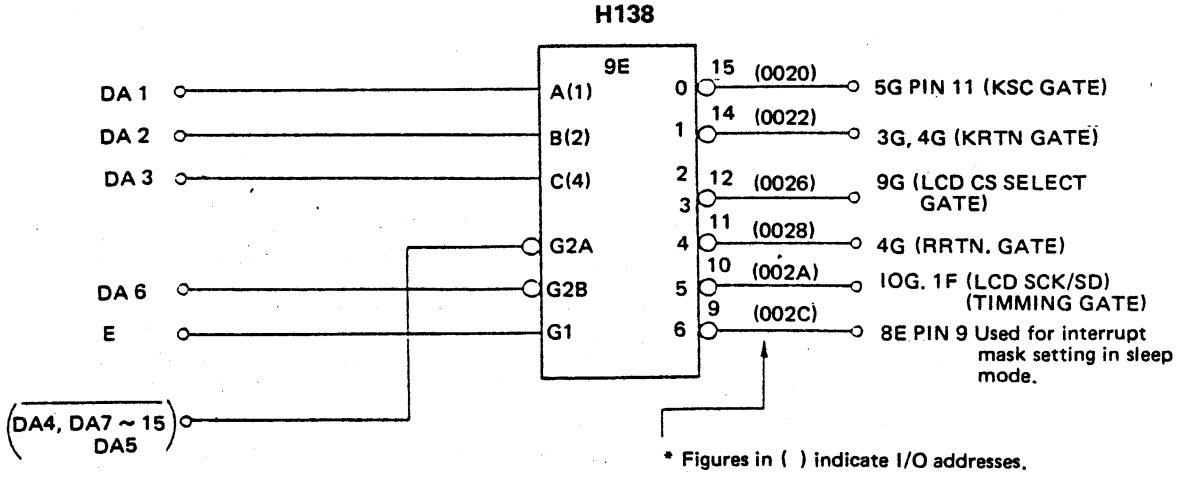


Fig. 2-13 I/O Select Circuit

0020: Used to output KSC GATE signal, to scan the keyboard data and the ON/OFF setting status of SW6.
0022: Used to input KRTN 0~7 signals to read out the keyboard data scanned by the KSC GATE signal onto the data bus.
0026: Used to mask an interrupt from the keyboard by changing the output level to Low at the pin No. 12 of IC "9G" in LCD chip select, ROM cartridge control, or interrupt mask reset in sleep mode.
0028: Used to read out KRTN signals 8 and 9, PW SW and BUSY (SO) signal onto the data bus.
002A: Used to output the SCK signal and SD (serial data) to the LCD.
002C Used for interrupt masking in sleep mode through IC "8E".

2.3.6 ROM select circuit
Fig. 2-14 shows a schematic of the ROM Select Circuit.

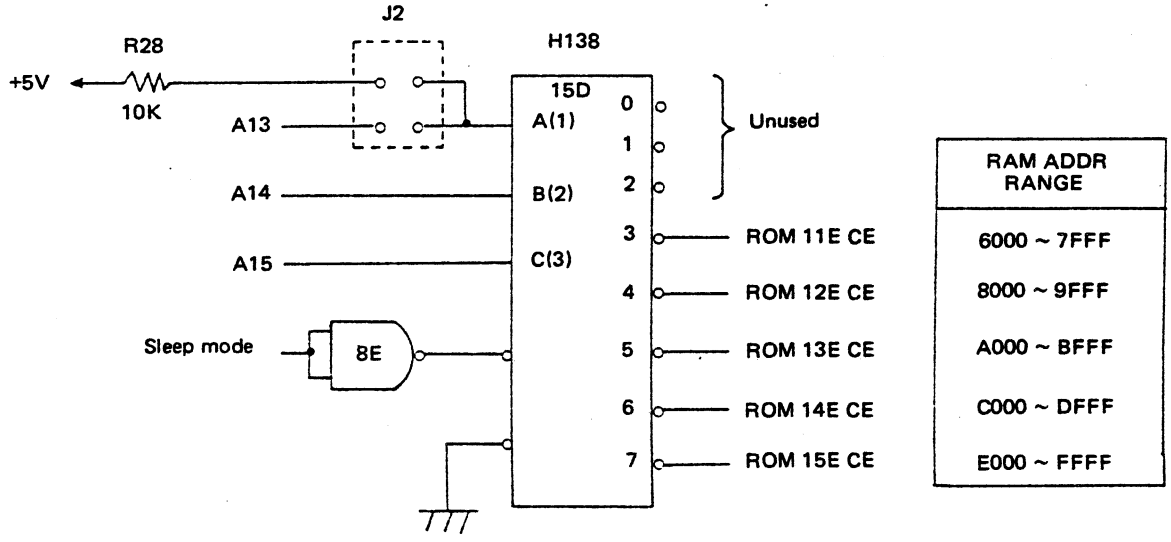


Fig. 2-14 ROM Select Circuit

2.4 Address Map
Since the master CPU operates in Expanded Multiplex mode (i.e., mode 4), addresses 0000 to 001F are used for the internal registers of the CPU and addresses 0020 to 007F for an external memory (I/O addresses, clock registers and RAM area).

Addresses 0080 to 00FF are assigned to the internal RAM of the CPU and addresses 0100 to FFFF to an external memory.

The slave CPU operates in Single Chip mode and thus addresses 0020 to 007F and 0100 to EFFF cannot be used.

2.4.1 Division of master CPU addresses (Low-order Area)
The addresses of the master CPU are divided by the RAM control bit 6 (address 0014) and IOCS signal as shown below.

Note: Addresses from 0080 to 00FF are selectable between the external RAM and internal RAM by the RAM control bit 6.

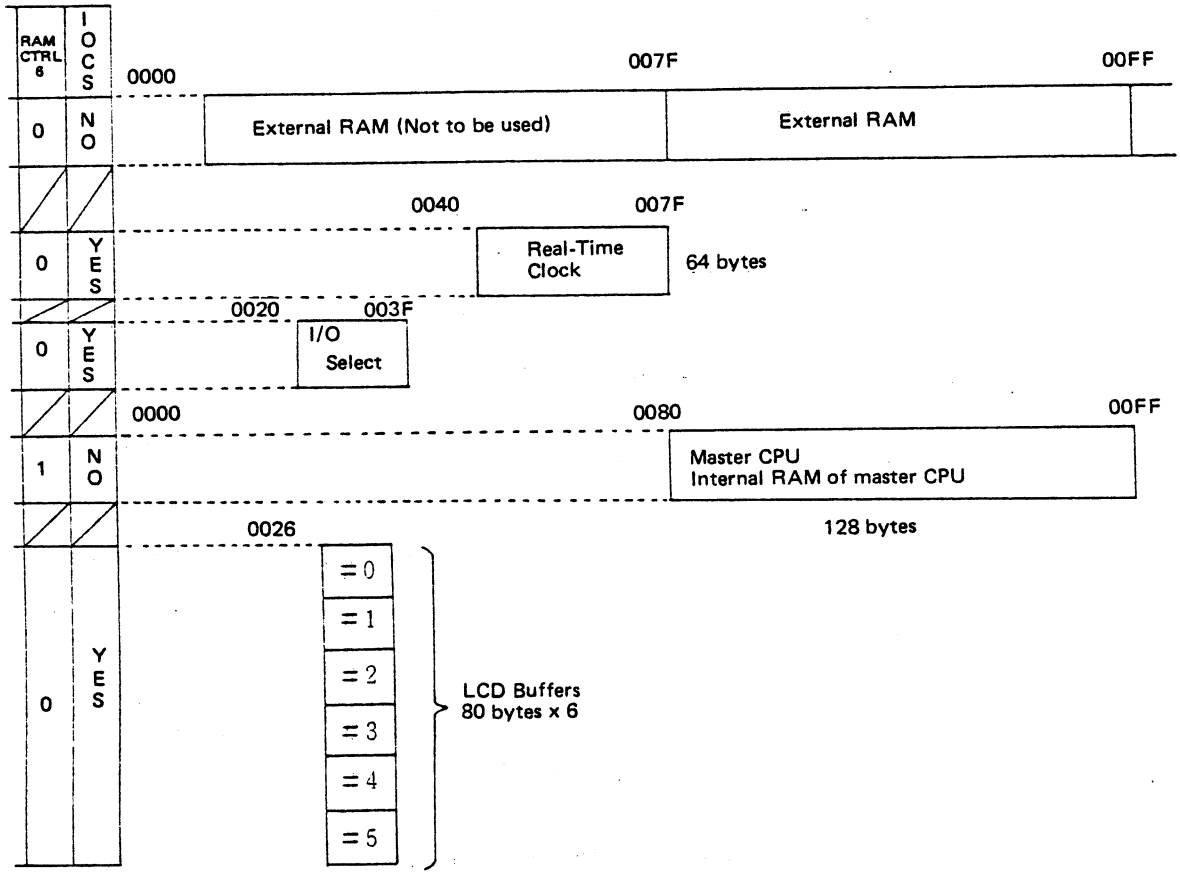


Fig. 2-15 Division of Master CPU Address

2.4.2 Memory map of master CPU (in Expanded Multiplex Mode 4)
Addresses 0000 to 00FF exist in the master CPU and addresses from 0100 and higher are assigned to an external RAM (ICs 13C~16C and 12G~15G and the expansion unit).

Address	Description
0000 ∫ 0007	Port control and registers PORT / PORT ADDR / DIRECTION REG. 1 / 0002 / 0000 (RS-232C I/F and others) 2 / 0003 / 0001 (Serial I/F, RS-232C I/F, barcode reader) 3 / 0006 / 0004 (A0~A7 and D0~D7) 4 / 0007 / 0005 (A8~A15)
0008 ∫ 000F	Timer control and data registers 0008 : Timer control 0009 ~ 000A : Free running counter ..... CPU R/W 000B ~ 000C : Output compare register ... R/W 000D ~ 000E : Input capture register .... READ 000F : P3 control register
0010 ∫ 0013	Serial control and registers 0010 : Serial bit rate 0011 : Serial control and status 0012 : Receive data register 0013 : Transmit data register
0014	RAM control : Switching between external RAM and internal RAM
0015 ∫ 001F	Unused
0020	Keyboard scan : KSC0~7 output or SW6 status read
0022	Keyboard input: KRTN0~7
0026	Cartridge interface, interrupt mask reset, LCD chip select or key masking
0028	Keyboard input : KRTN 8-9, $\overline{\text{PW SW}}$, BUSY
002A	Generates the clock for serial data transfer by ANDing with $\overline{R}/W$ signal.
0040 ∫ 004D	Clock registers 0040 : Second 0041 : Second (alarm) 0042 : Minute 0043 : Minute (alarm) 0044 : Hour 0045 : Hour (alarm) 0046 : Day of week 0047 : Date 0048 : Month 0049 : Year 004A ~ 004D : Control registers 1 ~ 4

Address	Description
004E ∫ 007F	RAM area for RAM system (50 bytes)
0080 ∫ 00FF	Internal RAM of CPU (128 bytes)
0100 ∫ FFFF	External RAM

2.4.3 Memory map of slave CPU (in Single Chip Mode)
The slave CPU controls input/output units such as microprinter, etc. by the control program stored in the built-in mask RAM (4KB).

Address	Description
0000 ∫ 0007	Port control and registers PORT 1 — PORT ADDR 0002 — DIRECTION REG. 0000 (microprinter and speaker) PORT 2 — PORT ADDR 0003 — DIRECTION REG. 0001 (SCI and others) PORT 3 — PORT ADDR 0006 — DIRECTION REG. 0004 (RS-232C I/F, external cassette and others) PORT 4 — PORT ADDR 0007 — DIRECTION REG. 0005 (RS-232C I/F, and ROM cartridge)
0008 ∫ 000F	Timer control and data registers 0008 : 0009 ~ 000A : 000B ~ 000C : Refer to the master CPU. 000D ~ 000E : 000F :
0010 ∫ 0013	Serial control and registers 0010 : 0011 : Refer to the master CPU. 0012 : 0013 :
0014	RAM control : Switching between external RAM and internal RAM

Address	Description
0015 ∫ 007F	Unused
0080 ∫ 00FF	Internal RAM (128 bytes)
0100 ∫ EFFF	Unused (These addresses do not exist physically.)
F000 ∫ FFFF	Internal ROM (4KB)

2.5 Interrupt Control

When an input/output unit etc., make a request for processing by the CPU, it must send an interrupt signal to the CPU.

According to the type of interrupt shown in the interrupt table below, each class of interrupts is assigned a priority. In each vector address, the starting address of the program required for the processing of an interrupt request (i.e., interrupt handling routine) is stored. When an interrupt request occurs and the CPU is ready to accept the interrupt request, the contents of the program counter and index register, etc., are saved to the stack area and the CPU processes the interrupt request.

2.5.1 Interrupt priority table of master CPU

Interrupt level	Vector address	Interruption source
HIGHEST	FFFE FFFF	° Immediately after power on ° After reset
	FFFF FFFF	° Address error or operation code error (TRAP) ... Used by the MONITOR.
	FFFC FFFD	° $\overline{\text{NMI}}$ signal (Unused)
	FFFA FFFB	° Software interrupt (Unused)
	FFF8 FFF9	° Key input ($\overline{\text{K.B REQUEST}}$ signal) ° Power on (PW SW signal) ° Power off ($\overline{\text{PW SW}}$ signal) ° Clock ($\overline{\text{CLOCK IRQ}}$ signal) ° External interrupt ($\overline{\text{INT EX}}$ signal)
	FFF6 FFF7	° Timer Input Capture (Unused)
	FFF4 FFF5	° Timer Output Compare (Keyboard)
	FFF2 FFF3	° Timer overflow (Microcassette)
LOWEST	FFF0 FFF1	° Interrupt from SCI (serial communication interface) (PIN signal) (CTS signal)

2.5.2 Interrupt priority table of slave CPU

Interrupt level	Vector address	Interruption Source
HIGHEST	FFFE FFFF	° Immediately after power on ° After reset
	FFFE FFFF	° Address error or operation code error (TRAP)
	FFFC FFFD	° $\overline{\text{NMI}}$ signal (Unused)
	FFFA FFFB	° Software interrupt
	FFF8 FFF9	° Unused
	FFF6 FFF7	° Timer Input Capture
	FFF4 FFF5	° Timer Output Compare
	FFF2 FFF3	° Timer Overflow (Microcassette)
LOWEST	FFF0 FFF1	° Interrupt from SCI

CHAPTER 3 INTERFACE OPERATION

3.1 RS-232C Interface

Using the RS-232C interface, the HX-20 can transfer data to and from a terminal printer, a personal computer, or other terminal via CX-20 acoustic coupler.

Since the RS-232C interface requires prescribed voltage levels (+3V to +27V for SPACE=logic "0" and -3V to -27V for MARK=logic "1"), the voltages meeting this requirement must be generated from the +5V battery voltage. In the HX-20, +8V and -8V are generated as the power supplies for the RS-232C interface by the built-in regulator. To minimize the power comsumption of the HX-20, this regulator is controlled under software so that it operates only when the RS-232C interface is used.

3.1.1 Operation at power ON

When the P36 of the slave CPU (6301) is set at 'HIGH' level, the pin No. 12 of IC "7E" goes low, causing $\overline{SWL}$ signal to be output. This in turn causes transistor Q2 to turn on. When transistor Q2 is turned on, voltage V_B is supplied to the pin No. 14 (V_{CC}) of the TL497, causing it to operate. The TL497 then starts switching transistor Q11 and generates +8V and -8V. +8V is passed to resistor R22 (5.1KΩ), where the voltage is converted to DTR signal.

By sending this signal to a MODEM, it is possible to confirm that the HX-20 and the MODEM interface have been interconnected properly. The RS-232C interface in the HX-20 employs USART (Universal Synchronous/ Asynchronous Receiver/Transmitter) ICs (6B: HD75188) quad line driver and 7B: HD75189 quad line receiver) conforming to the interface standard. Therefore, the RS-232C interface operates according to the same interface standard when a voltage of +8V/-8V is supplied.

3.1.2 Interface circuit

Fig. 3-1 shows the circuit diagram of the RS-232C interface.

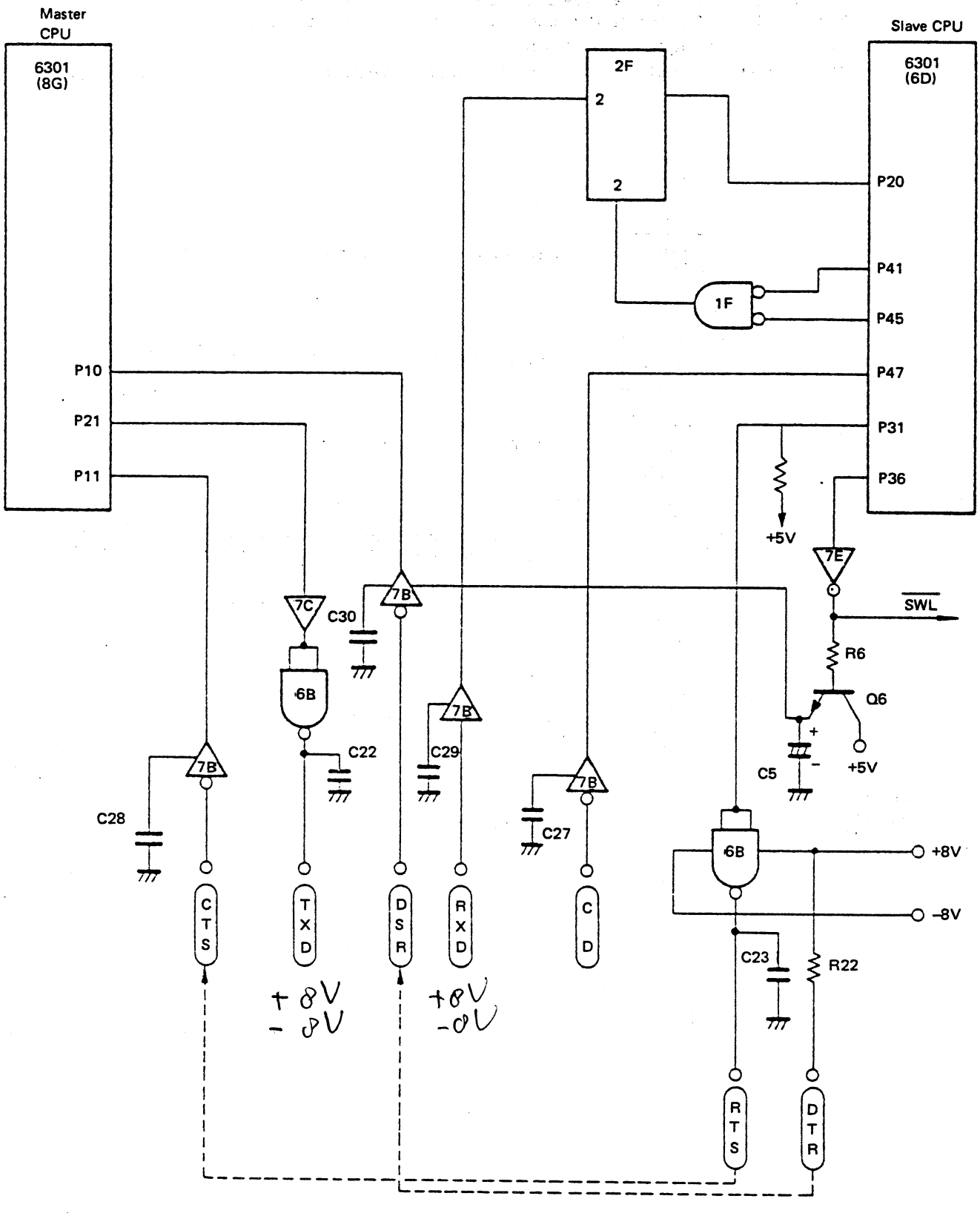


Fig. 3-1 RS-232C Interface Circuit

3.1.3 Operation sequence

In the HX-20, both the master CPU (6301: IC "8G") and slave CPU (6301: IC "6D") control the RS-232C interface operation.

The master CPU controls the data transmission while the slave CPU controls the data reception.

The normal operation of the RS-232C interface is as shown in Fig. 3-2.

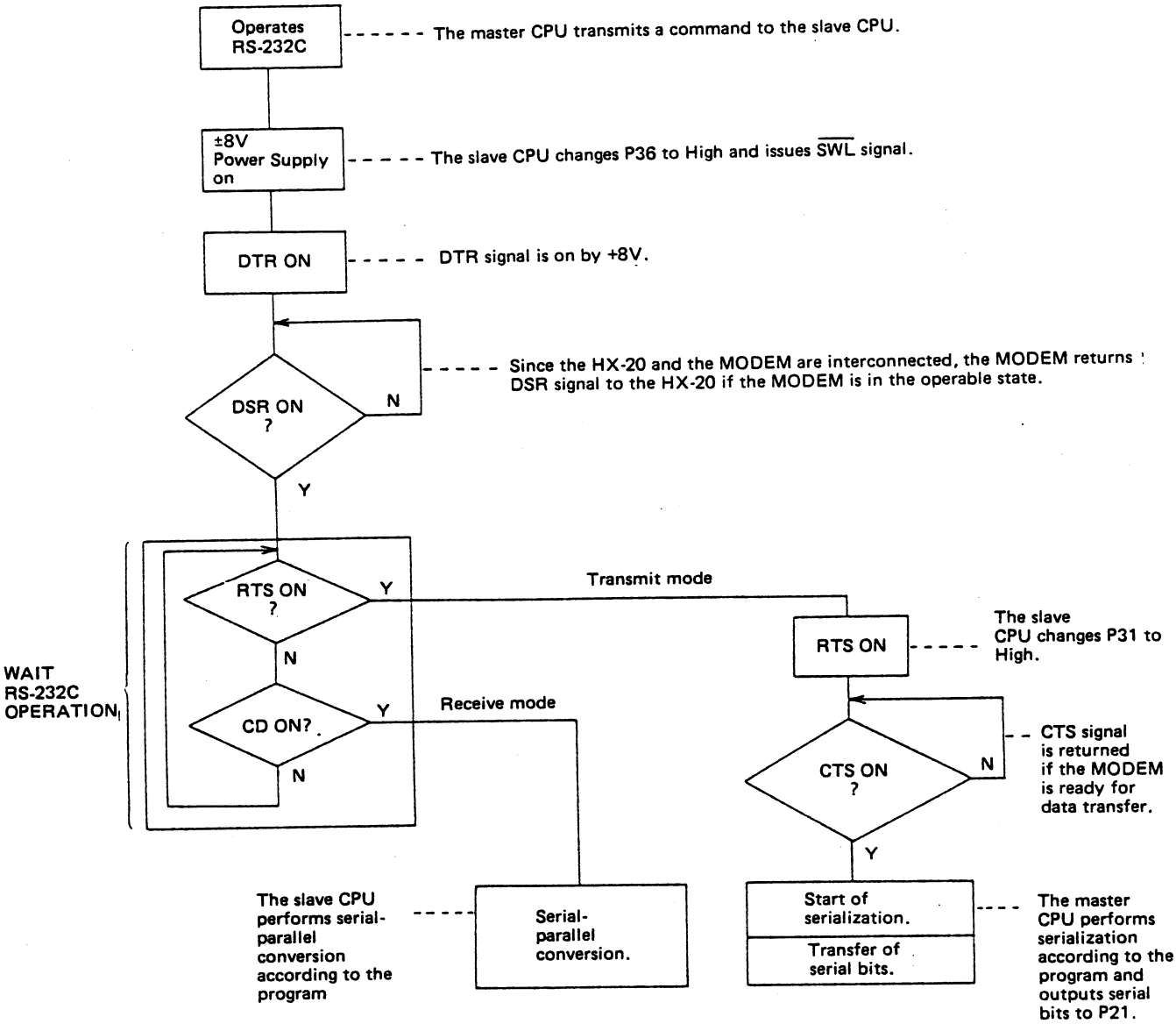


Fig. 3-2 Interface Operation

3.1.4 Operation timing of RS-232C interface

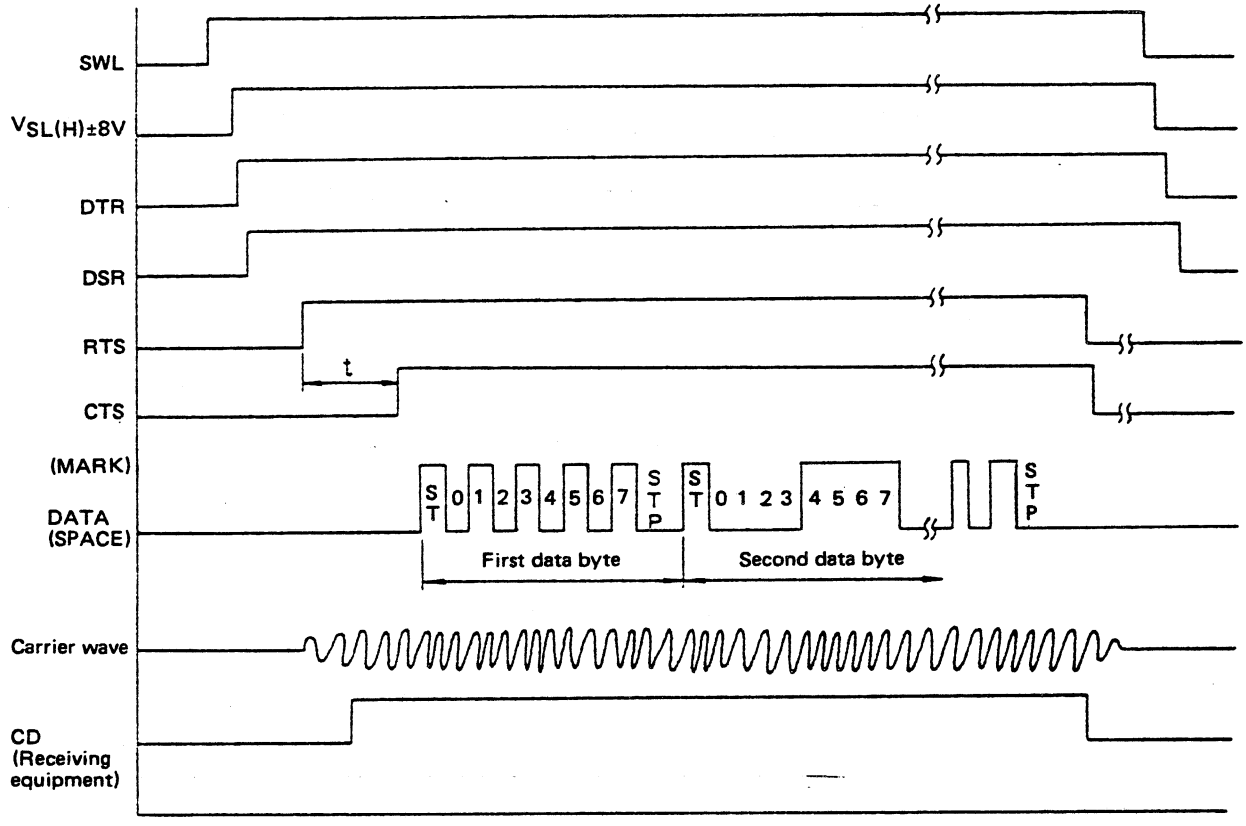


Fig. 3-3 Operation Timing of RS-232C Interface

*: t indicates the delay time until the MODEM becomes ready for data transmission. MODEMs may or may not require this delay time depending on the type.

(1) Signal polarity
    (a) Mark=logic "1" (-3V to -27V)
        : Stop bit
    (b) Space=logic "0" (+3V to +27V)
        : Start bit
(2) Word length
    (a) Start bit: 1 bit
    (b) Data bits: 7 or 8 bits
    (c) Stop bit: 1 bit or more
(3) Bit rate: 110 to 4800 BPS

3.1.5 Operation when a MODEM (coupler) is used

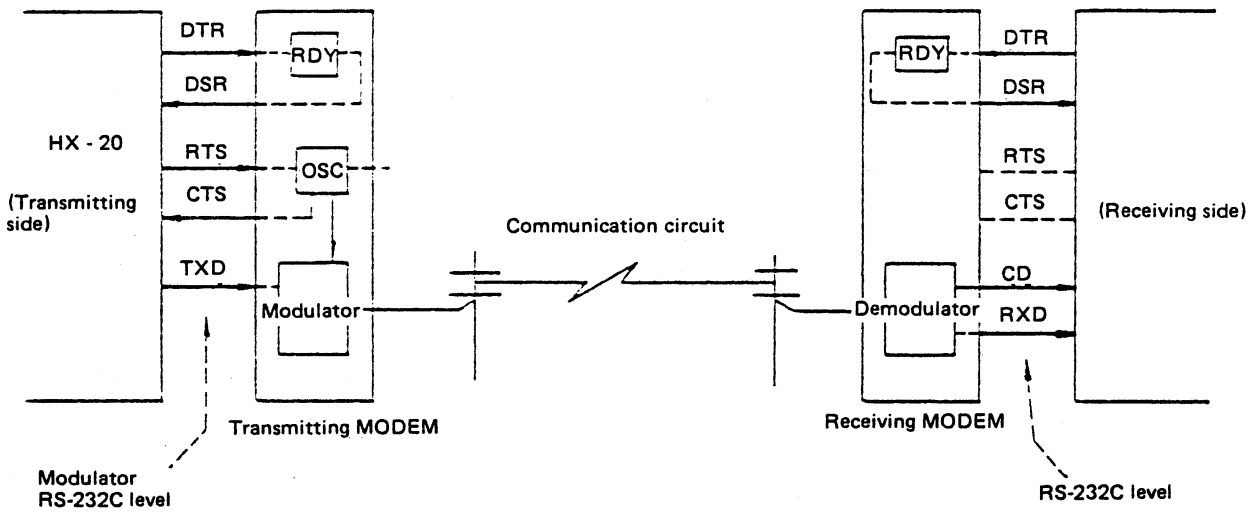


Fig. 3-4 Interface Operation with MODEM

(1) MODEM
MODEM is an acronym for MOdulator/DEModulator. There are 3 modulation modes: Frequency-shift keying (FSK), Phase-shift keying (PSK) and Amplitude modulation (AM).

(2) Operation
The transmitting terminal (HX-20 in Fig. 3-4) outputs a DTR (Data Terminal Ready) signal to check whether or not the MODEM is ready for operation. If the MODEM is operable, the HX-20 receives a DSR (Data Set Ready) signal from the MODEM and then requests the MODEM to transmit data by outputting an RTS (Request To Send) signal to the MODEM if there is any transmit data. When the MODEM receives the RTS signal, it activates the oscillator for a carrier wave and outputs this carrier wave to the transmit data line.
The MODEM also transmits a CTS (Clear To Send) signal to the transmitting terminal after the oscillator output has been stabilized. The time required for output stabilization depends on the characteristics, etc. of the oscillator).
When the receiving MODEM detects the carrier wave on the receive data line, it outputs a CD (Carrier Detect) signal and places the receiving terminal in the standby state for data reception. When the transmitting terminal receives the CTS signal, it converts parallel data into serial data and starts the transfer of data bit by bit to the transmitting MODEM.
The transmitting MODEM modulates the received data bits and transmits them to the transmit data line. As the receiving terminal has been placed in the receiving state by the CD signal, the data modulated and sent by the transmitting MODEM are demodulated by the receiving MODEM and sent to the receiving terminal as digital data. The above MODEM operations are shown in Fig. 3-5, Timing Chart of MODEM Operations.

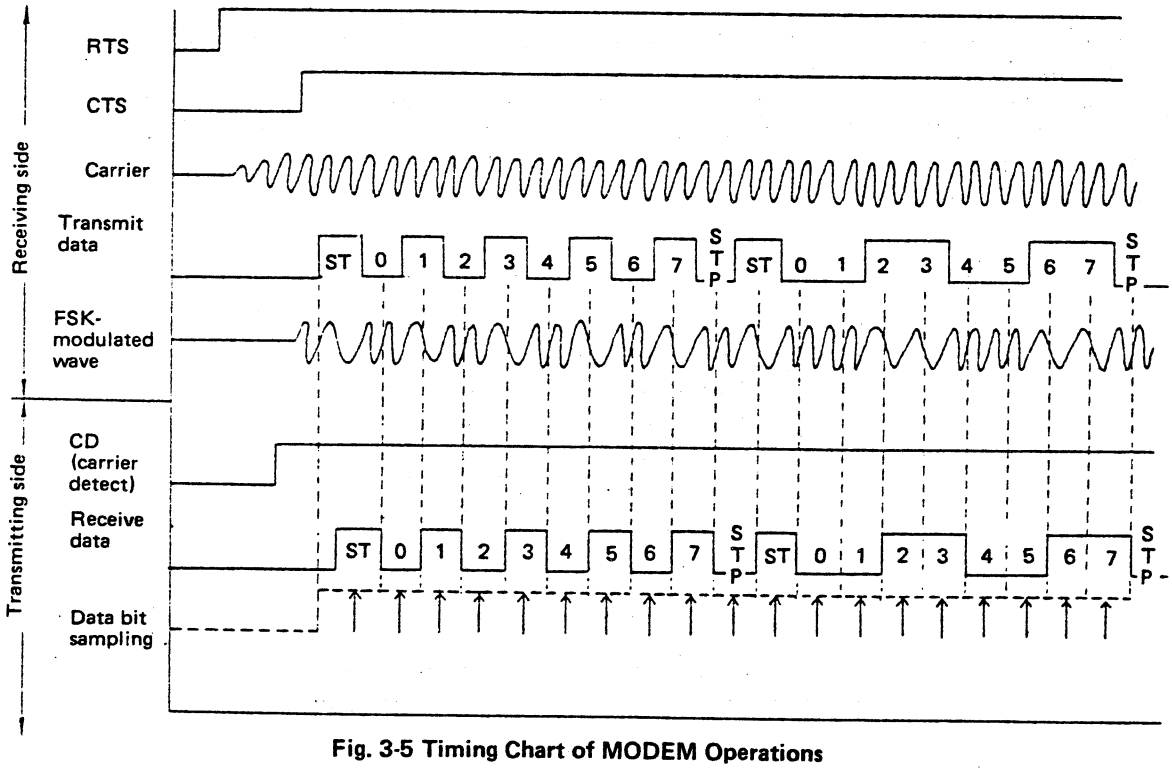


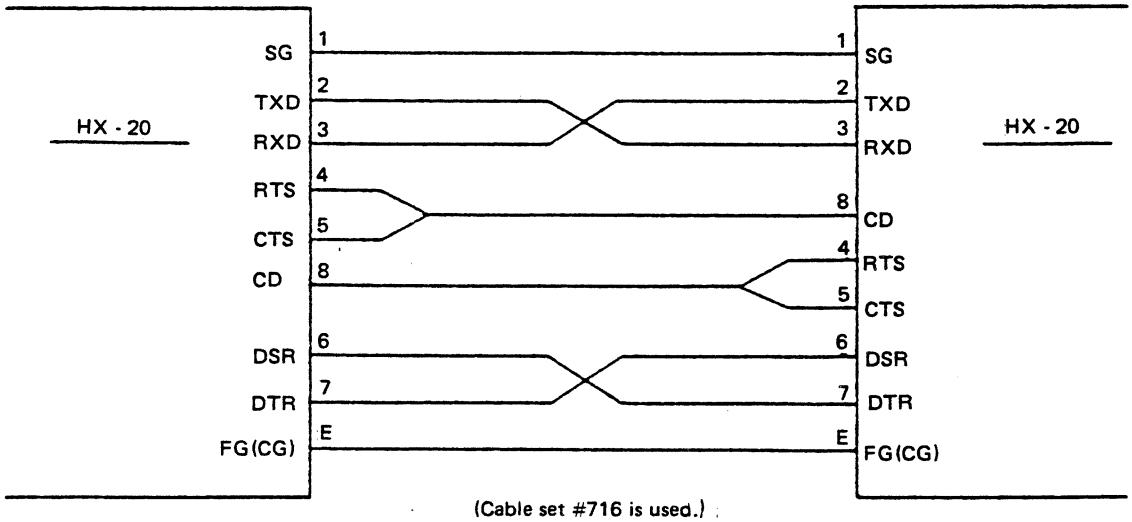
Fig. 3-5 Timing Chart of MODEM Operations

3.1.6 Data transfer between two HX-20 units

The data transmission/reception operation between the two HX-20 units interconnected without a MODEM differs from the normal RS-232C interface operatfon, in that these HX-20 units use the interconnected cables to generate the signals which cannot be normally output without the MODEM.

(1) The DSR and DTR terminals are cross-connected as shown in Fig. 3-6 to turn on the DSR terminal of the receiving HX-20 by the DTR signal of the transmitting HX-20.

(2) The RTS and CTS terminals are connected together within each HX-20 unit, so that a CTS signal is automatically detected upon output of an RTS signal. When the transmitting HX-20 sends this signal to the CD line, the receiving HX-20 enters the receiving state.



(Cable set #716 is used.)

Fig. 3-6 Data Transfer Between Two HX-20 Units

3.1.7 Operation with a terminal printer (exclusive of HX-20)
When an EPSON printer for exclusive use of the HX-20 is to be connected to the HX-20, the printer requires a serial interface (EPSON Cat. No. #8145 with a 2K buffer). When this interface is used, the printer can only receive data from the HX-20. It cannot transmit data to the HX-20.

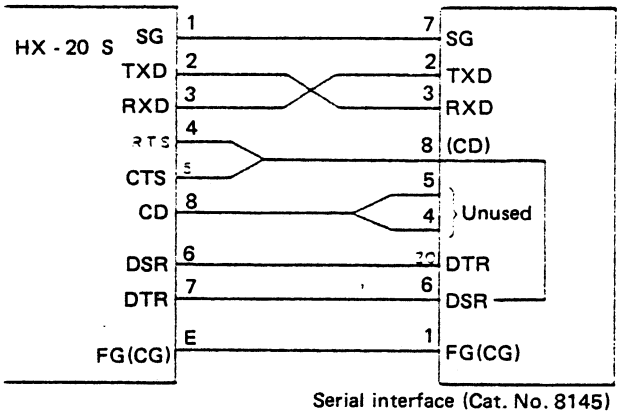


Fig. 3-7

(1) The RTS and CTS terminals are interconnected within the cable on the HX-20, so that a signal from the terminals is connected to the pin No. 8 (CD) of the interface connector on the printer side. Pin No. 8 (CD) and pin No. 6 (DSR) are interconnected on the serial interface board of the printer. Pin No. 6 is connected to the pin No. 7 (DTR) of the interface connector on the HX-20. When the HX-20 outputs a DTR or RTS signal, the RTS, CTS, and DTR terminals of the HX-20, and the CD and DSR terminals of the printer are activated.
(2) The DTR signal of the printer is connected to the DSR terminal of the HX-20 and indicates whether or not the printer is ready for data transfer (when this signal is high, the printer can receive data). The HX-20 thus transfers data to the printer while checking this DSR signal.

3.1.8 RS-232C interface signals
The RS-232C interface signals are controlled by the port addresses of the master or slave CPU and the direction registers corresponding to the port addresses. Since the input/output directions of the interface signals are fixed hardware-wise, they cannot be changed by setting the direction registers.

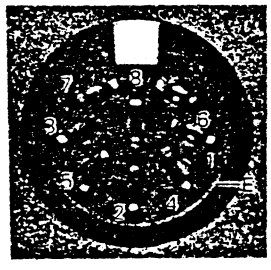
Since the RS-232C interface uses +8V and -8V as the interface signal levels, the port P36 of the slave CPU must be set to High and +8V and -8V must be produced from the battery voltage before using this interface.

Table 3-1 RS-232C Interface Signals

Pin No.	Signal name	Signal direction	Description	Control port (master/slave)	Port address	Control
1	GND	-	Signal Ground	-	-	Negative pole of the built-in battery
2	$\overline{TXD}$	OUT	Transmit Data	P21 (Master CPU)	"0003" Bit 1	Direction register address "0001"
3	$\overline{RXD}$	IN	Receive Data	P20 (Slave CPU)	"0003" Bit 0	Direction register address "0001" (Condition) P41 and P45 of the slave CPU must be LOW. (Address "0007" and Bits 1 and 5) Direction register address "0005"
4	$\overline{RTS}$	OUT	Request to Send	P31 (Slave CPU) (LOW active)	"0006" Bit 1	Direction register address "0004"
5	$\overline{CTS}$	IN	Clear to Send	P11 (Master CPU) (LOW active)	"0002" Bit 1	Direction register address "0000"
6	$\overline{DSR}$	IN	Data Set Ready	P10 (Master CPU) (LOW active)	"0002" Bit 0	Direction register address "0000"
7	$\overline{DTR}$	OUT	Data Terminal Ready	P36 (Slave CPU) (HIGH active)	"0006" Bit 6	Direction register address "0000"
8	$\overline{CD}$	IN	Carrier Detect	P47 (Slave CPU)	"0007" Bit 7	Direction register address "0005"
E	$\overline{CG}$	-	Protective Ground	-	-	This pin is connected to the signal ground via a parallel circuit consisting of a 220KΩ register and a 0.01μF capacitor.

NOTES: 1. Direction registers
Both the master and slave CPUs have the direction registers which correspond to the respective I/O ports and define the input/output directions of the respective I/O terminals as follows.
Bit 1: Output
Bit 0: Input
The bit 1 of port 2 can be used for input or timer output. Thus the port 2 cannot be used as an output port.

2. By setting the port P36 of the slave CPU to High and producing +8V with the regulator, the DTR signal can always be held in the ON state by +8V.



3.2 Serial Interface

As serial interface employs the high-speed data transfer line between the master CPU and the slave CPU, this line is open to external devices as a high-speed serial interface on a time sharing basis. This serial interface allows data transfer at a maximum rate of 38,400 BPS and enables the HX-20 to be connected to a TF-20 floppy disk unit.

3.2.1 Operation control

The IC "4D" (4016) is located between the master CPU and slave CPU. By controlling a gate signal from this IC by the port P22 of the master CPU, the serial line is switched to perform data transfer in the full-duplex transmission system.

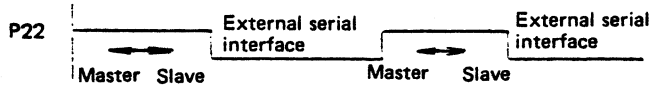


Fig. 3-8 Control of Interface Operation

3.2.2 Interface Operation

The serial interface is structured much simpler than the RS-232C interface, because the former can transfer data without a MODEM, eliminating the need of control signals for the MODEM.

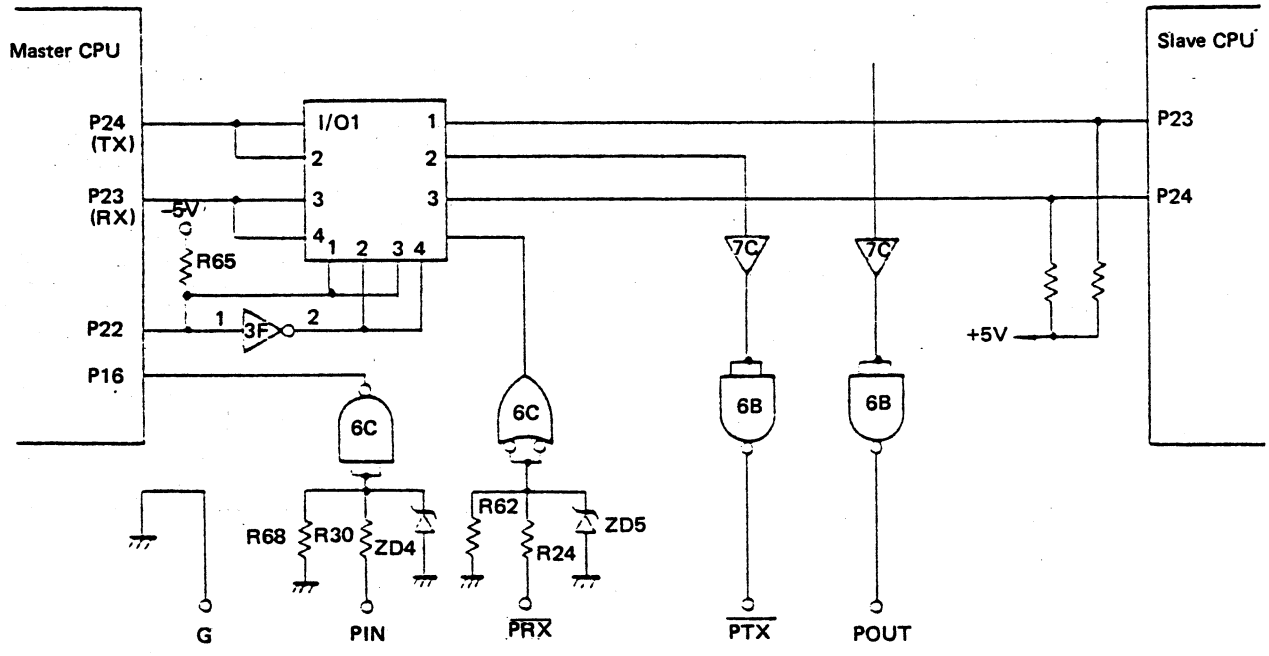


Fig. 3-9 Serial Interface Circuit

(1) Signal levels

The signal levels conforming to the RS-232C standard must be used when data transfer is to be performed between the HX-20 and an external device via the serial interface.

This means that +8V and -8V must be produced at the power supply section before starting the serial interface operation as in the case of the RS-232C interface.

3.2.3 Data transfer between two HX-20 units

The use of cable set #717 allows data transfer between two HX-20 units. The PTX and PRX terminals and the PIN and POUT terminals are cross-connected within the respective cables as shown in Fig. 3-10.

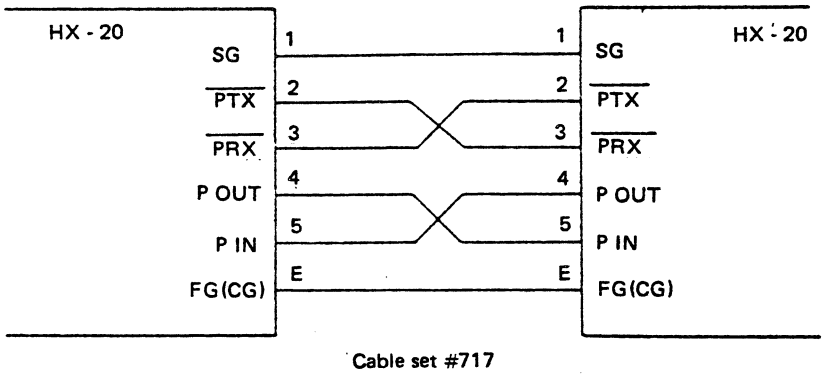


Fig. 3-10 Interconnection of Two HX-20 Units for Data Transfer

3.2.4 Connection with floppy disk units

Cable set #707 is used to connect two TF-20 floppy disk units with the HX-20 in daisy-chain mode. This cable uses two DIN connectors; 5-pin and 6-pin connectors. The pin No. 6 of the 6-pin DIN connector is not used for signal transmission, as it is merely intended for prevention of the incorrect insertion of the DIN connector.

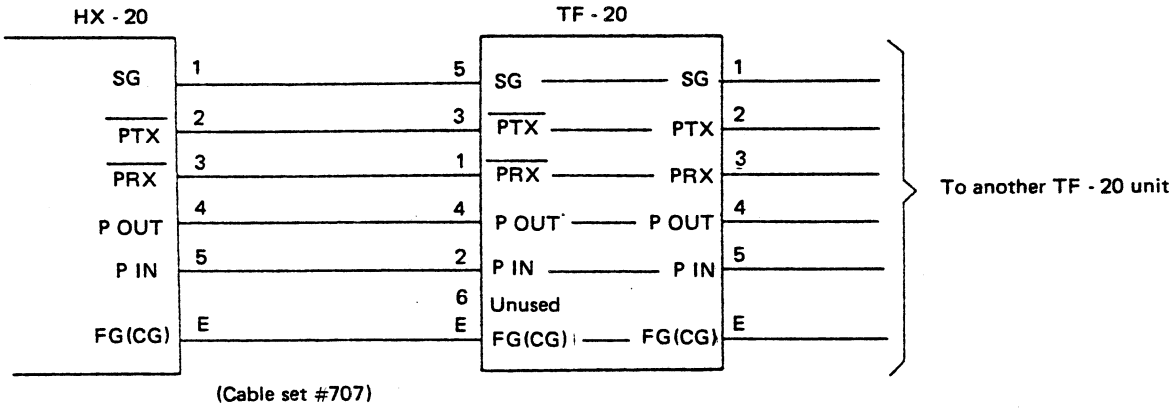


Fig. 3-11 Connection of HX-20 with TF-20

3.2.5 Serial interface signals

Since the serial interface uses +8V and -8V (supply voltages for RS-232C interface) as the interface signal levels, the port 36 (bit 6 of address "0006") of the slave CPU must be set to High and +8V and -8V must be output from the regulator before operating the serial interface. When ±8V is output, the DTR signal of the RS-232C interface is set to ON.

(1) As the input/output directions of the interface signals are fixed hardware-wise, they cannot be changed by setting the direction registers.

(2) Connector: 5-pin DIN connector TC4450

Table 3-2 Serial Interface Signals

Pin No.	Signal name	Signal direction	Description	Control port (Master/slave)	Port address	Control
1	GND	-	Signal ground	-	-	Negative pole of the built-in battery
2	$\overline{PTX}$	OUT	Transmit data	P24 (Master CPU) P22 (Master CPU) (LOW active)	Bit 4 "0003" Bit 2 "0003"	Direction register address "0001" (Condition) The P22 of the master CPU must be at LOW level. P22 controls switching between slave CPU and serial interface.
3	$\overline{PRX}$	IN	Receive data	P23 (Master CPU) P22 (Master CPU) (LOW active)	Bit 3 "0003" Bit 2 "0003"	Direction register address "0001" (Condition) The P22 of the master CPU must be at LOW level. P22 controls switching between slave CPU and serial interface.
4	POUT	OUT	Transmit mode	(Master CPU)	DA5 "0026"	
5	PIN	IN	Receive mode	P16 (Master CPU)	Bit 6 "0002"	Direction register address "0000"
E	CG	-	Protective ground	-	-	This pin is connected to the signal ground via a parallel circuit consisting of a 220KΩ resistor and a 0.01μF cpacitor.

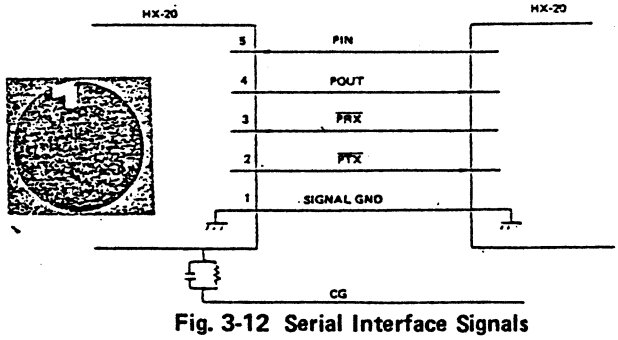


Fig. 3-12 Serial Interface Signals

3.3 External Cassette Interface

The external cassette interface in the HX-20 is used to read or write data (programs) to or from an ordinary cassette tape recorder. The same cassette tape recorder must be used for read/write operations, as the frequency characteristic, tape speed, the position adjustment of the read/write head (i.e., azimuth alignment), etc., of cassette tape recorders differ from one type to another. Note that if a tape written by one cassette tape recorder is read by another recorder, a read error may occur.

3.3.1 Operation control

All the cassette tape recorder operations are controlled by the slave CPU. Cable set #702 is used to connect the HX-20 with the cassette tape recorder.

(1) Motor control circuit

When the "RMT" cable is plugged into the cassette tape recorder and the recorder is placed in the RECORD or PLAYBACK mode, the HX-20 can control the motor of that recorder.

When the slave CPU receives a LOAD or SAVE command, the port P30 of the slave CPU goes Low, causing the anode side of diode D8 in the interface circuit to go Low, and the contact of relay LAD1 in the interface circuit to make. Then, the motor circuit of the cassette tape recorder is activated as shown in Fig. 3-13 and starts rewinding the cassette tape.

When the cassette tape recorder is not in use, the IN signal is pulled up from diode D10 so that the HX-20 accepts no data. However, when the port P30 of the slave CPU goes Low after the motor has been turned on, the IN signal line is also put in the operable state.

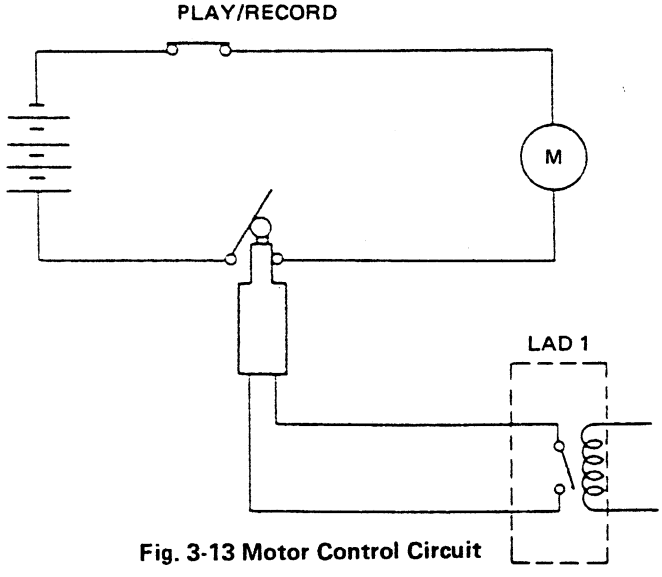


Fig. 3-13 Motor Control Circuit

(2) Data read

For a data read from the cassette tape recorder to the HX-20, the output signal from the cassette tape recorder enters the IN terminal of the interface circuit and is passed through capacitor C36 to cut the DC component of the output signal.
At the same time, the high voltage component due to noise is cut by zener diode ZD6. Then, the AC component thus obtained is supplied to IC "8D", where a threshold voltage is applied to the AC component with capacitor C25 and resistor R55 to shape its waveform as shown by ③ in Fig. 3-14 below. The signal is then passed to the pin No. 9 of IC "8D" and amplified for supply to the slave CPU as a pulse signal.

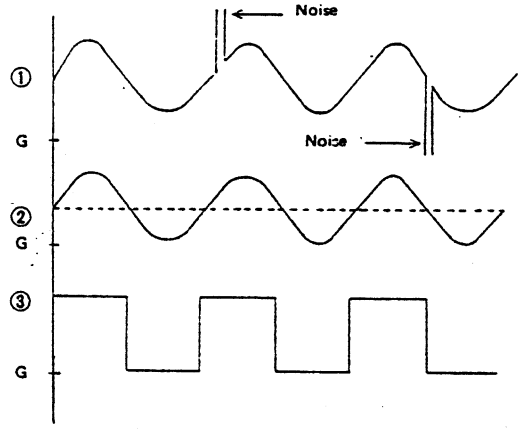


Fig. 3-14 AC Component of Output Signal

(3) Data write

For a data write from the HX-20 into the cassette tape recorder, a pulse signal is output to the cassette tape recorder from the port P33 of the slave CPU via the OUT terminal of the interface circuit. This signal is written into the cassette tape through the Read/Write circuit of the cassette tape recorder.

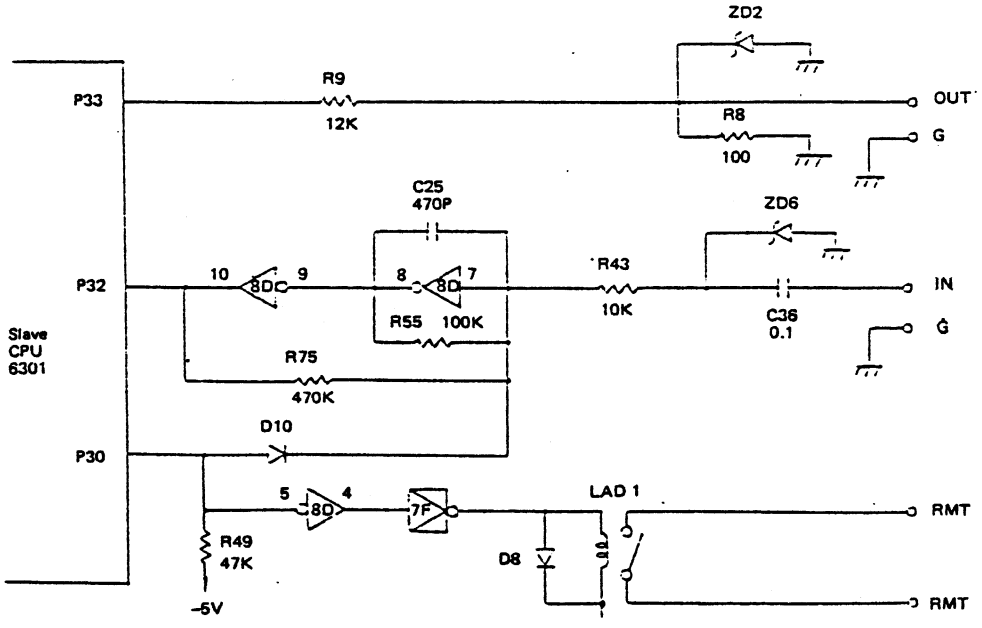


Fig. 3-15 Cassette Interface Circuit

3.3.2 Connection of external cassette with HX-20
Using the exclusive cables (cable set #702), the HX-20 must be connected to the cassette tape recorder as shown in Fig. 3-16.

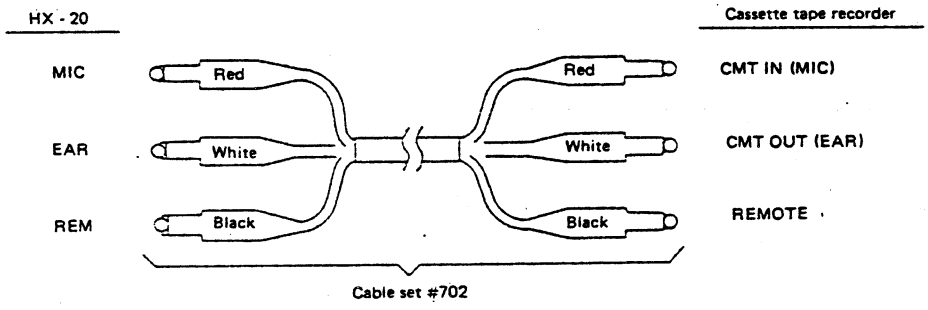


Fig. 3-16 Connection of External Cassette

The REMOTE signal is used for motor control of the cassette tape recorder. To control the motor of/off operation from the HX-20 using this REMOTE signal line, the cassette tape recorder must be set in the RECORD or PLAYBACK mode beforehand.

Note: Do not plug the REMOTE cable into the interface connector when the motor of the recorder is to be controlled manually without using a REMOTE signal.

(1) Read/write signals
The ON-OFF ratio of a read/write signal is 1KHz for ON and 2KHz for OFF.

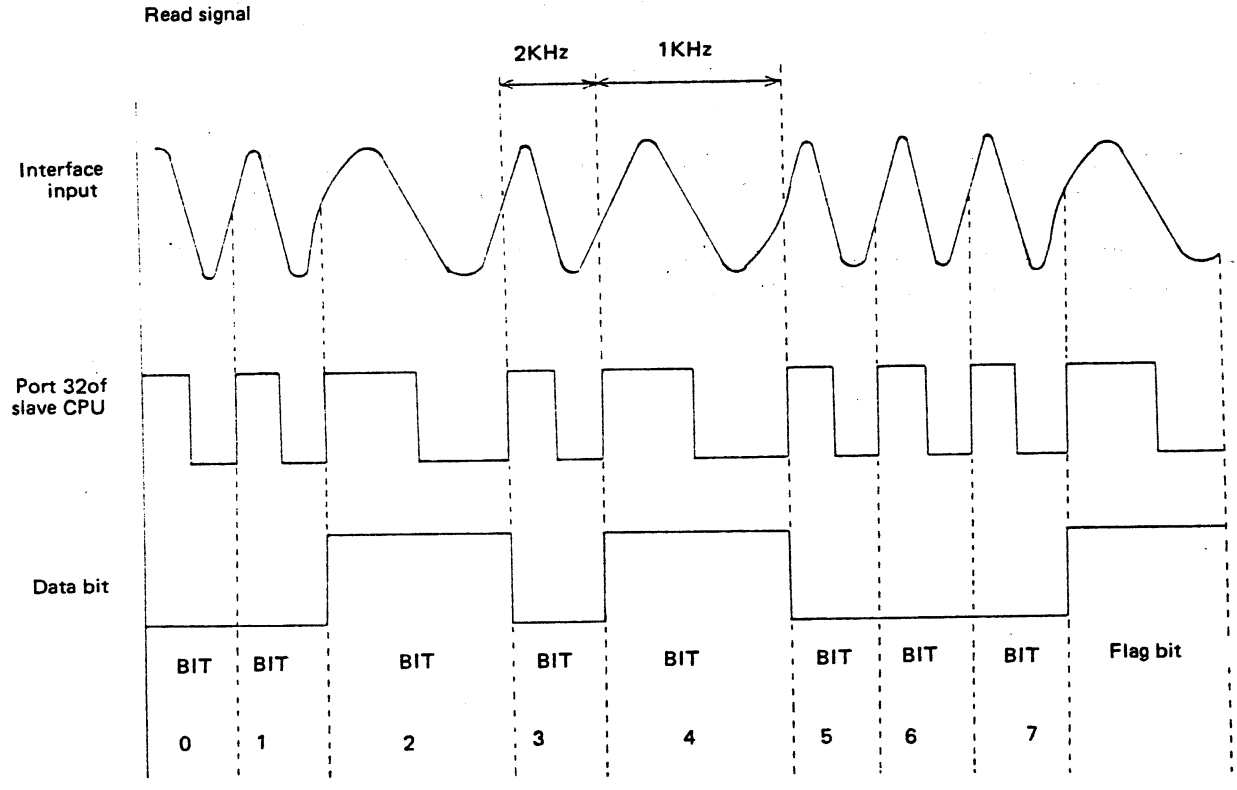


Fig. 3-17 Waveform of Read Signal

Note: A flag bit is required for each byte of data and must always be 1KHz (ON).

3.3.3 External cassette interface signals

As the input/output directions of the external cassette signals are fixed hardware-wise, they cannot be changed by setting the direction registers.

Table 3-3 External Cassette Interface Signals

Pin No.	Signal name	Signal direction	Description	Control port	Port address	Control
W3-1 W3-2	RMT RMT	- -	Remote ON/OFF control	P30 (Slave CPU) (LOW active)	"0006" Bit 0	Direction register address "0004" When port P30 of the slave CPU goes Low, SW3-1 and SW3-2 are interconnected through a 5.1Ω resistor and a relay contact.
W4-1	GND	-	Signal ground			Negative pole of the built-in battery
W4-2	IN	IN	Input data	P32 (Slave CPU)	"0006" Bit 2	Direction register address "0004" (Condition) The port P30 of the slave CPU must be Low.
W5-1	GND	-	Signal ground			Negative pole of the built-in battery
W5-2	OUT	OUT	Output data	P33 (Slave CPU)	"0006" Bit 3	Direction register address "0004"

Notes:

1. A 0.1μF capacitor is connected in series with the IN signal line and an output from this signal line is amplified by the IC via a 10KΩ resistor.
2. The OUT signal is a signal which is output from the port P33 of the slave CPU via a 12KΩ resistor.

3.4 Cartridge Interface (ROM Cartridge or Microcassette)

The cartridge interface is used to read data from the ROM cartridge or microcassette and to write data into the microcassette.

This interface is connected externally from the connector CN8 of the MOSU board via cable set #702 as shown in Fig. 3-18.

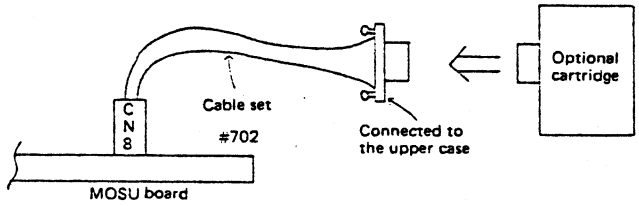


Fig. 3-18 Cartridge Interface

3.4.1 Operation control

Both the master CPU and slave CPU can control the cartridge interface. The type of the cartridge connected to the HX-20 is automatically identified by the 3 signal levels at the pin Nos. 1, 2, and 8 of cable set #702 as shown in Table 3-4.

Table 3-4 Signal Levels for Cartridge Type Identification

Cable set #702	Pin 8	Pin 1	Pin 2
Signal name & Port No. / Cartridge type	MI1 P17 (Master CPU)	SI1 P20 (Slave CPU)	SIO1 P46 (Slave CPU)
ROM cartridge	LOW	LOW	LOW
Microcassette	HIGH	-	-
Reserved	LOW	LOW	HIGH
Reserved	LOW	HIGH	HIGH
Not mounted	LOW	HIGH	LOW

3.4.2 Cartridge interface signals

The input/output directions of all the control signals except MO1 (pin No.5) and MO2 (pin No.6) can be changed by setting the direction registers, because these signals are directly connected to the ports of the master or slave CPU.

The directions of MO1 and MO2 signals are fixed hardware-wise as output only and cannot be changed.

Table 3-5 Cartridge Interface Signals

Pin No.	Signal name	Signal direction	Description	Control Port (Master/slave)	Port address	Control
1 and 2	+5V	OUT	Line voltage	-	-	This signal is supplied upon turning the power switch on.
3 and 4	GND	-	Signal ground			Negative pole of the built-in battery
5	MO1	OUT		(Master CPU)	"0026" DA6	
6	MO2	OUT		(Master CPU) P40 (Slave CPU)	"0026" DA7 "0007" Bit 0	Direction register address "0005"
7	MI1	IN		P17 (Master CPU)	"0002" Bit 7	Direction register address "0000" This pin is connected to the GND via a 1MΩ resistor.
8	V_B	OUT	Battery voltage	-	-	Positive pole of the built-in battery
9	SIO4	OUT		P42 (Slave CPU)	"0007" Bit 2	Direction register address "0005" This pin is connected to the GND via a 100KΩ resistor.
10	SIO3	OUT		P43 (Slave CPU)	"0007" Bit 3	Direction register address "0005" This pin is connected to the GND via a 100KΩ resistor.
11	SIO2	OUT		P44 (Slave CPU)	"0007" Bit 4	Direction register address "0005"
12	SO1	-		P21 (Slave CPU)	"0003" Bit 1	Direction register address "0001" This pin is connected to the GND via a 100KΩ resistor.
13	SIO1	IN		P46 (Slave CPU)	"0007" Bit 6	Direction register address "0005" This pin is connected to the GND via a 100KΩ resistor.
14	SI1			P20 (Slave CPU) P45 (Slave CPU) (HIGH active)	"0003" Bit 0 "0007" Bit 5	Direction register address "0001" (Condition) The P45 of the slave CPU (bit 5 of address "0007") must be HIGH. Direction register address "0005"

3.4.3 Microcassette interface connector and signals
The microcassette interface signals are connected to connector CN8 of the MOSU board via cable set #701.

(1) Connector CN8

(a) Use: To connect a microcassette drive or a ROM cartridge

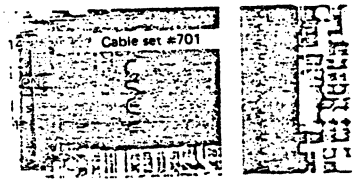


Fig. 3-19 Cable set #701

(b) Number of pins : 14

(2) Interface signals

See Table 3-6.

Table 3-6 Microcassette Interface Signals

CN8 pin No.	#701 pin No.	Signal name Exclusive name	Signal name Generic name	Signal direction	Description
14 13	1	RD/WE	SI1	IN	RD or WE signal is selected according to the value of CLK (pin No. 4) as follows. CLK=0: RD Read data of the microcassette CLK=1: WE Write erase protect signal (WE=0: Insertion inhibit)
12 11	2	CNT/HSW	SIO1	IN	CNT or HSW signal is selected according to the value of CLK (pin No. 4) as follows. CLK=0: CNT Count detection signal CLK=1: HSW Head switch (HSW=0: Head OFF)
10	3	WD	SO1	OUT	Write data to the microcassette
9	4	CLK	SIO2	OUT	Command set clock or RE/WE or CNT/HSW select signal
8	5	CMMND	SIO3	OUT	Serial data output of a command
7	6	PWSW	SIO4	OUT	Power ON/OFF switch
6	7	V_P		-	+5V ((or microccssette drive)
5	8	MCMT/CNT	MI1	IN	When the power is OFF, this signal indicates whether or not the microcassette is connected. (1: Connected 0: Not connected) When the power is ON, this signal causes the count detection signal to be input.
4	9		MO2	OUT	Unused
3	10		MO1	OUT	Unused
2	11	GND		-	Ground
1	12	V_L		-	+5V (for read/write circuit and selector instruction-register)

3.4.4 ROM cartridge

Table 3-7 ROM cartridge Interface Signals

CN8 pin No.	#701 pin No.	Signal name	Signal direction	Description
14	1	SI1	IN	ROM casette judgement input (Always "0")
13	2	SIO1	IN	ROM cassette judgement input (Always "0")
12	3	SO1	-	Unused
11	4	SIO2	OUT	Address counter clear
10	5	SIO3	OUT	ROM power on
9	6	SIO4	OUT	Shift register clear (The register is cleared when this signal is logic "0".)
8	7	V_B	-	Battery voltage
7	8	MI1	IN	Shift register output
6	9	MO2	OUT	Shift register clock input
5	10	MO1	OUT	Counter input ($\overline{\sim\!\!\_}$) or shift register SHIFT/LOAD select
4 and 3	11	G	-	Ground
2 and 1	12	+5V	-	Line voltage

3.4.4. Barcode interface

The DATA signal line is fixed hardware-wise for input. Before using this interface, the port 35 of the slave CPU must be set to Low to output +5V.

Table 3-8 Barcode Reader Interface Signals

Pin No.	Signal name	Signal direction	Description	Control port	Port address	Control
1	GND	-	Signal ground	-	-	Negative pole of the built-in battery
2	DATA	IN	Received serial data	P20 (Master CPU) P41 (Slave CPU) (LOW active) P35 (Slave CPU) (LOW active)	"0003" Bit 0 "0007" Bit 4 "0006" Bit 5"	Direction register address "0001" Signal Pin No.3
3	+5V	OUT	Line voltage	P35 (Slave CPU) (LOW active)	"0006" Bit 5	

3.5 Expansion Unit Interface

(1) The expansion unit interface is provided in the HX-20 for extension of RAM and ROM memories. To this interface, 16 address lines and 8 data lines are parallelly output, as well as the $\overline{R/W}$ signal is output so that the master CPU can directly access the extended RAM or ROM memory by selecting an appropriate memory bank. In addition, line voltage V_L (+5V), backup voltage V_C (+3V/+5V) and battery voltage V_B are output to the interface so that the circuitry of the expansion unit can be driven with the built-in power supply of the HX-20 alone.

(2) This interface also has other signal lines such as NMI, INT, and EX interrupt signals and bank select signal ROM E. Therefore, it allows the HX-20 to mount units other than the expansion unit.

3.5.1 Operation control

(1) Since the ROM/RAM in the expansion unit and the ROM in the HX-20 share partially the same memory addresses, switching of the memory banks is a must. To switch the memory banks, I/O addresses "0030" through "0033" are used. The ROM E signal is a signal used for this purpose. This signal is normally High. Once the ROM or RAM memory in the expansion unit is specified (by output of address "0030" or "0032"), ROM E goes Low and the ROM selector (IC "15D") in the HX-20 is placed in the non-operating state, causing 40K bytes of addresses "6000" through "FFFF" to be inaccessible.

(2) After the bank selection, the master CPU directly controls the expansion unit using the address and data lines as in the case of the internal ROM or RAM.

3.5.2 Interface connector and signals

(1) Connector CN7

(a) Use: To connect the control signals and data bus lines to the expansion unit

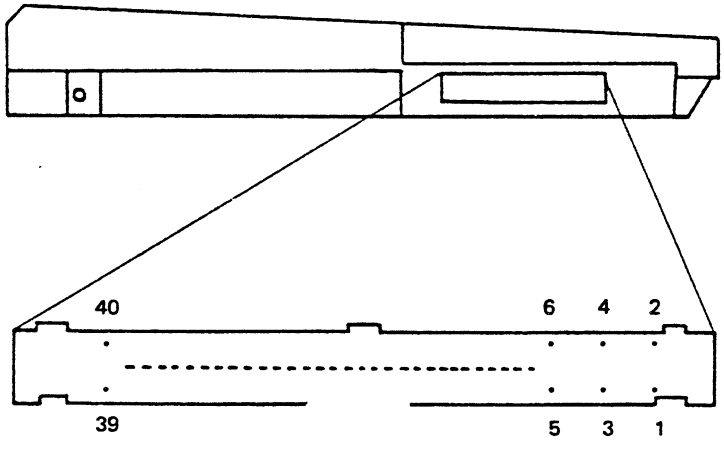


Fig. 3-19 Interface Connector CN7

(b) Number of pins: 40

(2) Interface signals

Table 3-9 Expansion Unit Interface Signals

Pin No.	Signal name	Signal direction	Description
1	VB	-	+5V
2	$\overline{NMI}$	-	Unused
3	+5V	-	Logic voltage
4			
5	DATA7	IN/OUT	Data line 7
6	DATA6	IN/OUT	Data line 6
7	DATA5	IN/OUT	Data line 5
8	DATA4	IN/OUT	Data line 4
9	DATA3	IN/OUT	Data line 3
10	DATA2	IN/OUT	Data line 2
11	DATA1	IN/OUT	Data line 1
12	DATA0	IN/OUT	Data line 0
13	$\overline{IOCS}$	OUT	I/O chip select
14	V_C	-	RAM backup voltage
15	ADDR0	OUT	Address line 0
16	ADDR1	OUT	Address line 1
17	ADDR2	OUT	Address line 2
18	ADDR3	OUT	Address line 3
19	ADDR4	OUT	Address line 4
20	ADDR5	OUT	Address line 5

Pin No.	Signal name	Signal direction	Description
21	ADDR6	OUT	Address line 6
22	ADDR7	OUT	Address line 7
23	ADDR8	OUT	Address line 8
24	ADDR9	OUT	Address line 9
25	ADDR10	OUT	Address line 10
26	ADDR11	OUT	Address line 11
27	ADDR12	OUT	Address line 12
28	ADDR13	OUT	Address line 13
29	ADDR14	OUT	Address lin3 14
30	ADDR15	OUT	Address line 15
31	R	OUT	Reset
32	$\overline{R}$/W	OUT	Read/write
33	$\overline{R}$ (RAM)	OUT	RAM reset
34	E	OUT	ENABLE signal
35	ROM E	IN	ROM ENABLE
36	$\overline{INTEX}$	IN	External interrupt signal
37	GND	-	Signal ground
38			
39	CG	-	Chassis ground
40			

Description of each interface signals follows:

V_B : This signal is output from the position terminal of the built-in battery. A voltage of +4V to +6V is normally output from the built-in battery via fuse F1 (5A) regardless of the ON/OFF state of the power switch.

NMI: Non-maskable interrupt signal. Upon completion of a command under execution, the contents of the program counter, index register, etc. are saved to the stack area, a vector address is generated and then program control is transferred to the NMI service routine.

+5V: Line voltage. +5V is supplied only while the power switch is being turned on.

DATA0~ DATA7: 8 parallel data lines. These signals indicate the respective I/O data codes. In Expanded Multiplex mode, these signals can also be used as the 8 low-order bits (ADDR0 through ADDR7) of an address. Each data line is connected to the GND via a 1MΩ resistor (RM-7).

$\overline{IOCS}$: $\overline{A7}$~$\overline{A15}$ address signal. This signal is used as follows.
(1) To enable the accessing of the real-time clock RAM (HD146818) when the address is 004XH (X=0~D). (In this case, the CHIP ENABLE terminal of the HD146818 is set to on.)
(2) To disable the accessing of low-order addresses 0000H through 07FFH of the external RAM in the HX-20. In this case, CE2 signal for RAM at location "13C" is not output.
(3) To enable I/O chip selection when the address is 002XH (X=0, 2, 6, 8, A, or C).

V_C: C-MOS RAM backup voltage. Approx. +3V is output when the power switch is turned off. The effective output current is 40mA max.

ADDR0~ ADDR15: 16 parallel address lines. These signals are used to address the peripheral devices (RAM and ROM, etc.) connected to the master CPU. In expanded Multiplex mode, the 8 low-order bits (A0 through A7) of an address are also used as data lines D0 through D7.

$\overline{R}$: Reset signal line. This signal is output only when power is applied or when the RESET switch is pressed.
NOTE: This signal is the same as the Reset signal of the master CPU.

$\overline{R}$/W: $\overline{Read}$/Write signal. This signal is an inversion of the R/$\overline{W}$ signal of the master CPU. The signal inversion is performed by IC "3F" (TC40H004).

R (RAM): Reset signal line. This signal is output only when power is applied or when the RESET switch is pressed.
NOTE: The Reset signal of the master CPU is the same as the R (RAM) signal which is output via IC "7C" (TC4049UBP).

E: E (ENABLE) signal of the master CPU. This signal serves as a system clock (614.6 KHz) for external devices.

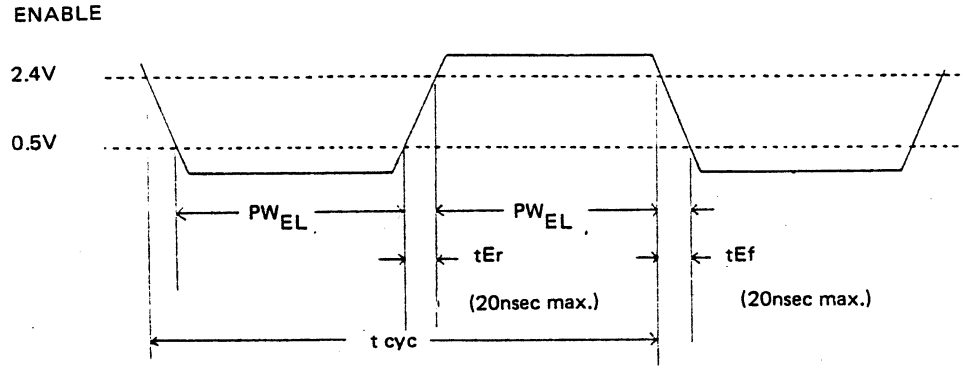


Fig. 3-20 ENABLE signal

ROM E: ROM ENABLE. This signal controls the output of the selector (IC "15D") in the internal ROM (locations 15E through 11E) and is pulled up by +5V line voltage via a 100KΩ resistor (R64) in the control circuit.
When the ROM E signal goes Low, selection of the internal ROM is disabled, since the CE (Chip Enable) signal is not output to the internal ROM.

INTEX: External interrupt signal. This signal serves as an interrupt request ($\overline{IRQ}$) signal to the master CPU and is pulled up by +5V line voltage via a 100KΩ resistor (R70) in the control circuit.

GND: Signal ground. This pin is connected to the negative pole of the built-in battery.

CG: Chassis ground

3.5.3 Timing chart of interface signals
See Fig. 3-2 for the timing chart of the respective interface signals.

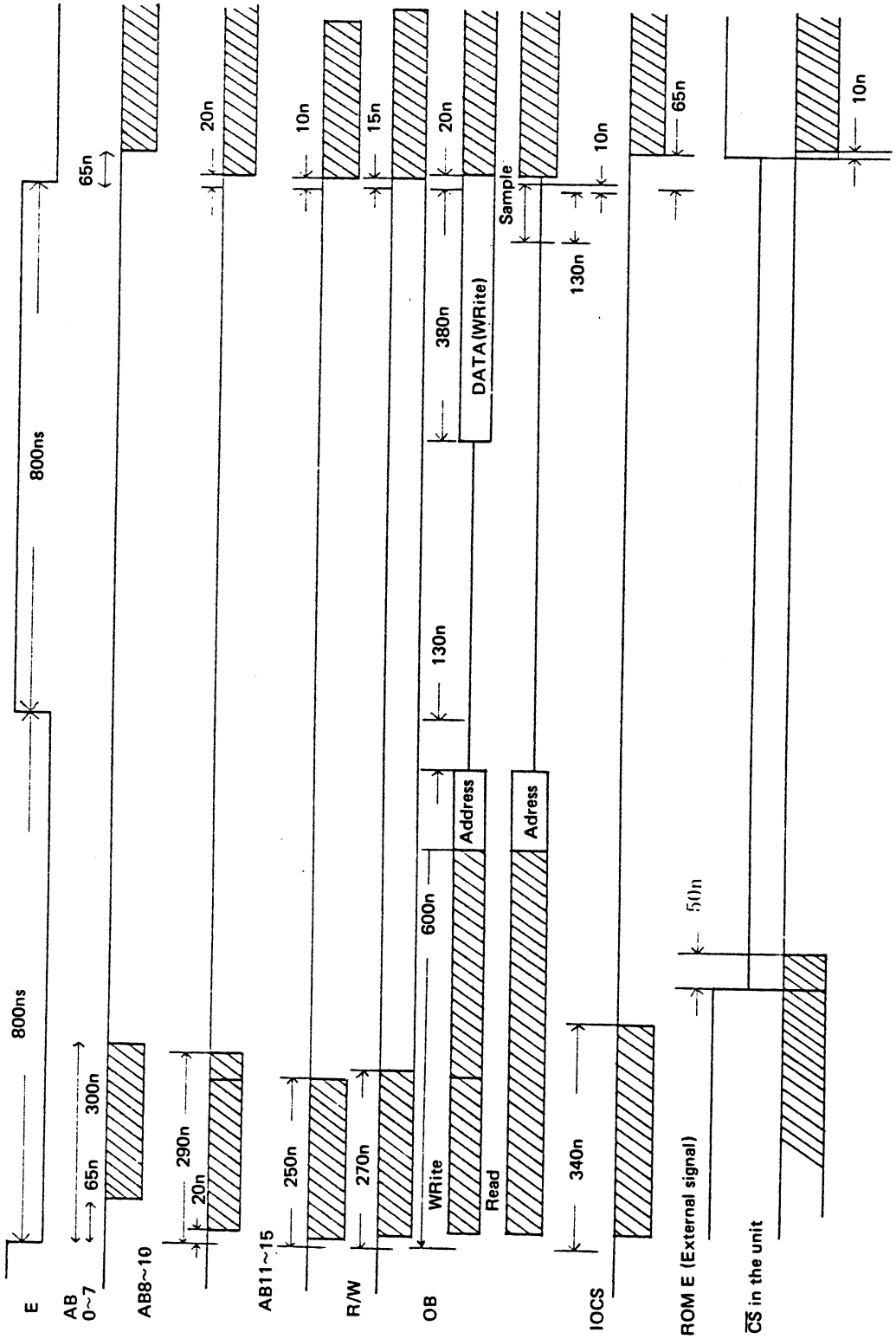


Fig. 3-21 Timing Chart of Expansion Unit Interface Signals

CHAPTER 4 SYSTEM EXPANSION

4.1 Options

4.1.1 ROM cartridge

The ROM cartridge can accommodate any of CMOS/NMOS mask ROMs and PROMs which have the pin configurations compatible with those of the 2764 (8KB), 27128 (16KB), or 27256 (32KB). Since programs and data are stored in the ROM housed in the cartridge, the memory contents are not destroyed even if an overrun error occurs. The ROM cartridge features much shorter access time than that with conventional cassette tape, etc. and assures complete data read. Reading of data from the ROM is performed in serial mode.

(1) Principles of Operation

The ROM cartridge is connected to the connector CN8 on the MOSU board through cable set #701. The ROM cartridge is controlled by both the master CPU and slave CPU. The master CPU handles address output and data readout, while the slave CPU controls power ON/OFF and address counter and shift register clear operations. As the programs and data stored in the ROM cartridge are in the form of files, a filename must be specified to read data from the cartridge.

Upon execution of a LOAD command, the power supply of the cartridge is turned on and the address counter and shift register are cleared. The contents of the header are then read from the address "0000" of the ROM cartridge in serial mode by the address output and the shift clocks for readout as follows.

If the filename in the header matches that specified by the LOAD command, the contents of the header (containing filename, starting address, etc. of the specified file) are transferred to the system area in the RAM. Simultaneously, message "Found" appears on the LCD, and the read operation proceeds up to the starting address of the specified file. Upon reaching the starting address, the shift clocks for readout are generated and the contents of the file are read in the master CPU in serial data format. (8 shift clock pulses are required to read 1 byte of data).

This operation continues until the ending address of the file. The data read serially are then converted byte by byte into parallel data and stored in the specified RAM addresses.

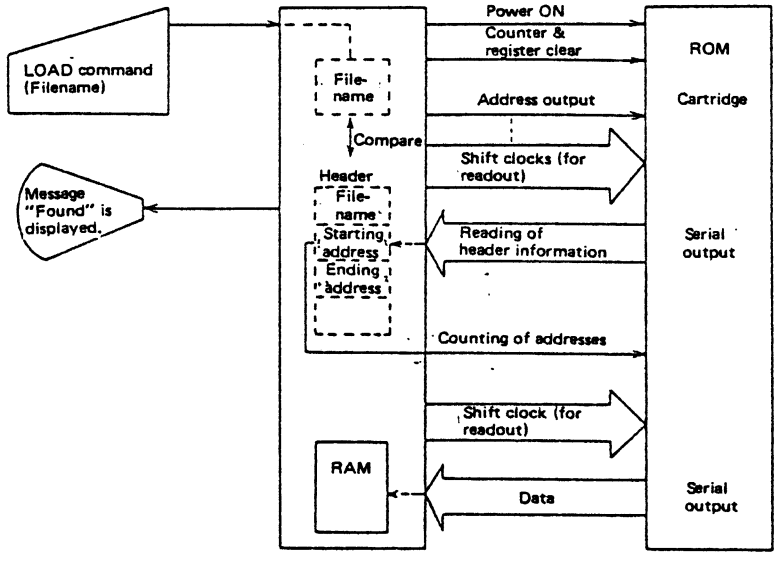


Fig. 4-1 Reading Data from ROM Cartridge

(2) Address counter

This address counter employs 2 counter ICs to specify memory addresses sequentially starting from the lowest address using MO1 signal (shift pulses for addressing).
Therefore, after reading the header information, MO1 signal pulses must be output continuously until the starting address of the file. (With the ROM cartridge, random file addressing is not allowed.)

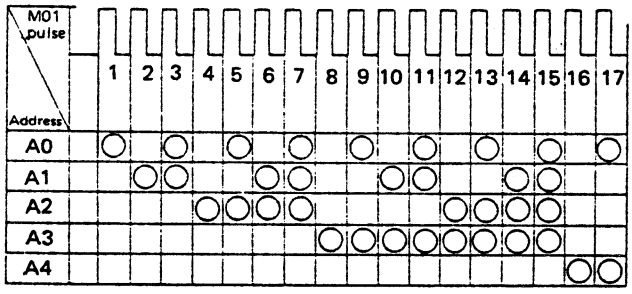


Fig. 4-2 M01 Shift Pulses for Addressing

(3) Shift register

The shift register reads 1 byte of data from the ROM and transfers the data bit by bit to the MI1 signal line (Serial Data Line) using "MO2" shift clocks.

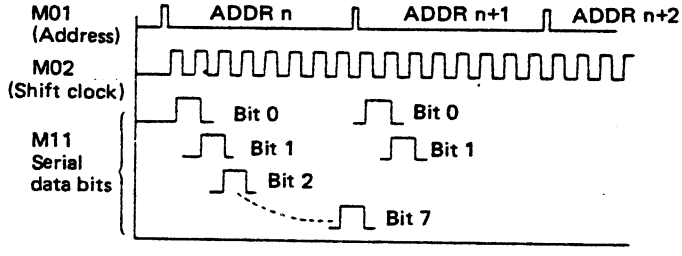


Fig. 4-3 Shift Clocks for Readout

(4) Operation sequence

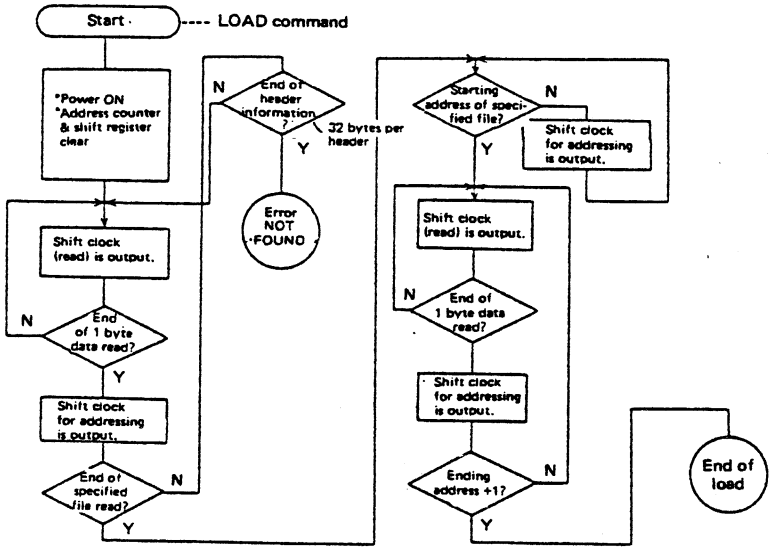


Fig. 4-4 LOAD Operation from ROM Cartridge

(5) ROM format

In the HX-20, the ROM cartridge is handled as a sequential file. Therefore, headers are provided in the starting address part of each file to facilitate file accessing. A maximum of 32 bytes of data may be set in each header.

NOTE: The HX-20 is designed to allow the setting of a maximum of 32 headers. However, the program for writing data into the ROM supports only 31 headers.

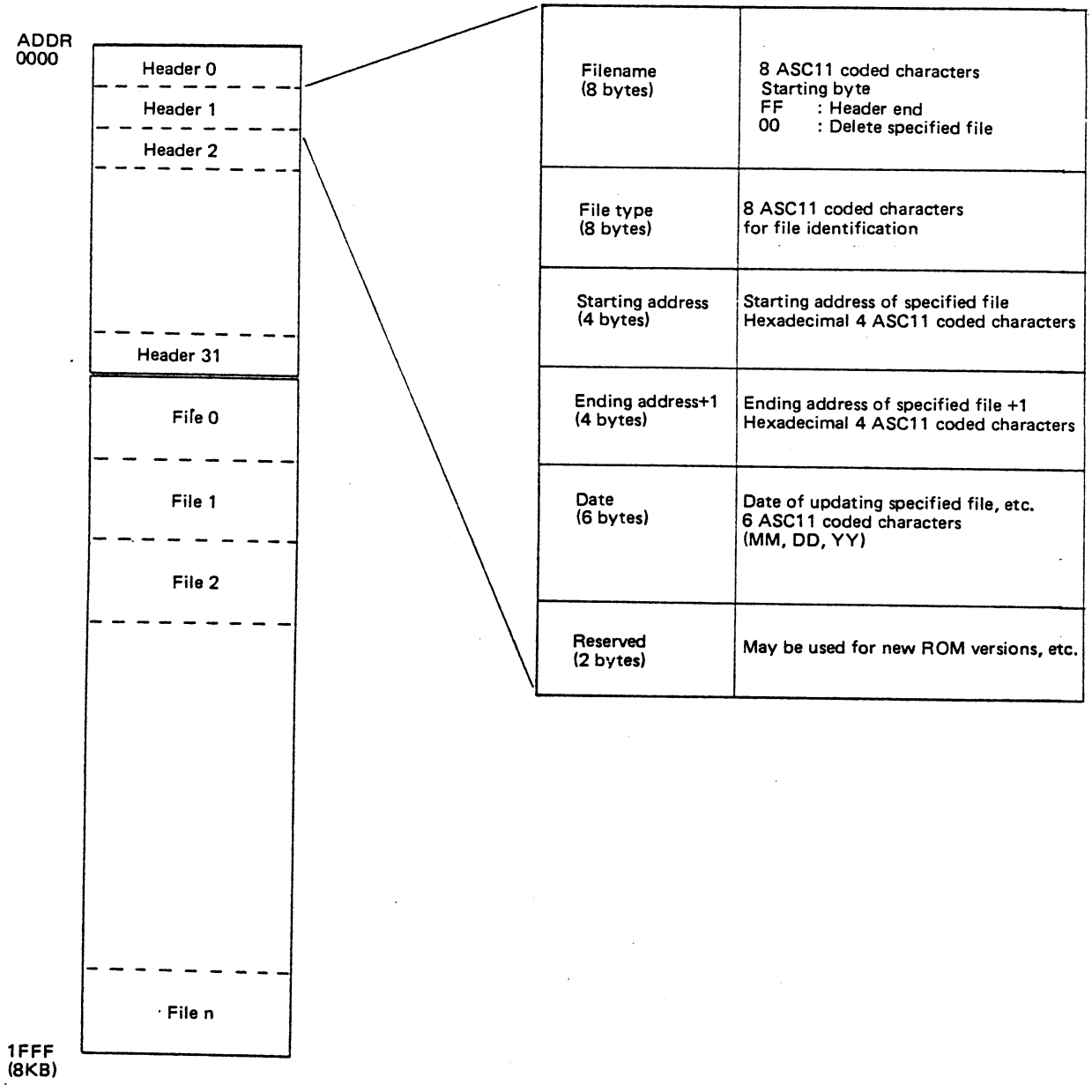


Fig. 4-5 ROM Format

4.1.2 Microcassette drive

The microcassette drive is controlled by both the master CPU and slave CPU. The mechanical operation of the microcassette drive is controlled by the slave CPU by commands which are output serially from the slave CPU and stored in the instruction register. The microcassette drive has a counter circuit incorporating a photo reflector. Using this counter circuit, the tape may be fast forwarded to the required position.

(1) Hardware configuration

The microcassette drive consists of a power supply section, a motor drive circuit section, a read/write control section, a motor speed control section, etc., and is designed to operate only when the power supply is turned ON.

The tape speed of 2.4cm/sec. is obtained using a capstan motor rated at 2,400 rpm. Data read/write is performed at a rate of 1,300BPS. Up to 50K bytes of data can be recorded on a 30-minute microcassette tape.

(2) Data read/write

Read/Write operations to and from the microcassette drive are the same as those with the external audio cassette, with the ON-OFF ratio of a read/write signal at 1KHz for OFF and 2KHz for ON. Data write format is also identical. Namely, one byte of data is written in 9 bits (consisting of 8 data bits and 1 stop bit).

(3) Operation sequence

The microcassette has two motors. One is used for loading or unloading the R/W head, while the other is a main motor used for driving the cassette reel. The two motors are controlled by the command bits set in the instruction register. As these commands are transferred serially, a shift register as shown in Fig. 4-6 is employed as an instruction register.

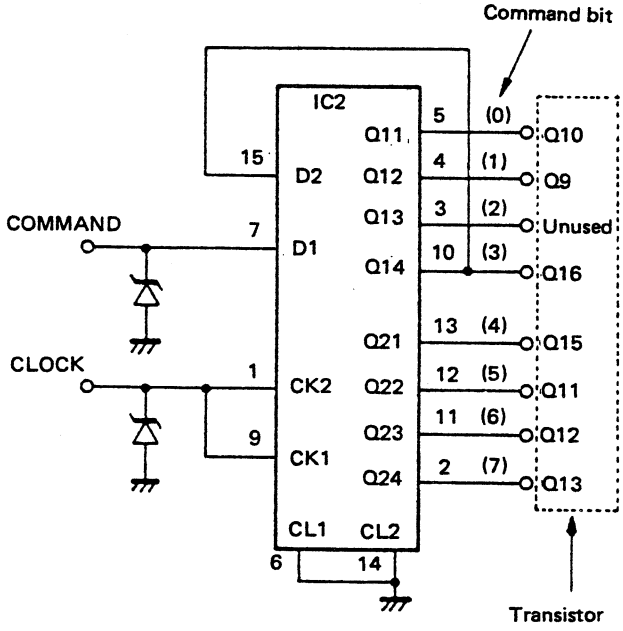


Fig. 4-6 Instruction Register

Outputs from the above instruction register serve as the inputs to the bases of the respective transistors controlling the motor operation.

The following 8 microcassette control commands are provided.

Table 4-1 Microcassette Control Commands

Command	Code (Hex)	Code bit 7	6	5	4	3	2	1	0	Function
STOP	00									Motor stop command
REW	0A					o		o		Tape rewind command
PLAY	01								o	Data read command
FF	11				o				o	Fast forward command
REC	81	o							o	Data write command
BRAKE	18				o	o				Capstan motor control command
HLD	20			o						Head load/unload command
H BRAKE	40		o							Head motor control command

An example of a series of operations from the fast forwarding of the tape, reading of data from the specified file to the termination of the data read operation is described below. (Also see Fig. 4-8.)

① The R/W head switch is checked to determine whether or not the tape is in the Unloaded state. If the tape is in the Loaded state, the head motor is activated to place the tape in the Unloaded state.
(In Fig. 4-7 below, the tape is in the Unloaded state when shaft C is disengaged from the pinch roller and in the Loaded state when shaft C engages the pinch roller.

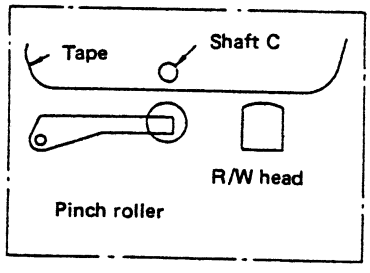


Fig. 4-7 Unloaded State of Tape

② After the motor power supply is turned off, both ends of the head motor are short-circuited and brake is applied to the head rotation due to the inertia of the head motor.
③ The capstan motor runs without speed control and the tape is fast forwarded until it reaches the specified count. (The tape feed length is counted by the photo reflector in the counter circuit.)
④ After the motor power supply is turned off, both ends of the capstan motor are short-circuited and brake is applied to the capstan motor.
⑤ The read/write head is placed in the Loaded state.
⑥ Brake is applied to the head motor rotated in the above step.
⑦ The tape is rewound at a constant speed and the tape is read. (The tape speed can be controlled to 2.4cm/sec.)
⑧ Brake is applied to the capstan motor.
⑨ The read/write head is placed in the Unloaded state.
⑩ Brake is applied to the head motor.
⑪ A STOP command is sent from the slave CPU to reset the contents of the instruction register to "00".

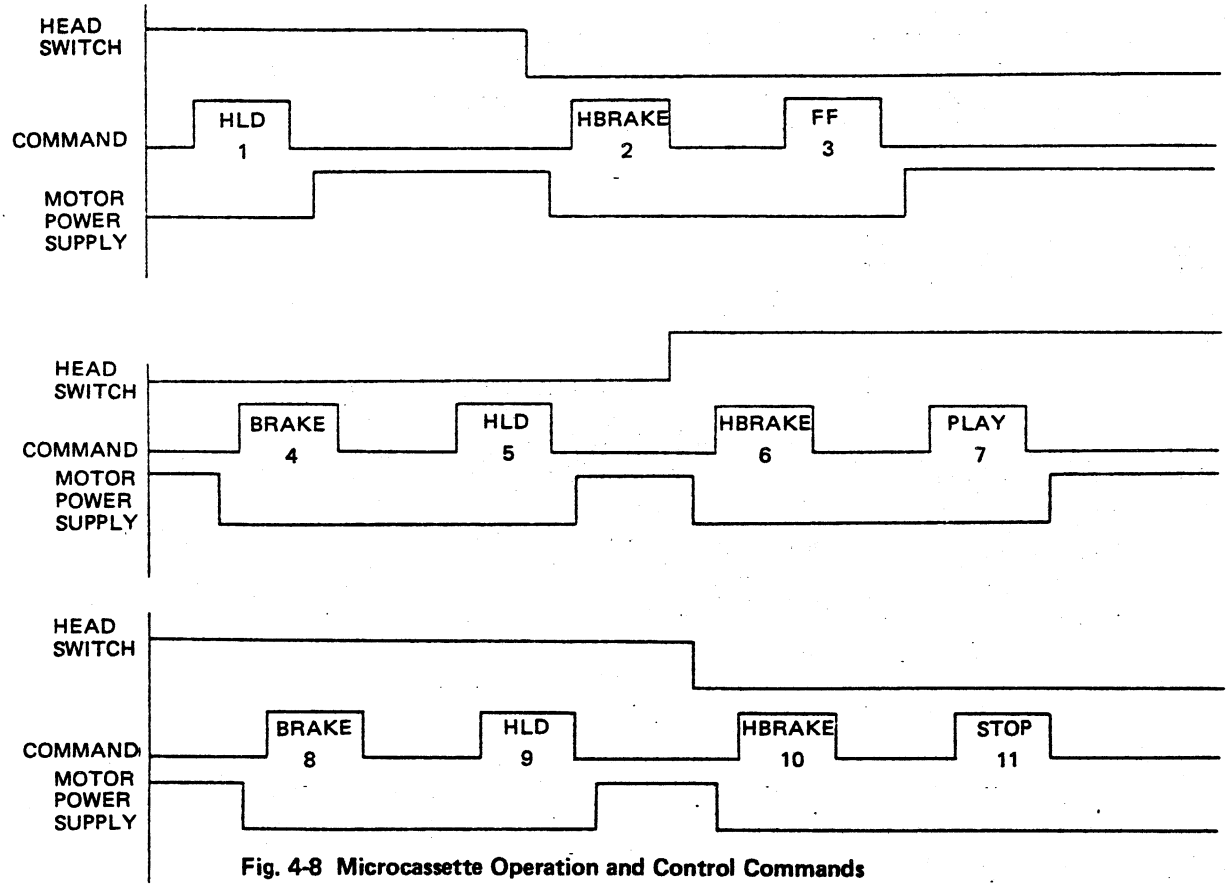


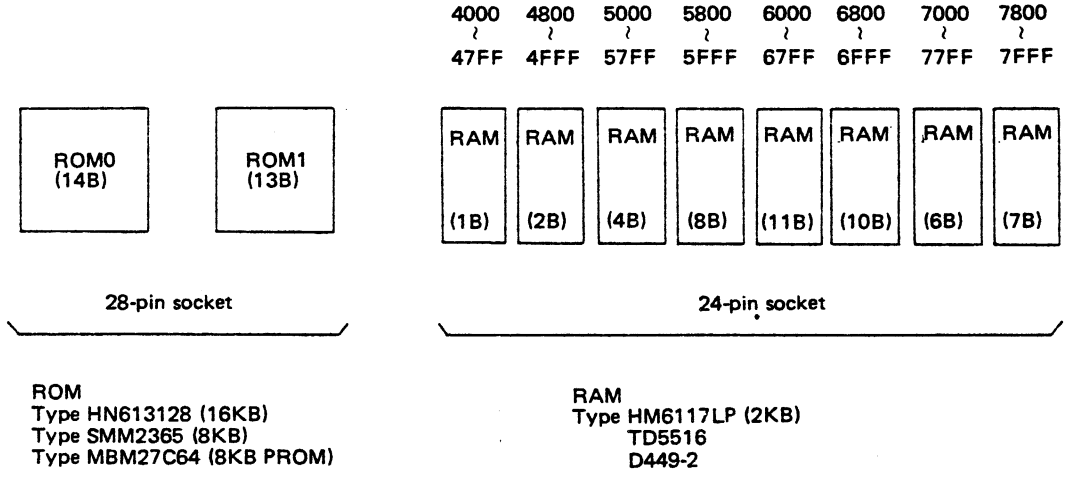
Fig. 4-8 Microcassette Operation and Control Commands

4.1.3 Expansion unit

The expansion unit is used for expansion of the ROM/RAM memory. The memory may be expanded up to 32K bytes.

(1) Expansion IC sockets

There are 2 28-pin IC sockets for ROM expansion and 8 24-pin IC sockets for RAM expansion as shown below.



ROM
Type HN613128 (16KB)
Type SMM2365 (8KB)
Type MBM27C64 (8KB PROM)

RAM
Type HM6117LP (2KB)
TD5516
D449-2

Fig. 4-9 Expansion IC Sockets

(2) RAM/ROM structure

The RAM/ROM memory can be expanded to a total of 32K bytes. Two jumpers (J1 and J2) and one DIP switch (SW2) are located on the Expansion Board for RAM/ROM memory assignment and ROM type (8KB/16KB) selection. (See Fig. 4-10.)

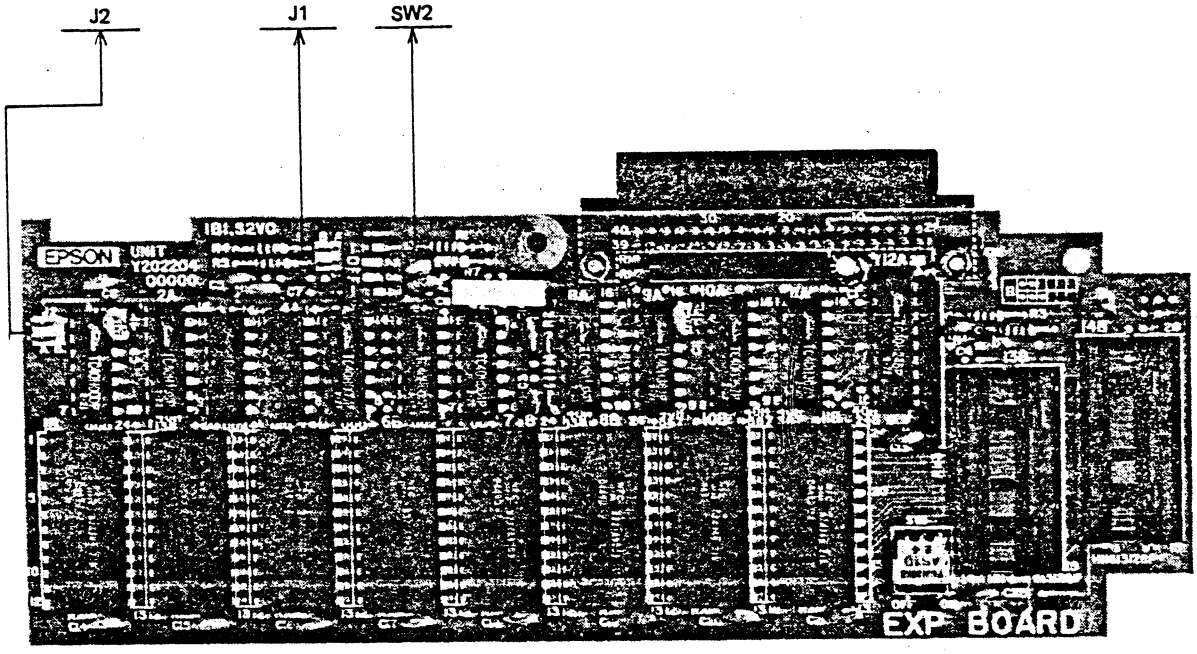


Fig. 4-10 Expansion Board

(3) Setting of jumpers J1 and J2 and DIP SW2

(a) The pin Nos. 1 and 2 of SW2 are used to assign RAM/ROM area.
NOTE: DIP SW1 is used to turn on and off the backup voltage (V_C) supplied from the HX-20.

(b) The pin Nos. 3 and 4 of SW2 and jumpers J1 and J2 are used to specify the ROM type (8KB/16KB) to be used.

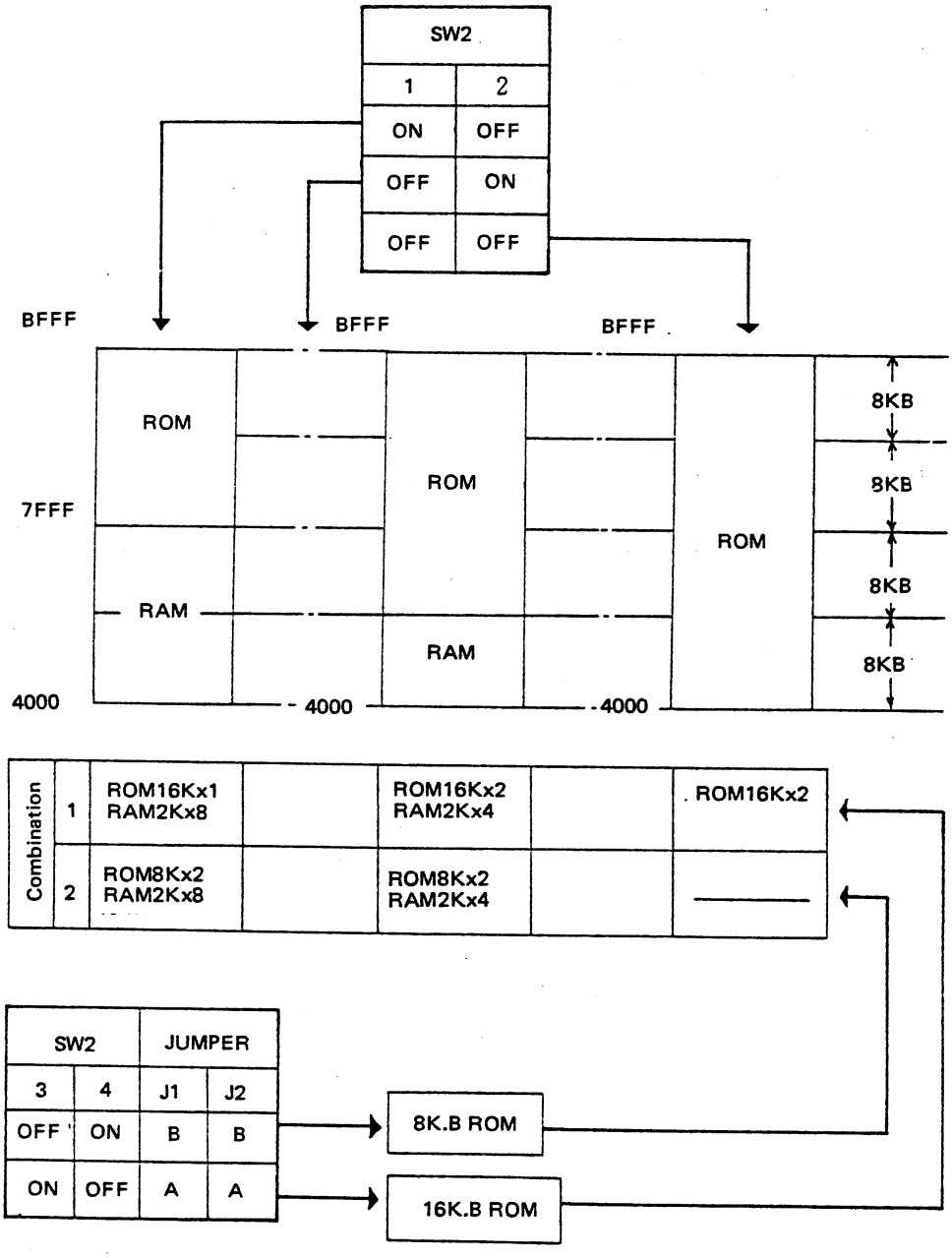


Fig. 4-11 Setting of Jumpers and DIP Switch

(4) Bank switching

The HX-20 can directly address up to 64K bytes of memory space (65,536 addresses). However, the memory capacity of the HX-20 may exceed 64K bytes when an expansion unit is connected to the HX-20. Therefore, bank switching is executed in the HX-20 so that the CPU can access a different memory area with the same logical addresses. The bank switching can be done by both the hardware and software. As the HX-20 operates in Multiplexed/RAM mode, addresses 0100 to FFFF can be used by the external memory. The addresses 4000 to BFFF (32K bytes in total) of this external memory area can be accessed by switching the ON/OFF position of the bank select DIP switch. The ROM E signal line is also available as a control signal on connector 7. This signal may be used to disable the ROM (address 8000 to FFFF) provided in the HX-20 as standard equipment.

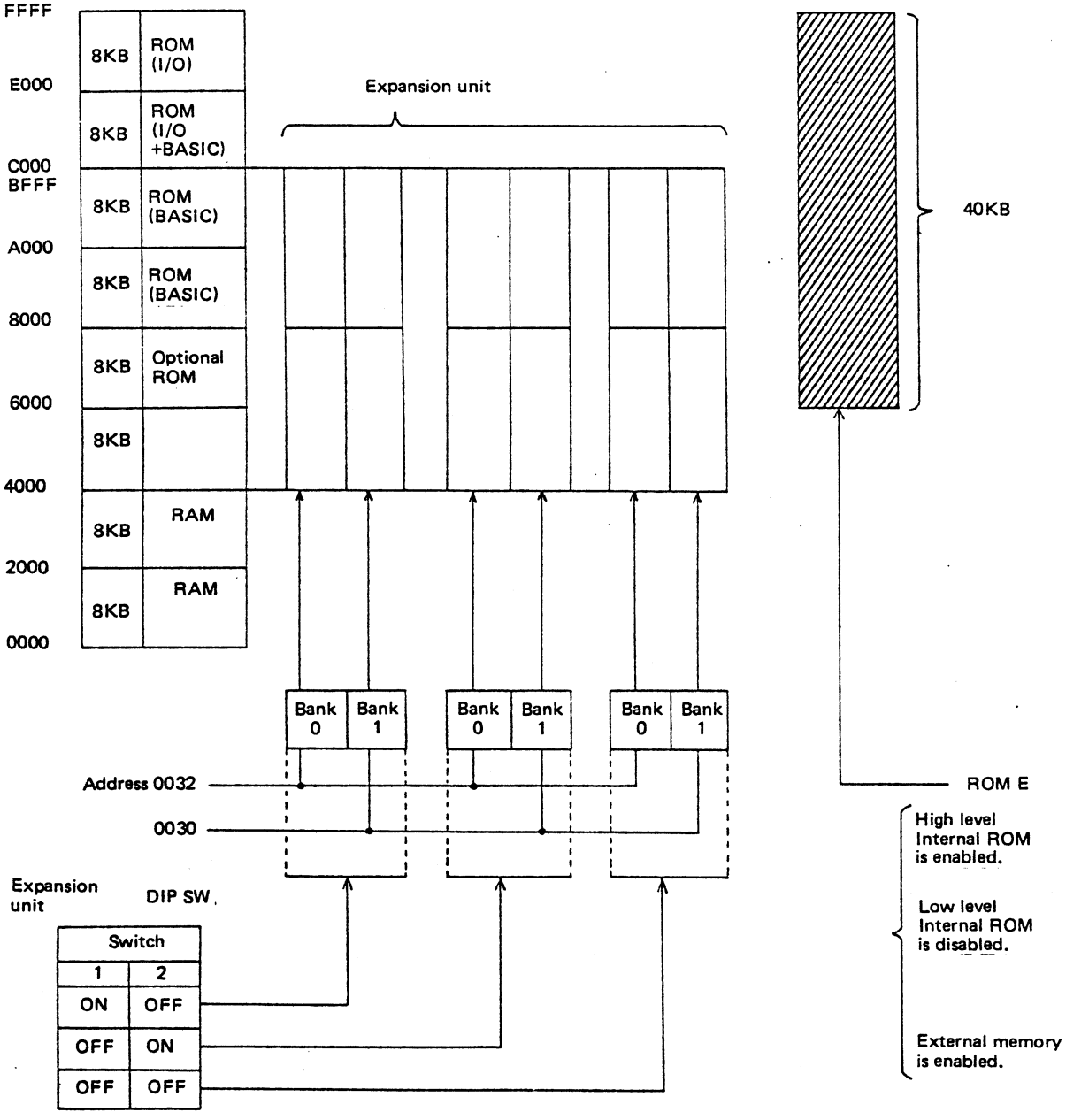


Fig. 4-12 Bank Switching

(5) ROM E (Internal ROM ENABLE)

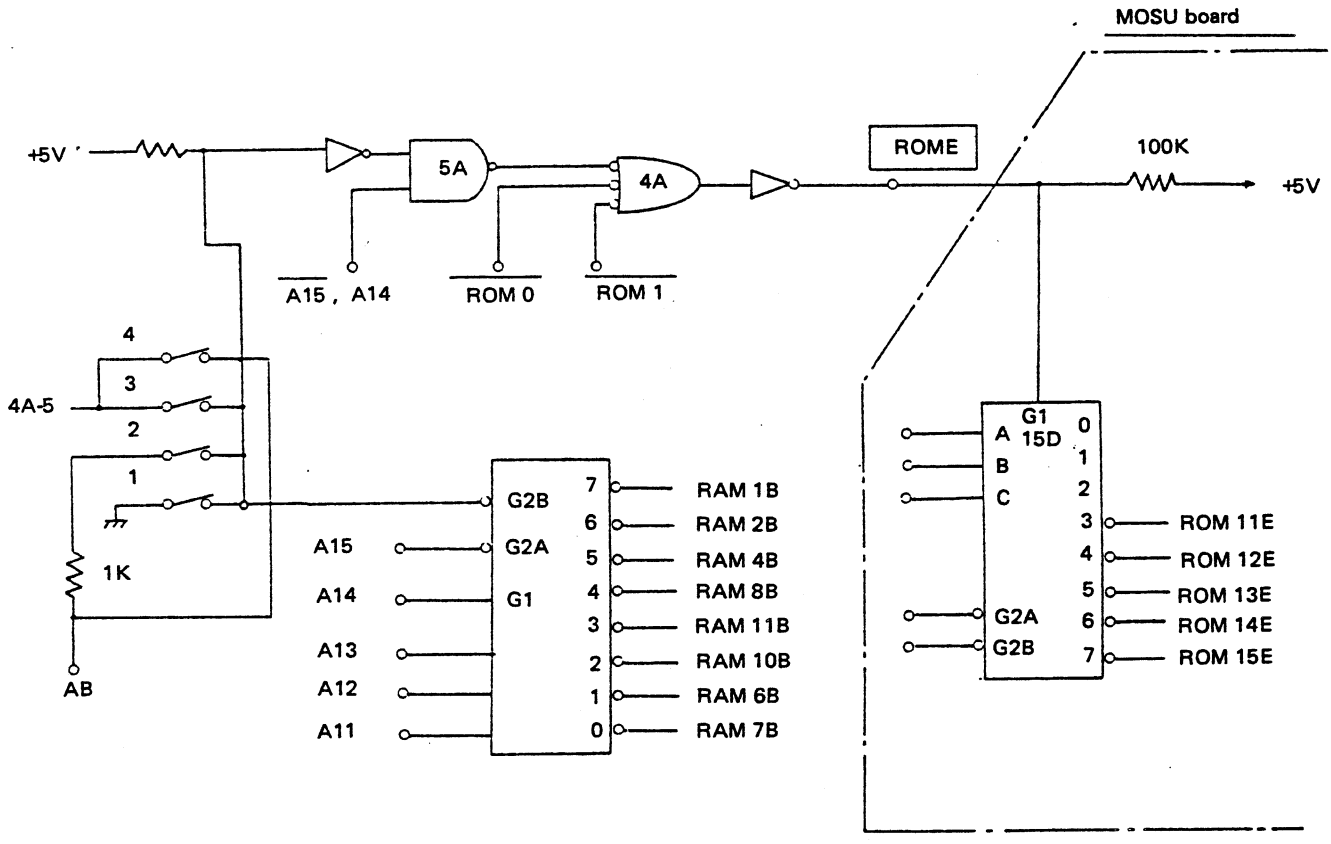


Fig. 4-13 ROM E Signal

The ROM E signal is normally High to select the internal ROM (addresses 6000 to FFFF) of the HX-20. This signal goes Low when the addresses higher than 6000 of the ROM0, ROM1 or RAM in the expansion unit are selected, thus disabling the internal ROM of the HX-20. Accordingly, with this ROM E signal, the internal or external memory having the same addresses can be used as required.

4.1.4 Display

As the master CPU operates in Expanded Multiplex mode "6", the memory map for display is as shown below.

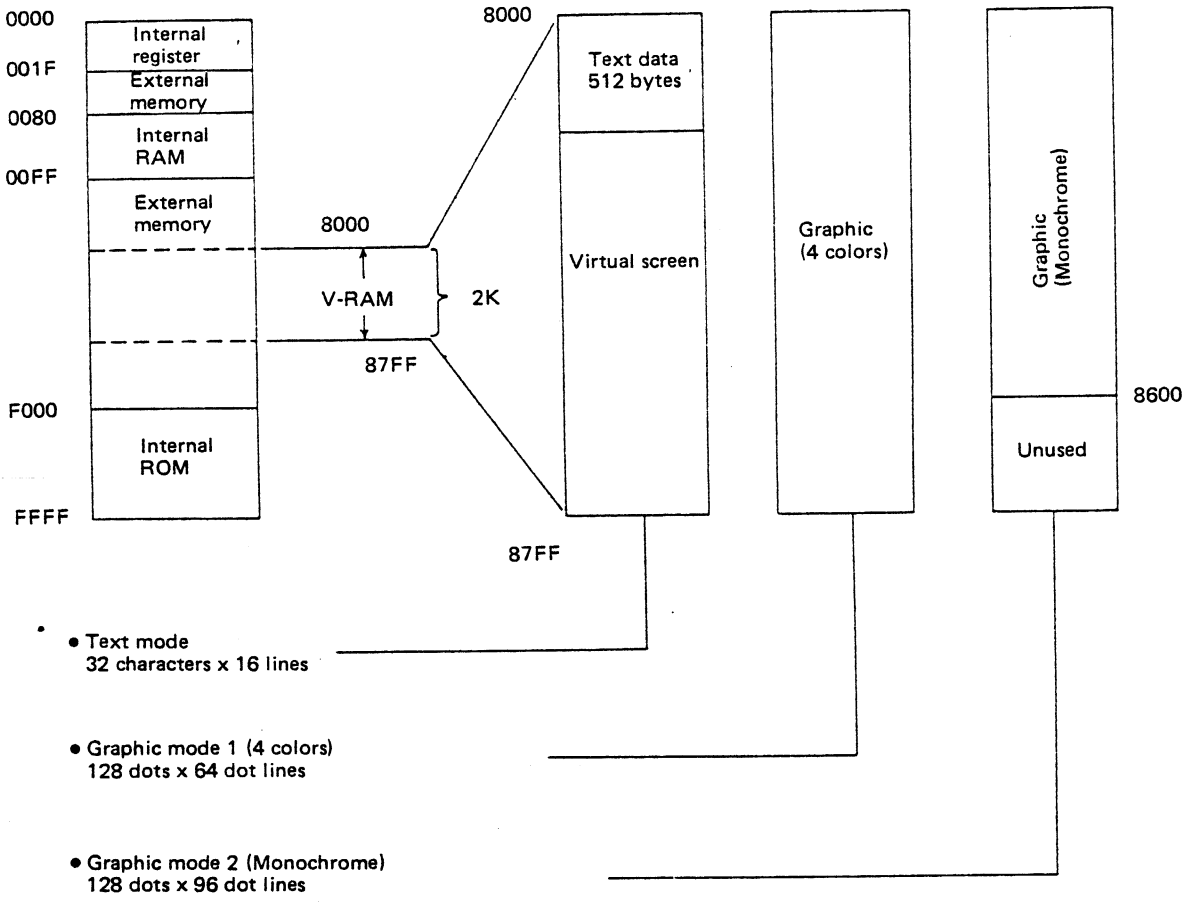


Fig. 4-14 Memory Map for Display

4.1.5 Floppy disk unit

The EPSON TF-20 Terminal Floppy is a floppy disk unit that can be connected to the HX-20 via a serial interface. The floppy disk unit has two 320KB disk drives and enables the use of DISK BASIC.
(Disk specifications: 16 sectors/track, 40 tracks/drive, double-sided double-density)

4.2 Applications

The HX-20 is an all-in-one type portable computer incorporating an LCD and a microprinter as standard equipment. The HX-20 also has the built-in rechargeable battery to allow the use of the computer for an extended period without connecting it to the AC power receptacle.

As all the operations of the HX-20 are supported by EPSON-MICROSOFT BASIC, programs can be developed with ease. If necessary, programs can be written in machine language using the computer in the Monitor mode. Therefore, systems ideal for a wide variety of applications can be configured by adding various EPSON options to the HX-20.

(1) Changing the interface operation

The HX-20 is equipped with a total of 6 interfaces (i.e., RS-232C, Serial, Barcode reader, External cassette, optional cartridge and expansion unit). These interfaces can operate entirely different from what they are originally intended if the programs to control their operations are modified. In this case, use of more effective BASIC subroutines and preparation of machine language programs will become necessary.

(2) Connecting the external unit

Special external units meeting the specific applications may be connected to the HX-20 interfaces. When connecting such units, careful consideration must be given to the interface specifications, timing, power requirements, etc. If the external unit to be connected to one of the HX-20 interfaces is an intelligent type, the external unit may have its own control functions. By so doing, the interface may operate entirely different from what it is originally intended by operating a relatively simple program from the HX-20 side.

If the external unit is not of an intelligent type, all the functions of the external unit must be controlled by the HX-20, which may require the use of a more sophisticated control program.

In any case, it is best to connect the external unit to the external unit interface of the HX-20 to which the address/data bus is open.

4.2.1 Power supplies

When connecting special units to the HX-20 to expand the system functions, pay attention to the points described below. Also note that the external units to be connected to the HX-20 have their own power supplies, since the built-in battery of the HX-20 has a limited capacity (approx. 1100mAH).

(1) Cautions when operating the external unit with the built-in battery of the HX-20

(a) The V_L line (line voltage) must be 50mA max. at +5V.

(b) The V_B (battery voltage) line must be 1000mA max. at +5V.

(c) The V_C (backup voltage) line must be 40mA max. at +5V.

(d) A fuse (1A max.) must be attached to the V_B line for overcurrent protection.

(e) The V_C line must be connected to the GND (Signal Ground) through a 30μF electrolytic capacitor at the external unit. Also, attach a 0.01μF (capacitor to the circuit wired to each element and to the V_{CC} of each element (RAM, ROM, etc.), respectively for voltage stabilization or noise prevention.

(2) Cautions when operating the external unit with its own power supply.

(a) The power supply section of the external unit must have an independent ground line (in the 3-conductor power cord).

(b) The ground line must be separate from the signal ground.

(c) The power supply lines of the HX-20 must not be connected to the external unit.

(d) The external unit must have its own reset circuit so that it does not operate before the HX-20 becomes ready for operation.

(e) The external unit must have a protective circuit against abnormalities in the power supply (overvoltage, overcurrent, low voltage, etc.).

(f) The external unit must be provided with measures against noise due to electromagnetic waves, etc.

(g) The external unit must satisfy all other requirements specified in the safety and various other standards.

(3) Power ON/OFF control

When operating the external unit with the built-in battery of the HX-20, pay attention to the following points.

(a) V_B line

° Power must be turned on and off with the built-in switch of the external unit or by the program so as to prevent the unwanted battery consumption except when the external unit is in operation.

° The V_B voltage line must be protected against overcurrent by inserting a fuse rated at 1A max.

Example:

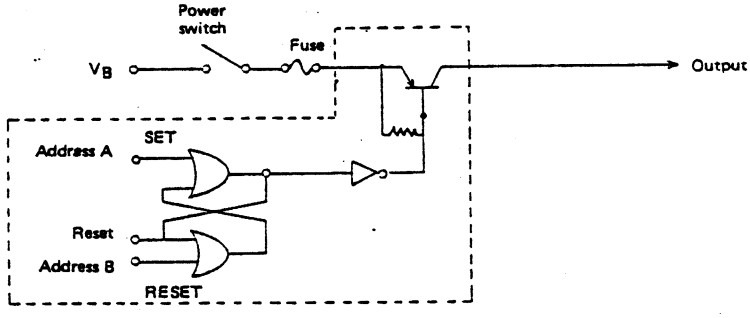


Fig. 4-15 Overcurrent Protection

The circuit enclosed by the dotted line in the above figure indicates a power ON/OFF circuit which uses two addresses for power ON/OFF control.

By this circuit, the unwanted battery consumption may be prevented by turning the power ON only when the external unit is used and turning it OFF immediately after the unit has been used.

(b) V_C line

° Use of this line must be limited to only the case where the external unit requires battery backup voltage.

° The V_C line must not be connected to any other voltage lines such as V_L (line voltage).

° The element to be backed up must be of a C-MOS type.

(c) V_L line (+5V)

° This line must not be used when load fluctuations on the external unit side are great.

4.2.2 Interfaces

The interface cables specified by EPSON must be used for RS-232C and serial interfaces which employ a USART IC in the interface board. When using other than the above two interfaces such as expansion unit interface, etc., pay attention to the following four points.

(1) Connection

- ° Use a connector conforming with the interface standard.
- ° Secure the expansion unit interface connector using the screw (M3x8) mounting holes provided on the side of the HX-20 for this purpose.
- ° The distance between the expansion unit interface and the I/O elements on the external unit should be less than 150mm. Avoid the use of an interface cable, etc. as much as possible. If the interface cable is required, see paragraph (2) below.

(2) Interface specifications

Signals for the expansion unit interface, cartridge interface, etc. are output directly from the master or slave CPU. Therefore, the interfacing distance between the HX-20 and the external unit must be minimized and a line buffer (or driver) be provided on the external unit to prevent signal levels from dropping as well as to prevent the HX-20 from malfunctioning due to noise. The interface differs depending on the cable material, elements, etc. used. However, the interfacing distance from the I/O connector section of the HX-20 to the line buffer on the external unit must be less than 150mm.

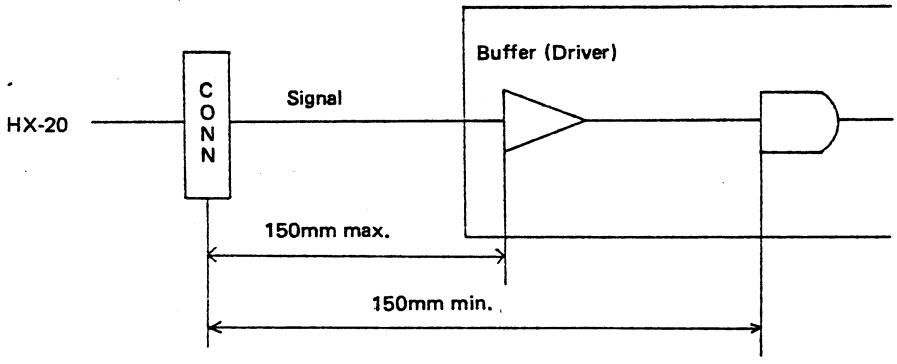


Fig. 4-16 Interfacing Distance

(3) Interface cables
The interface cable to be used for connection of the external unit to the HX-20 must be twisted pair. The return wire of each signal line must be connected to the signal ground.
The interface cable must also be shielded and the both ends of the shield be connected to the chassis grounds of the HX-20 and the external unit, respectively.
Connect the return side of twisted line to grounding terminal.

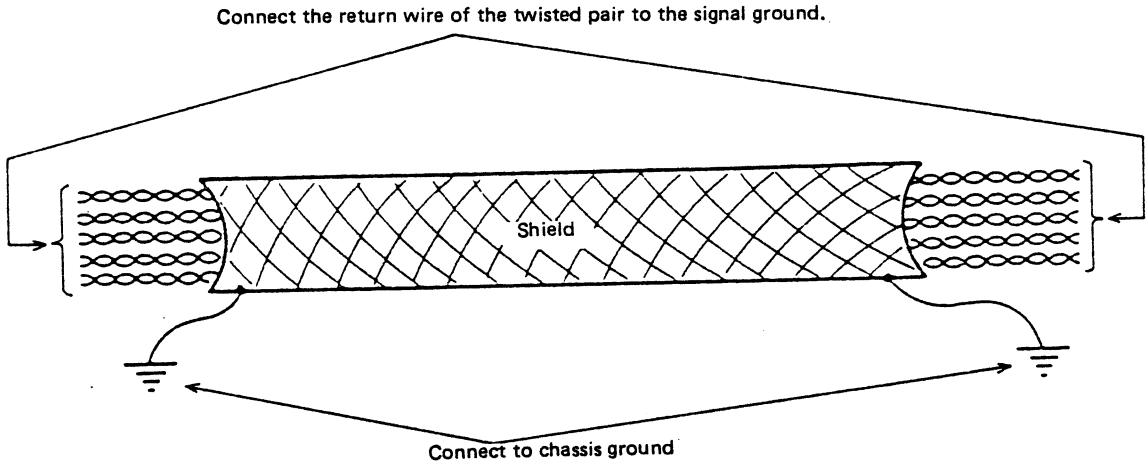


Fig. 4-17 Connection of Interface Cable

NOTES:
1. The length of the interface cable must be minimized, as the extensible cable length is governed by the cable material and the type of element used as a signal driver.
2. When using the interface, avoid use of the HX-20 power supplies (V_B, V_L and V_C) as much as possible to prevent voltage drop.
   - Input signal lines to the HX-20 and all other signal lines except voltage and ground lines must be connected to the signal GND via a 1MΩ resistor.
   - A bidirectional gate circuit (H245, etc.) must be provided for each data bus line.
   - Use of open collector type elements is recommended for the input signal lines to the HX-20.
   - The signal levels for the external unit must be TTL compatible.
   - The signal GND must be separate from the chassis GND.
   - When the external unit has a built-in power supply, make sure that noise due to power ON/OFF does not have any adverse impact on the signal lines.

[Application Example]

° Memory expansion

When the same control as that for the expansion unit is to be effected on external units via the interface connector CN7 on the MOSU board, memory may be expanded up to 40K bytes (address "6000" to "FFFF") per bank by using unassigned addresses "0030" to "003F" for bank switching. If multiple banks are to be used, a program is required to cover the set/reset control involved in the bank switching.

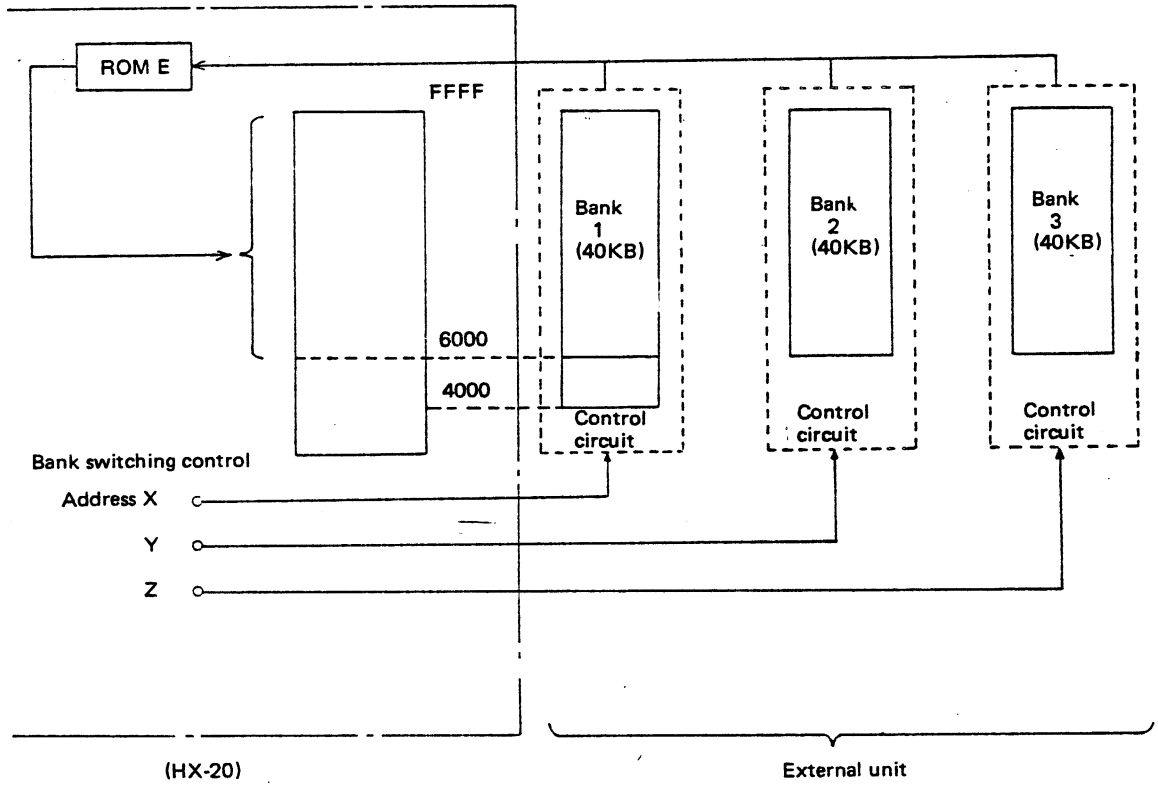
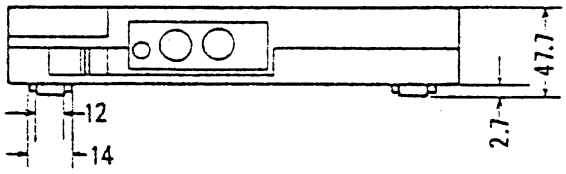


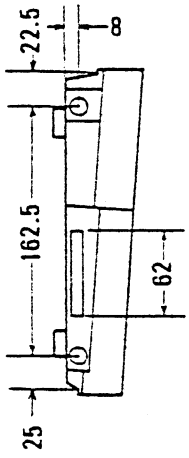
Fig. 4-18 Bank Switching Control

APPENDIX 1 OUTLINE DIMENSIONED DRAWINGS

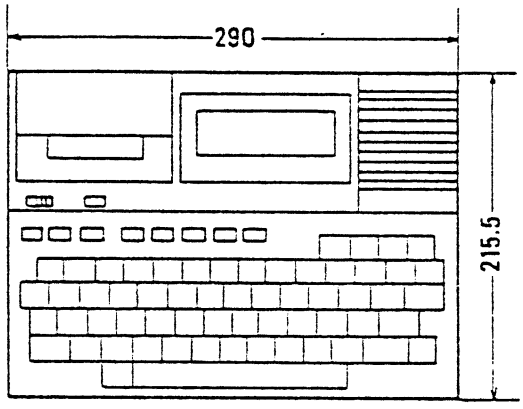
APP1-1 Outline Dimensions of HX-20



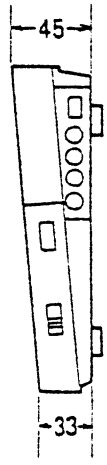
(Rear View)



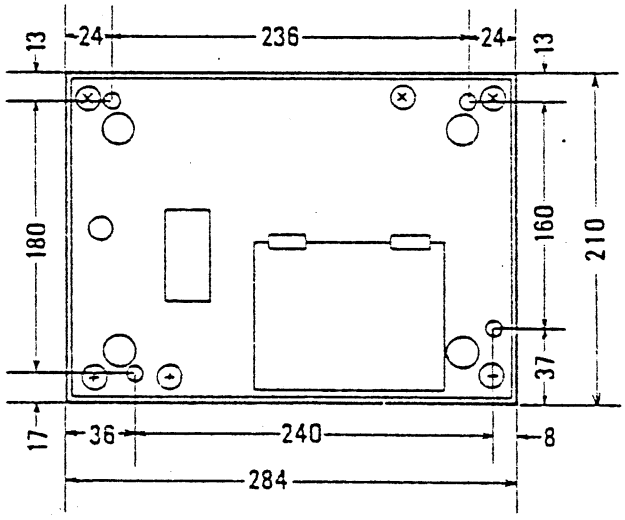
(Left Side)



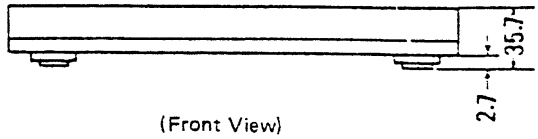
(Top View)



(Right Side)



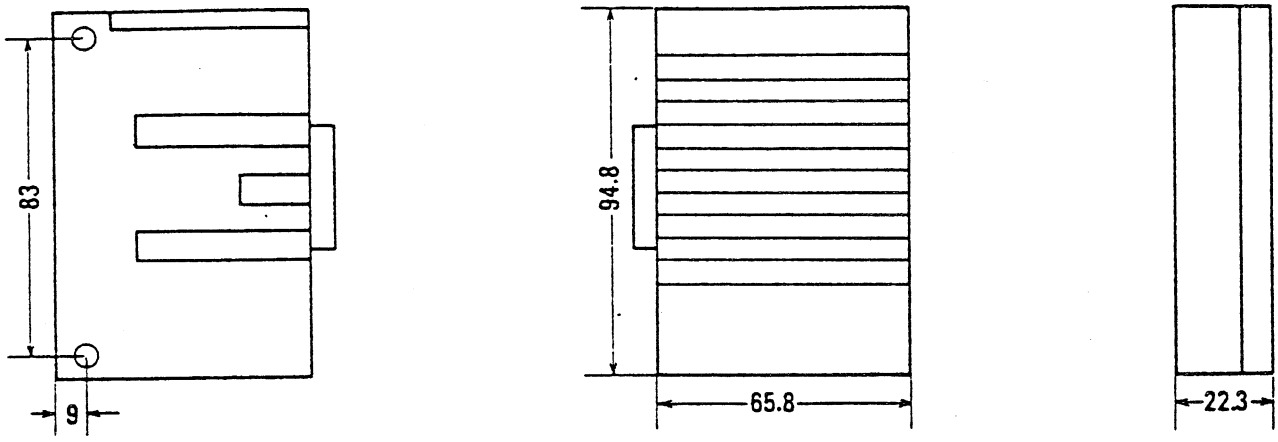
(Bottom View)

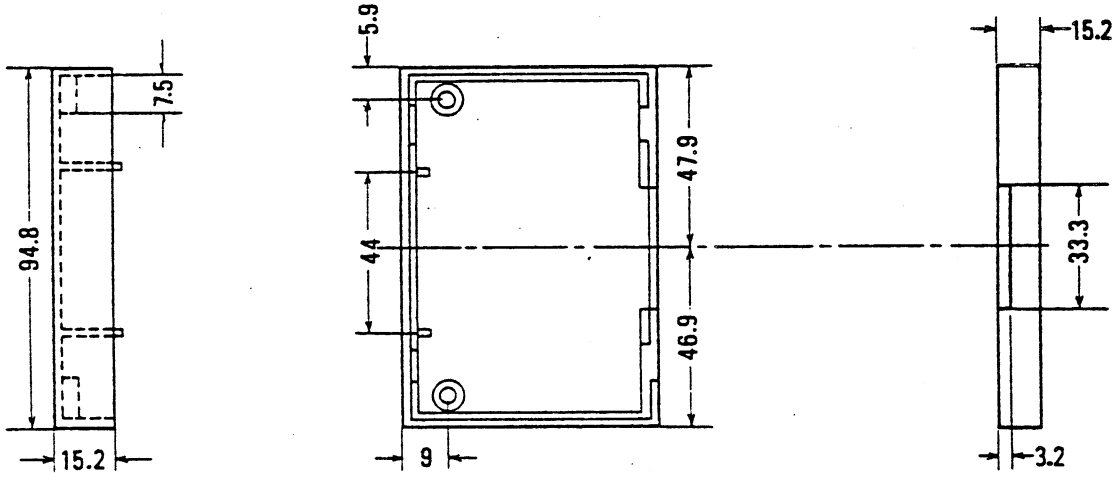


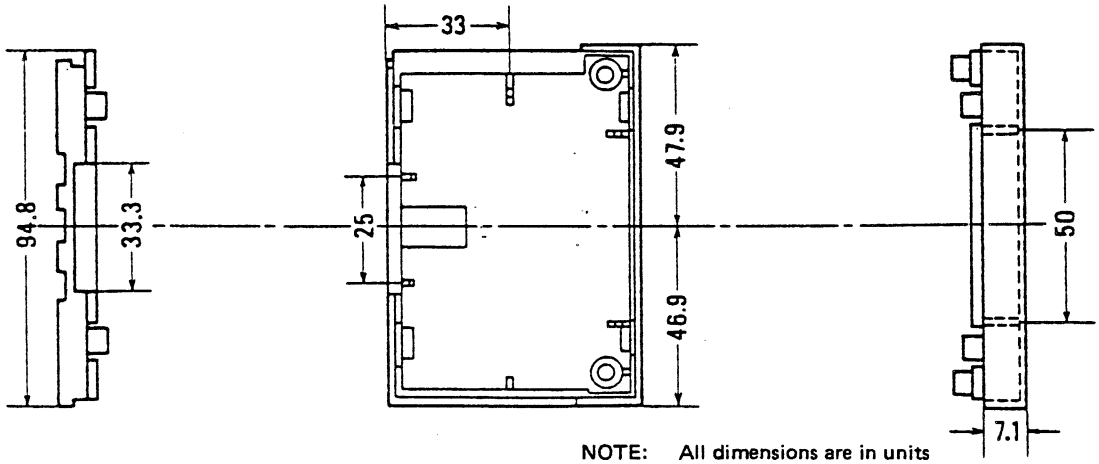
(Front View)

NOTE: All dimensions are in units of millimeters.

APP1-2 Outline Dimensions of ROM Cartridge

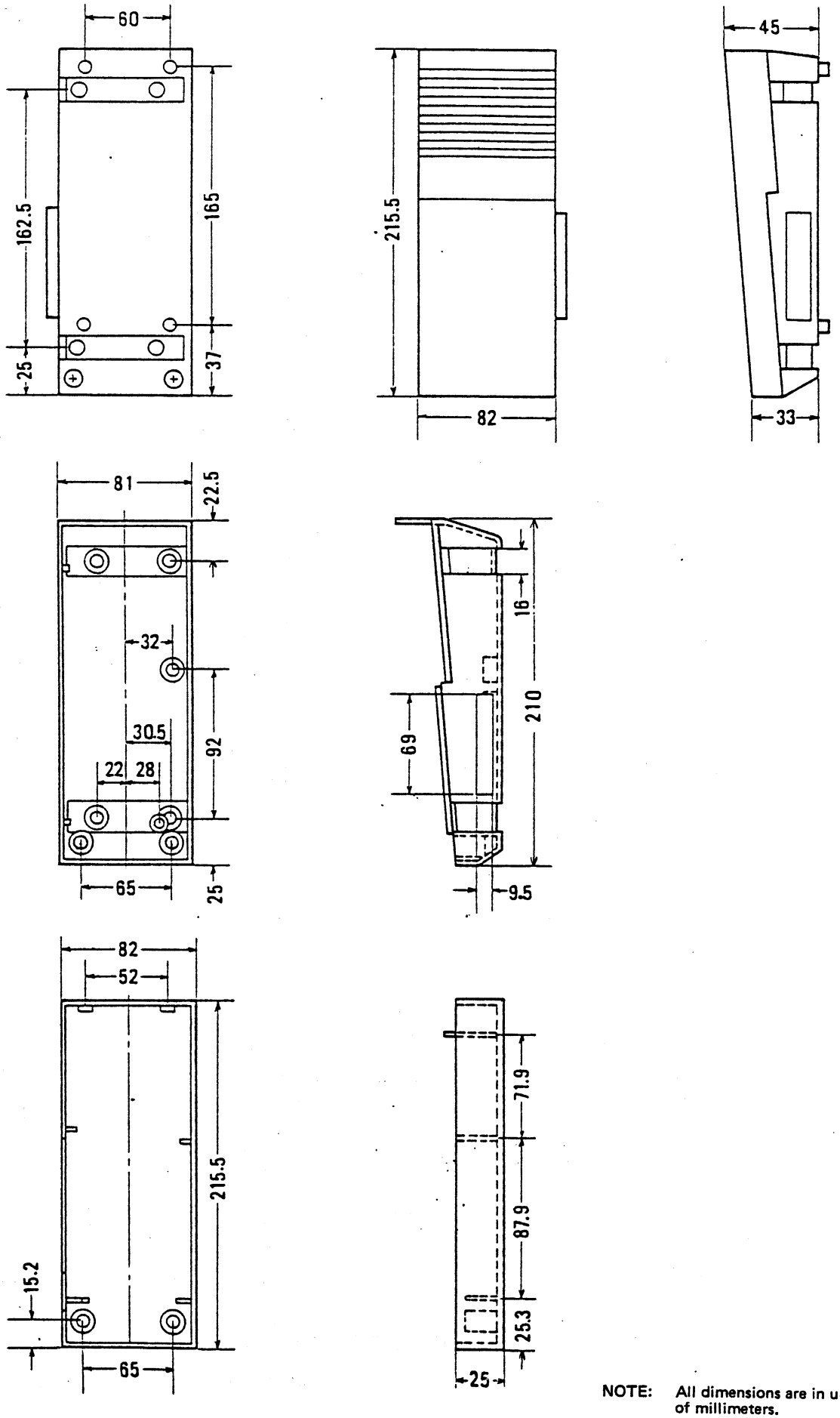






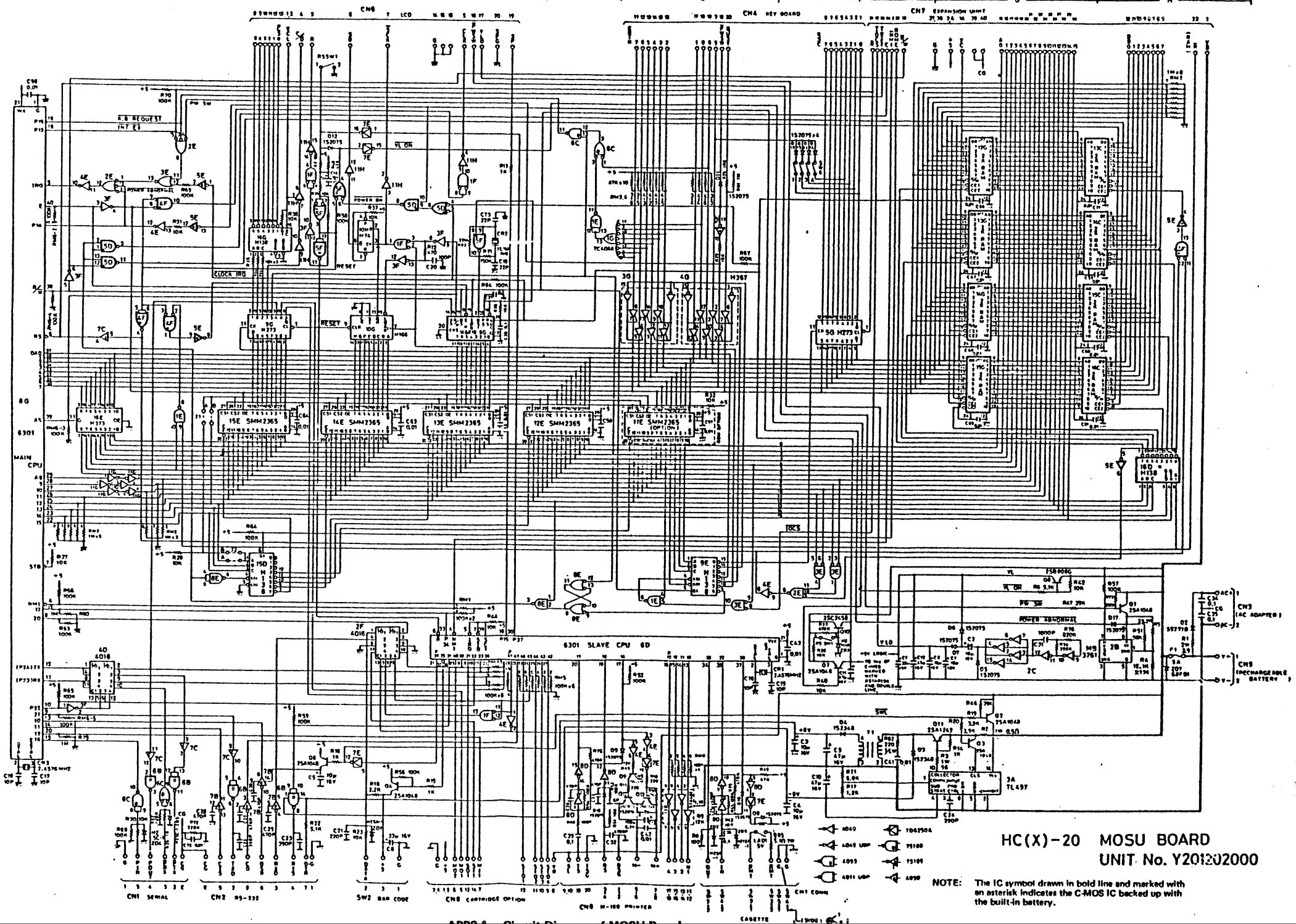
NOTE: All dimensions are in units of millimeters.

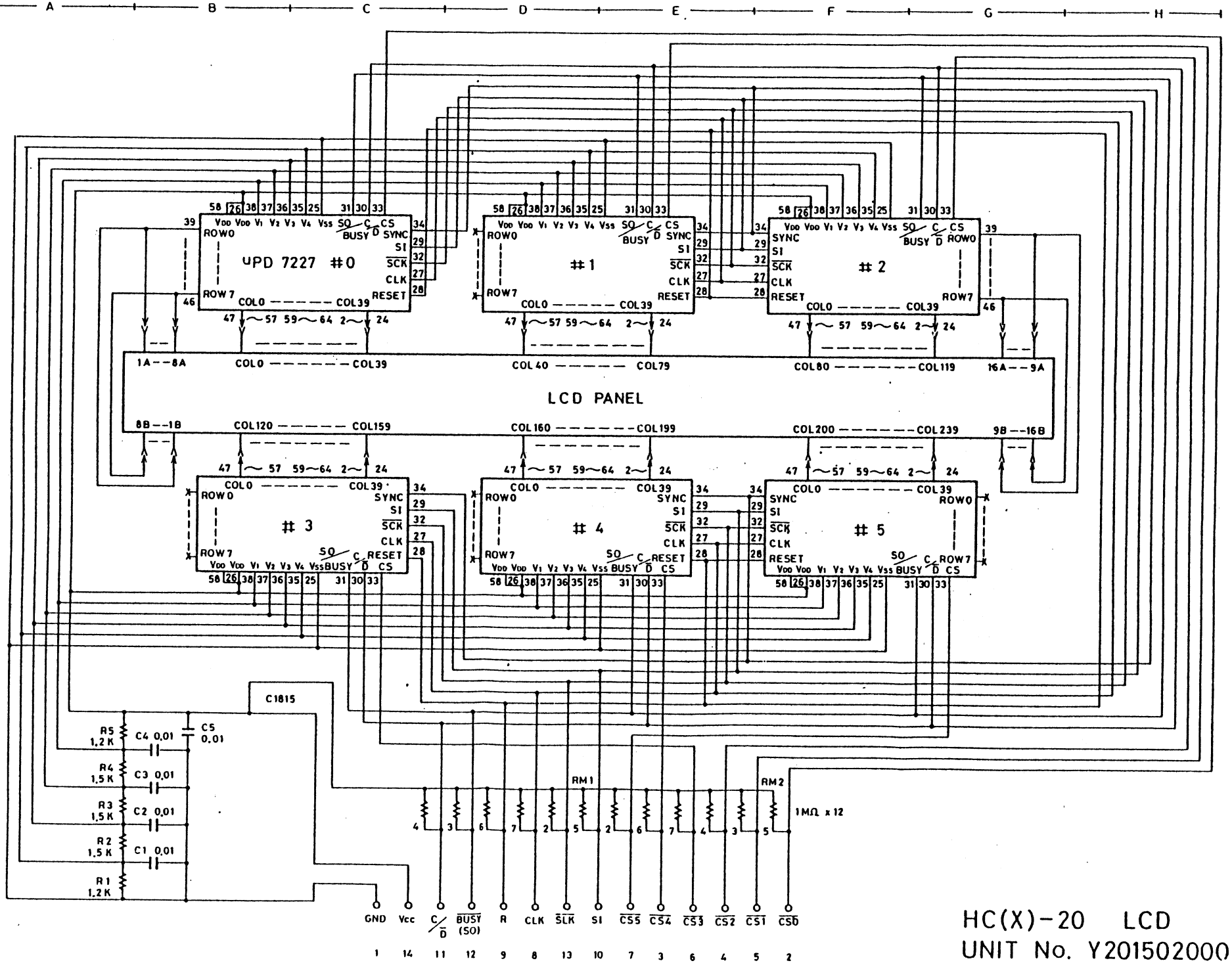
APP1-3 Outline Dimensions of Expansion Unit



NOTE: All dimensions are in units of millimeters.

APPENDIX 2 CIRCUIT DIAGRAMS

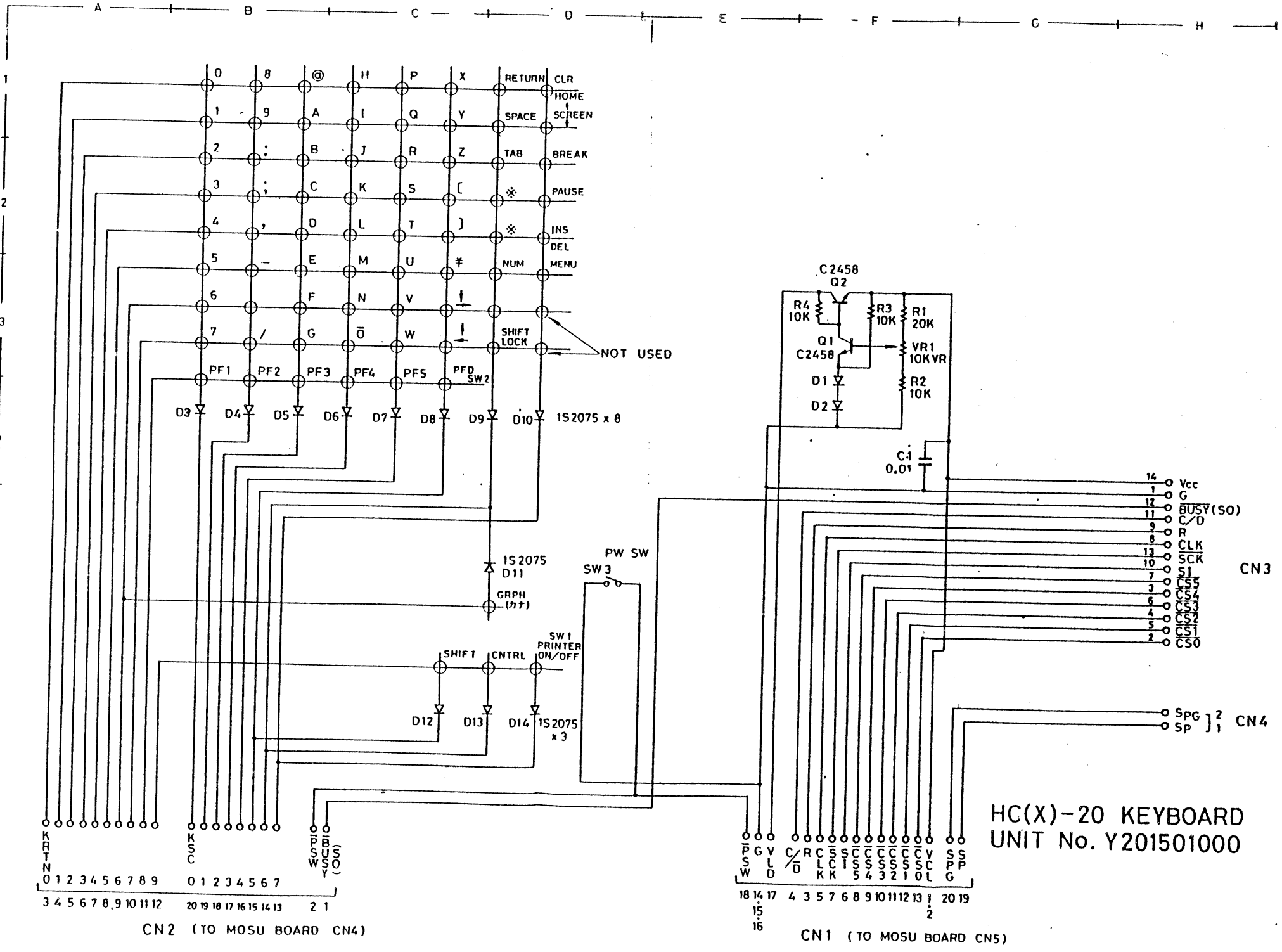

HC(X)-20 MOSU BOARD
UNIT No. Y201202000
NOTE: The IC symbol drawn in bold line and marked with an asterisk indicates the C-MOS IC backed up with the built-in battery.
6301 SLAVE CPU
MAIN CPU
CN1 SERIAL
CN2 RS-232
SW2 BAR CODE
CN8 CARTRIDGE OPTION
CN8 M-100 PRINTER
CN7 EXPANSION UNIT
CN4 KEY BOARD
CN3 (AC ADAPTER)
CN9 (RECHARGEABLE BATTERY)



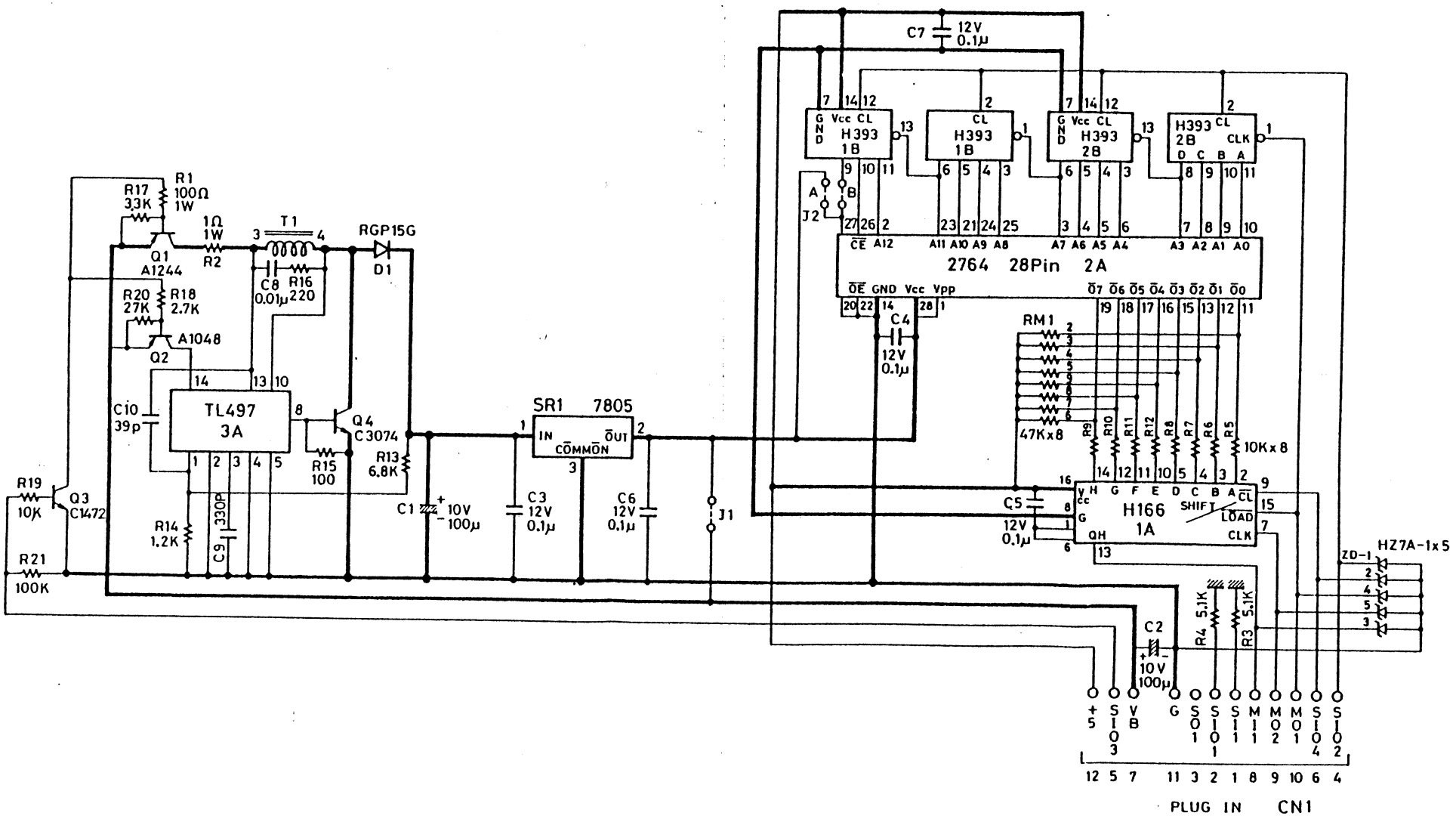
HC(X)-20 LCD
UNIT No. Y201502000

CN1 (TO KEYBOARD CONNECTOR CN3)

APP2-2 Circuit Diagram of LCD

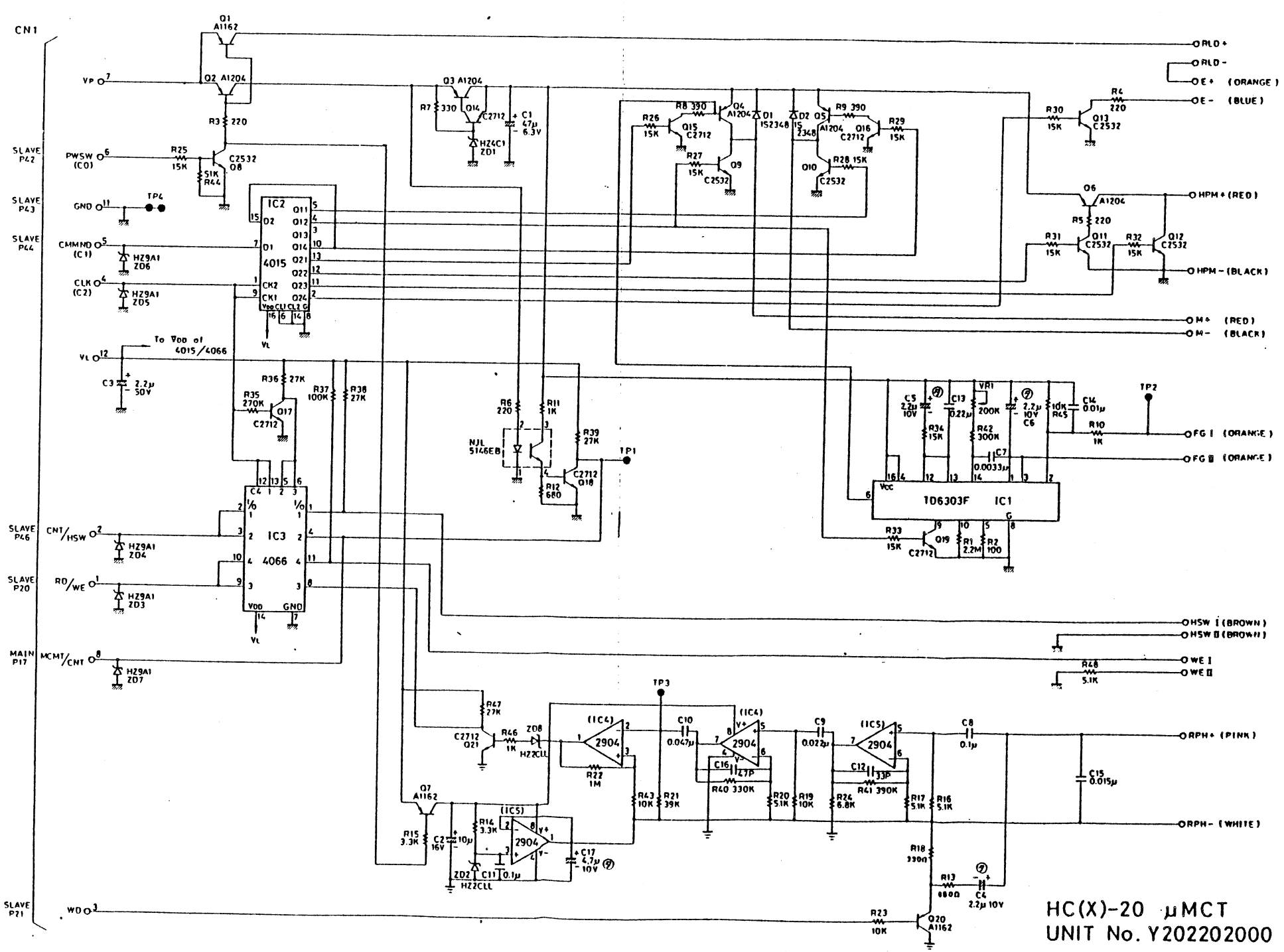


APP2-3 Circuit Diagram of Keyboard

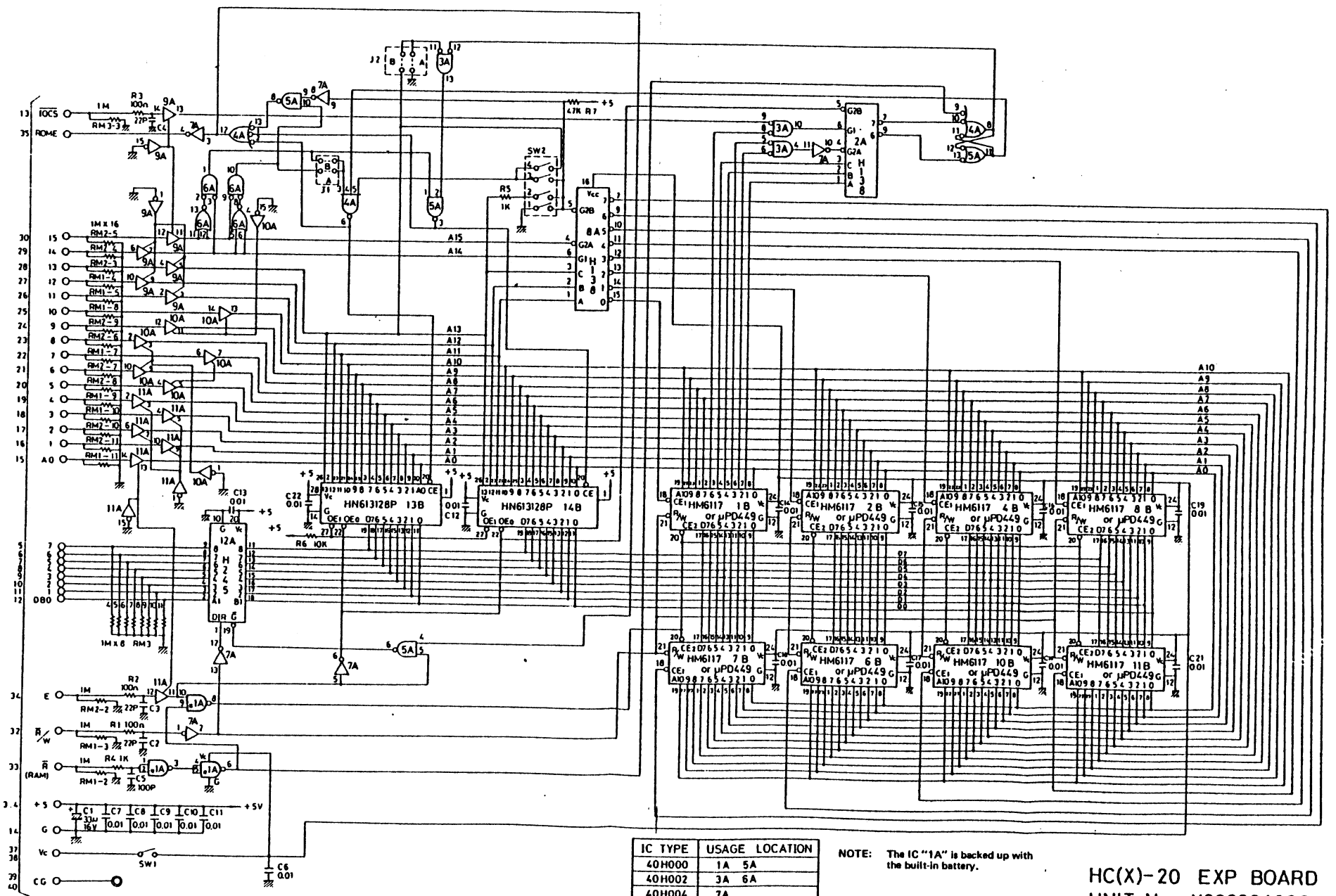


HC(X)-20 ROM CAT
UNIT No. Y202201000

APP2-4 Circuit Diagram of ROM Cartridge



APP2-5 Circuit Diagram of μMCT

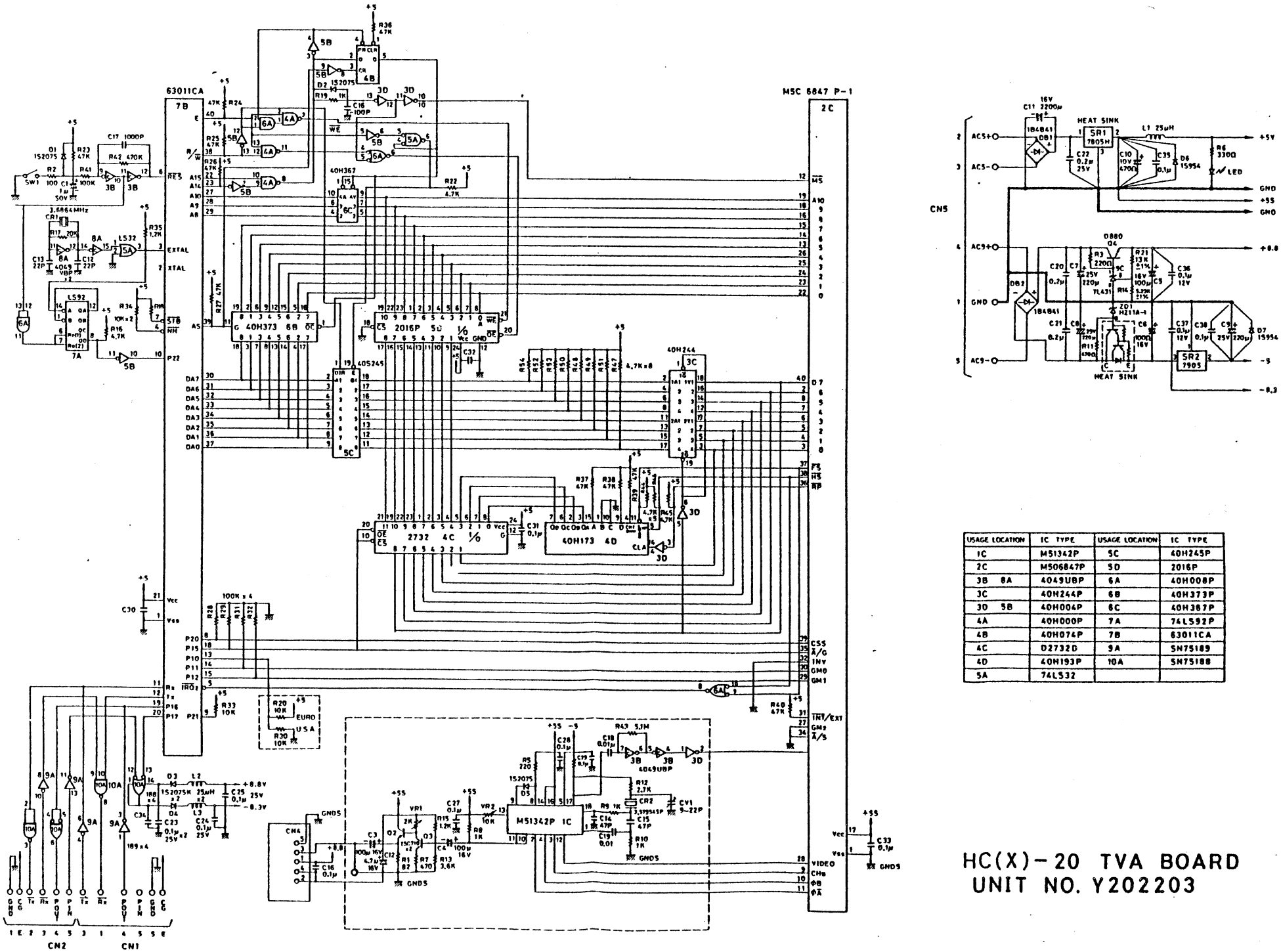


IC TYPE	USAGE LOCATION
40H000	1A 5A
40H002	3A 6A
40H004	7A
40H010	4A
40H138	2A 8A
40H367	9A 10A 11A
40H245	12A

NOTE: The IC "1A" is backed up with the built-in battery.

HC(X)-20 EXP BOARD
UNIT No. Y202204000

APP2-6 Circuit Diagram of EXP Board



USAGE LOCATION	IC TYPE	USAGE LOCATION	IC TYPE
1C	M51342P	5C	40H245P
2C	M506847P	5D	2016P
3B 8A	4049UBP	6A	40H008P
3C	40H244P	6B	40H373P
3D 5B	40H004P	6C	40H367P
4A	40H000P	7A	74LS92P
4B	40H074P	7B	63011CA
4C	D2732D	9A	SN75189
4D	40H193P	10A	SN75188
5A	74LS32		

HC(X)-20 TVA BOARD
UNIT NO. Y202203

SECTION 3 SOFTWARE